



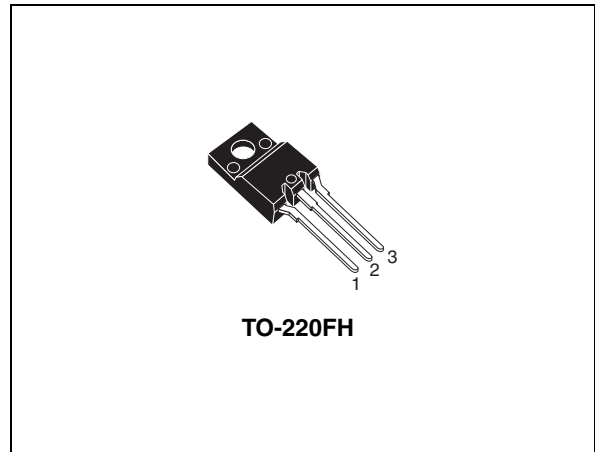
STFV4N150

N-channel 1500V - 5Ω - 4A - TO-220FH
Very high voltage PowerMESH™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STFV4N150	1500V	<7Ω	4A	40W

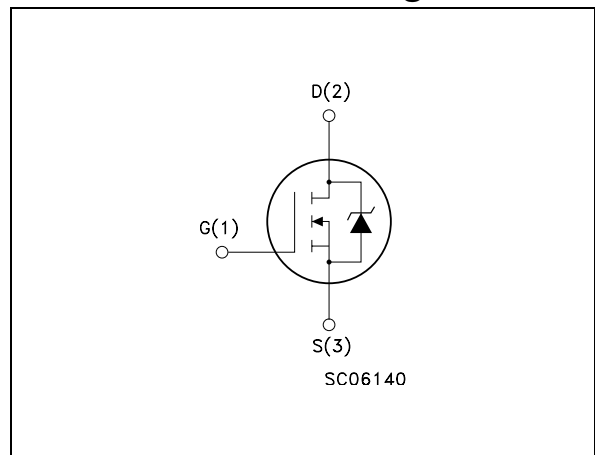
- Avalanche ruggedness
- Gate charge minimized
- Very low intrinsic capacitances
- High speed switching
- Fully plastic TO-220 package
- Creepage distance path is > 4mm



Description

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, unrivalled gate charge and switching characteristics. The creepage path is what makes this package unique from TO-220FP. The creepage distance path between each lead and between the leads and the heatsink has been increased to >4.0mm, making this package met all stringent safety norms in high voltage applications.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STFV4N150	FV4N150	TO-220FH	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	1500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	1500	V
V_{GS}	Gate- source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	12	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	40	W
	Derating factor	0.32	W/ $^\circ\text{C}$
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{s}$; $T_C=25^\circ\text{C}$)	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Limited only by maximum temperature allowed

2. Pulse width limited by safe operating area

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	3.12	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	350	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	1500			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			10 500	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 30\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 2\text{A}$		5	7	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 30\text{V}$, $I_D = 2\text{A}$		3.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		1300 120 12		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 600\text{V}$, $I_D = 4\text{A}$, $V_{GS} = 10\text{V}$ (see Figure 15)		30 10 9	50	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 750V$, $I_D = 2A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 14)		35		ns
t_r	Rise time			30		ns
$t_{d(off)}$	Turn-off-delay time			45		ns
t_f	Fall time			45		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4A$, $V_{GS} = 0$			2	V
t_{rr}	Reverse recovery time	$I_{SD} = 4A$, $di/dt = 100A/\mu s$ $V_{DD} = 45V$ (see Figure 19)		510		ns
Q_{rr}	Reverse recovery charge			3		μC
I_{RRM}	Reverse recovery current			12		A
t_{rr}	Reverse recovery time	$I_{SD} = 4A$, $di/dt = 100A/\mu s$ $V_{DD} = 45V$, $T_j = 150^\circ C$ (see Figure 19)		650		ns
Q_{rr}	Reverse recovery charge			4		μC
I_{RRM}	Reverse recovery current			12.6		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

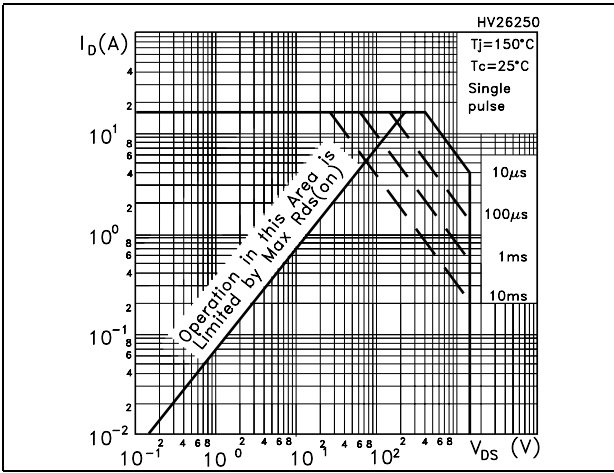


Figure 2. Thermal impedance

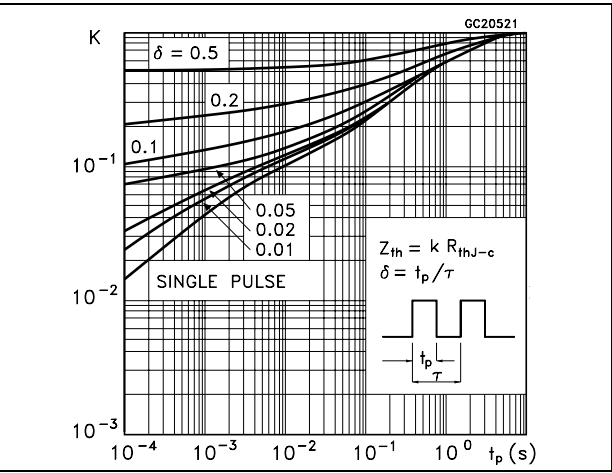


Figure 3. Output characteristics

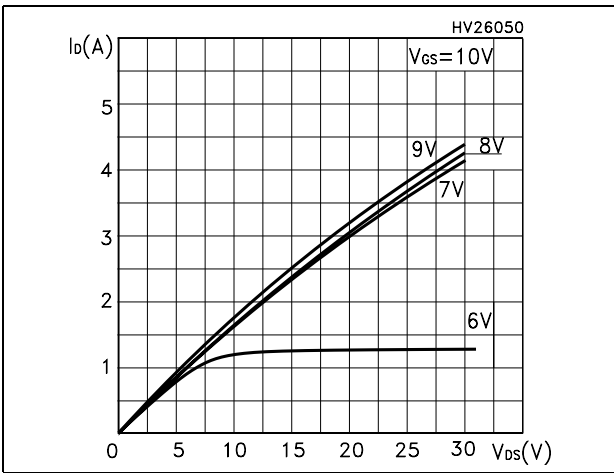


Figure 4. Transfer characteristics

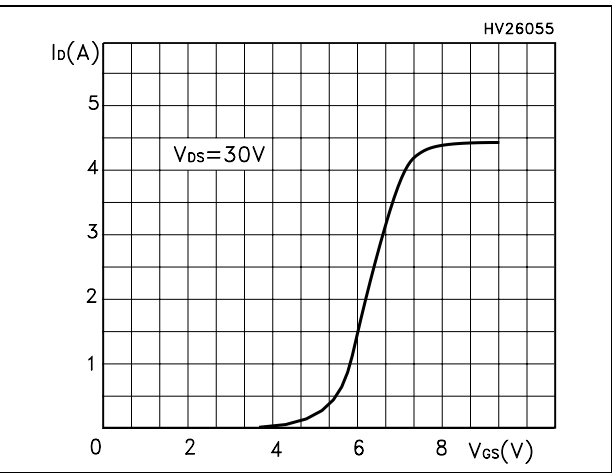


Figure 5. Transconductance

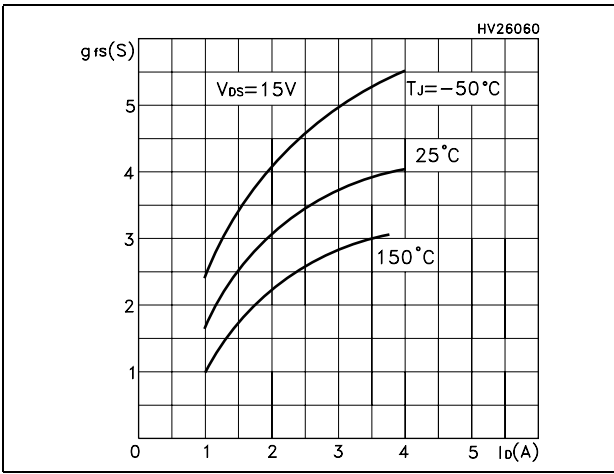


Figure 6. Static drain-source on resistance

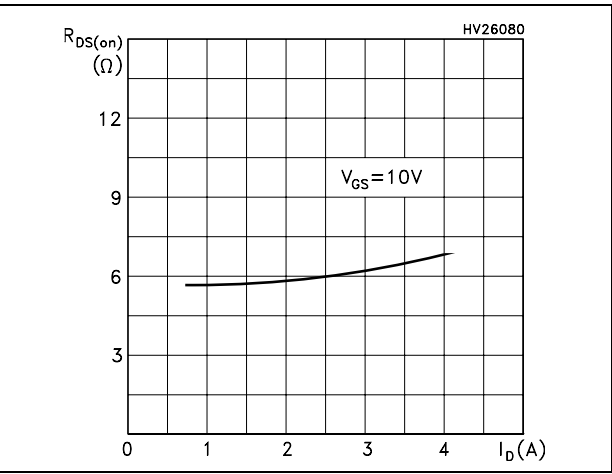


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

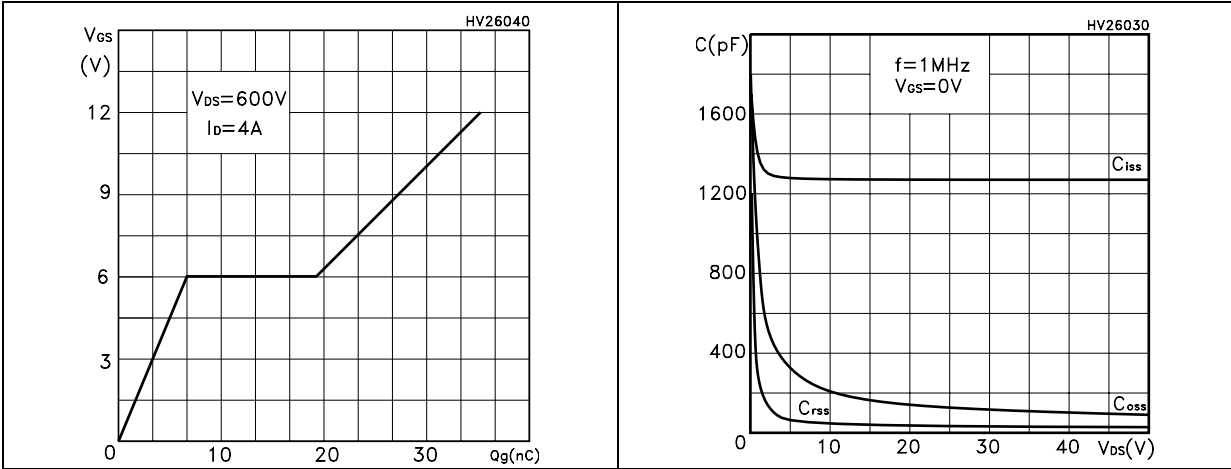


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

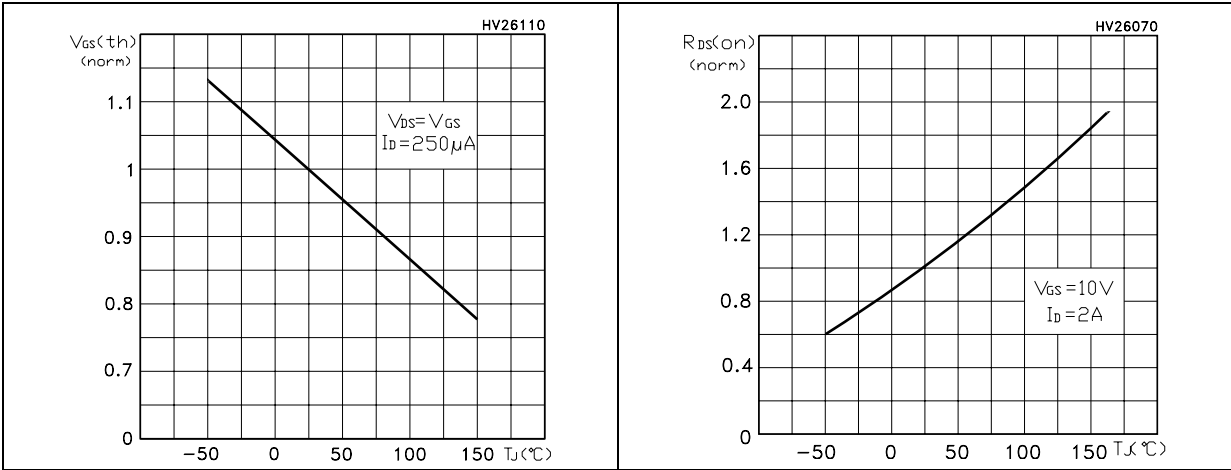


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized $B_{V_{DS}}$ vs temperature

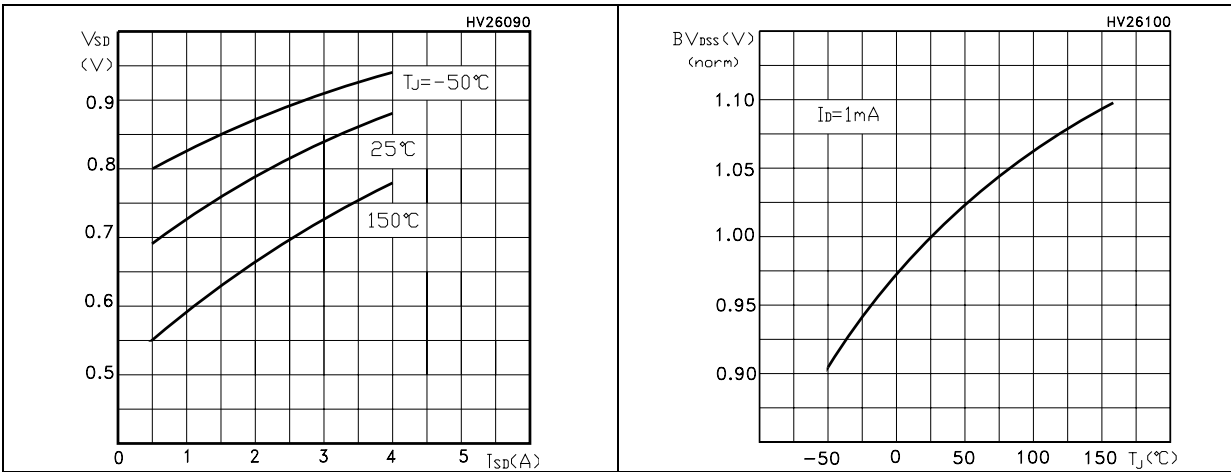
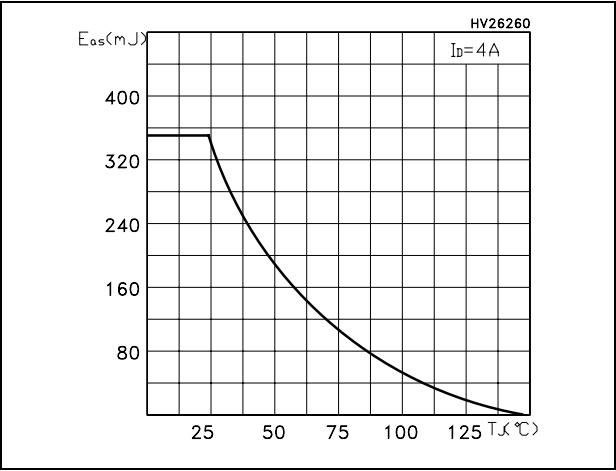


Figure 13. Maximum avalanche energy vs temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load

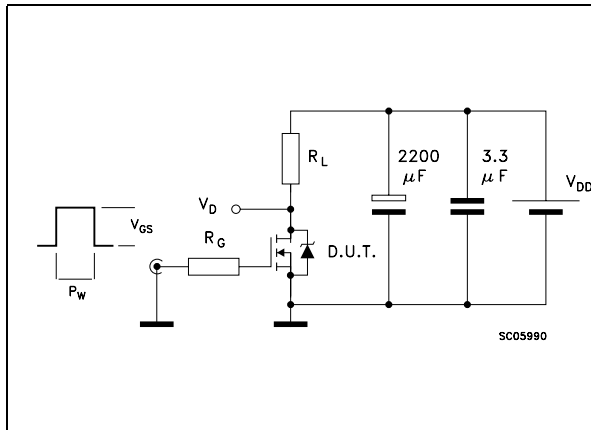


Figure 15. Gate charge test circuit

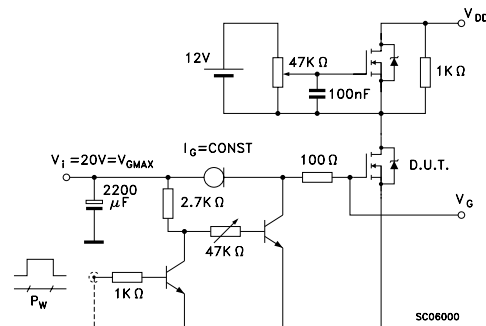


Figure 16. Test circuit for inductive load switching and diode recovery times

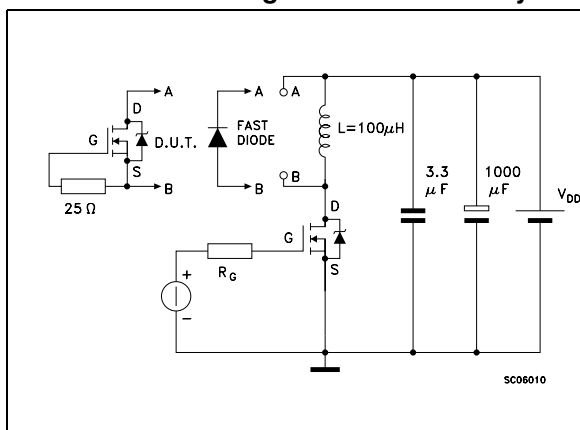


Figure 17. Unclamped inductive load test circuit

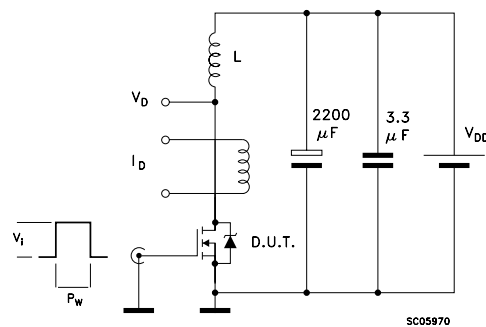


Figure 18. Unclamped inductive waveform

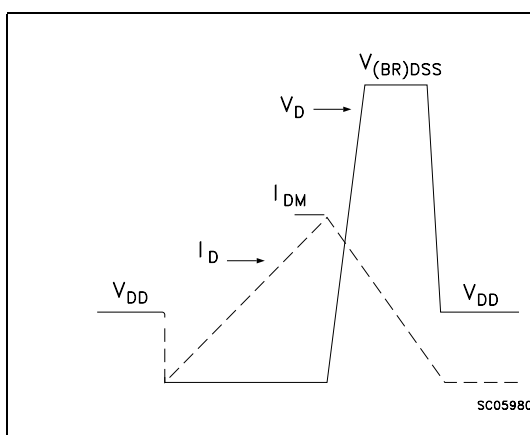
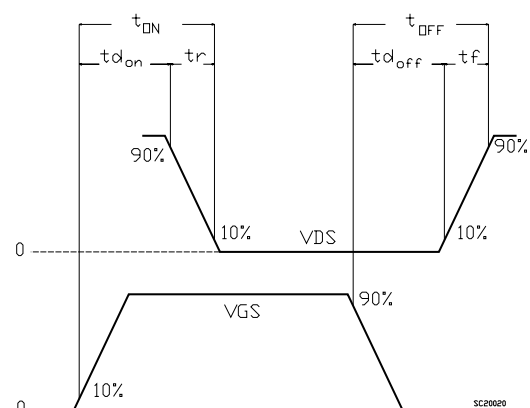


Figure 19. Switching time waveform

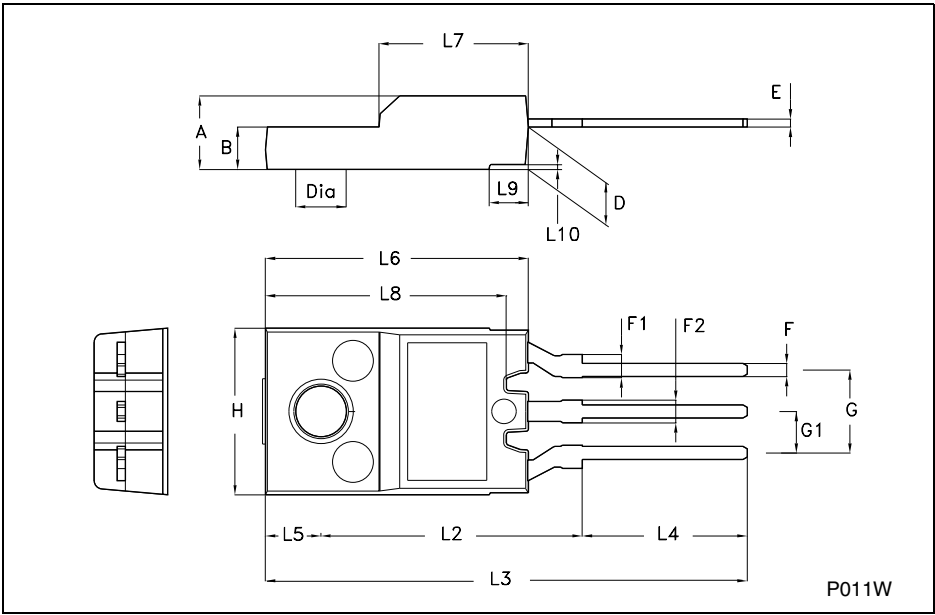


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220FH (Fully plastic High voltage) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.3		1.8	0.051		0.070
F2	1.3		1.8	0.051		0.070
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L5		3.4			0.134	
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
L8	14.5		15	0.570		0.590
L9		2.4			0.094	



5 Revision history

Table 8. Revision history

Date	Revision	Changes
07-Jul-2005	1	First Release
06-Jun-2006	2	New template, inerted new value on <i>Absolute maximum ratings</i>
28-Jun-2006	3	The document has been reformatted
06-Mar-2007	4	Typo mistake on page 1

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