TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type

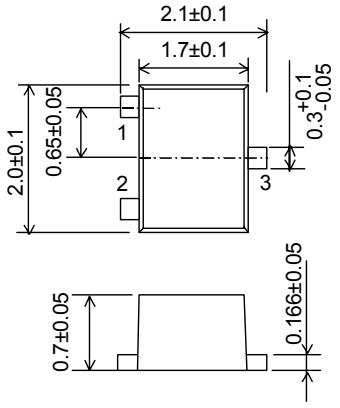
# SSM3K104TU

Power Management Switch Applications

High-Speed Switching Applications

- 1.8 V drive
- Low ON-resistance: $R_{on}$ = 110 mΩ (max) (@$V_{GS}$ = 1.8 V)
  $R_{on}$ = 74 mΩ (max) (@$V_{GS}$ = 2.5 V)
  $R_{on}$ = 56 mΩ (max) (@$V_{GS}$ = 4.0 V)
- Lead (Pb)-free

Unit: mm




1 : Gate
2 : Source
3 : Drain

UFM

| | |
|---|---|
| JEDEC | ― |
| JEITA | ― |
| TOSHIBA | 2-2U1A |

Weight: 6.6 mg (typ.)

## Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-Source voltage | | $V_{DS}$ | 20 | V |
| Gate-Source voltage | | $V_{GSS}$ | ± 12 | V |
| Drain current | DC | $I_D$ | 3.0 | A |
| | Pulse | $I_{DP}$ | 6.0 | |
| Drain power dissipation | | $P_{D\ (Note\ 1)}$ | 800 | mW |
| | | $P_{D\ (Note\ 2)}$ | 500 | |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55~150 | °C |

Note 1: Mounted on a ceramic board.
(25.4 mm × 25.4 mm × 0.8 t, Cu Pad: 645 $mm^2$ )
Note 2: Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 $mm^2$ )

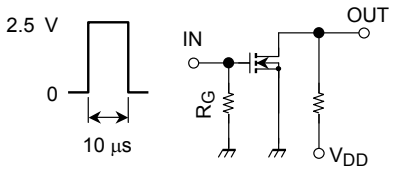
## Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Drain-Source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 1 mA, $V_{GS}$ = 0 | 20 | ― | ― | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = 1 mA, $V_{GS}$ = −12 V | 12 | ― | ― | |
| Drain cutoff current | | $I_{DSS}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 | ― | ― | 1 | μA |
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±12 V, $V_{DS}$ = 0 | ― | ― | ±1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 3 V, $I_D$ = 1 mA | 0.4 | ― | 1.0 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 3 V, $I_D$ = 2.0 A (Note 3) | 6 | 10 | ― | S |
| Drain-Source ON-resistance | | $R_{DS\ (ON)}$ | $I_D$ = 2.0 A, $V_{GS}$ = 4.0 V (Note 3) | ― | 44 | 56 | mΩ |
| | | | $I_D$ = 1.0 A, $V_{GS}$ = 2.5 V (Note 3) | ― | 53 | 74 | |
| | | | $I_D$ = 0.5 A, $V_{GS}$ = 1.8 V (Note 3) | ― | 70 | 110 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | ― | 320 | ― | pF |
| Output capacitance | | $C_{oss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | ― | 62 | ― | pF |
| Reverse transfer capacitance | | $C_{rss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | ― | 51 | ― | pF |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = 10 V, $I_D$ = 2 A, | ― | 18 | ― | ns |
| | Turn-off time | $t_{off}$ | $V_{GS}$ = 0~2.5 V, $R_G$ = 4.7 Ω | ― | 14 | ― | |
| Drain-Source forward voltage | | $V_{DSF}$ | $I_D$ = −3.0 A, $V_{GS}$ = 0 V (Note 3) | ― | −0.85 | −1.2 | V |

Note 3: Pulse test

## Switching Time Test Circuit

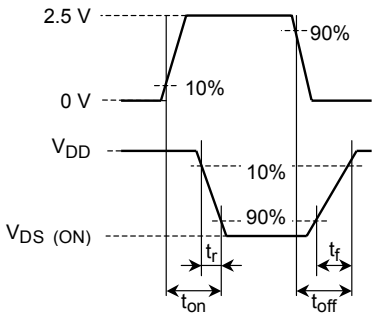
### (a) Test Circuit



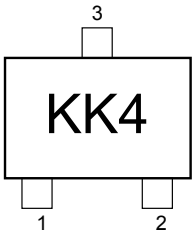

$V_{DD}$ = 10 V
$R_G$ = 4.7 Ω
D.U. ≦ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
Common Source
Ta = 25°C

### (b) $V_{IN}$

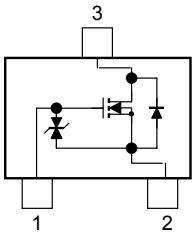
### (c) $V_{OUT}$




## Marking




## Equivalent Circuit (top view)




## Notice on Usage

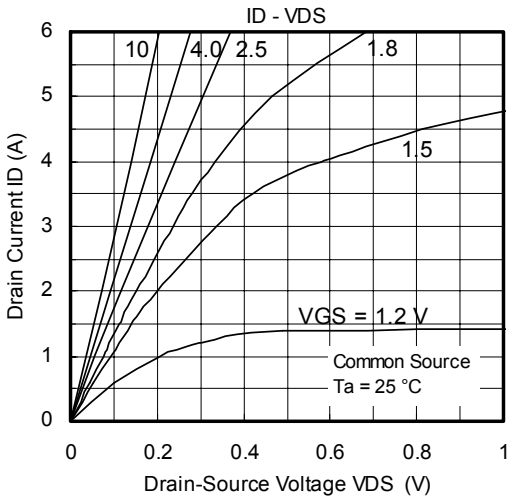
$V_{th}$ can be expressed as the voltage between gate and source when the low operating current value is $I_D$ = 1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than $V_{th}$, and $V_{GS\ (off)}$ requires a lower voltage than $V_{th}$. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

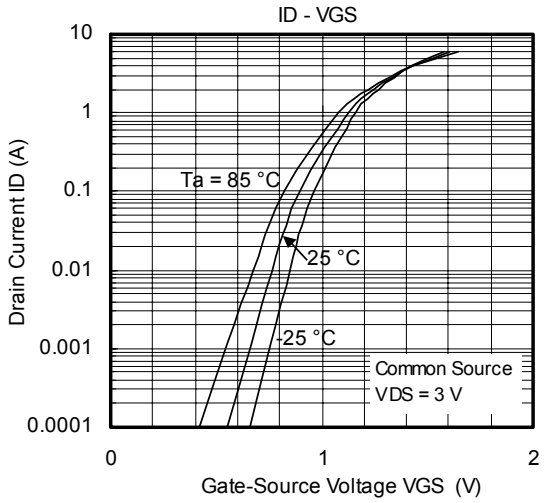
Take this into consideration when using the device.

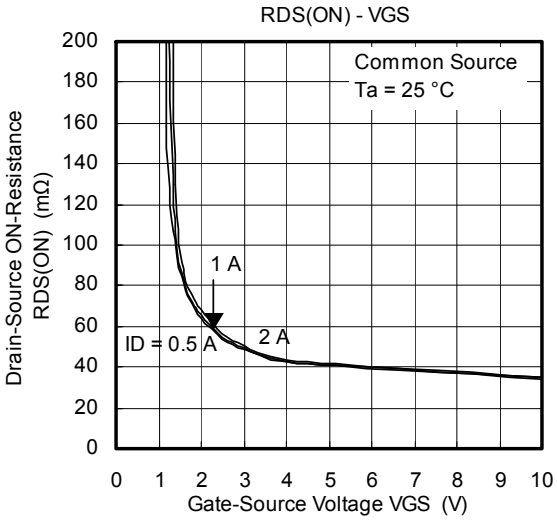
The recommended $V_{GS}$ voltage for turning on this product is 1.8 V or higher.

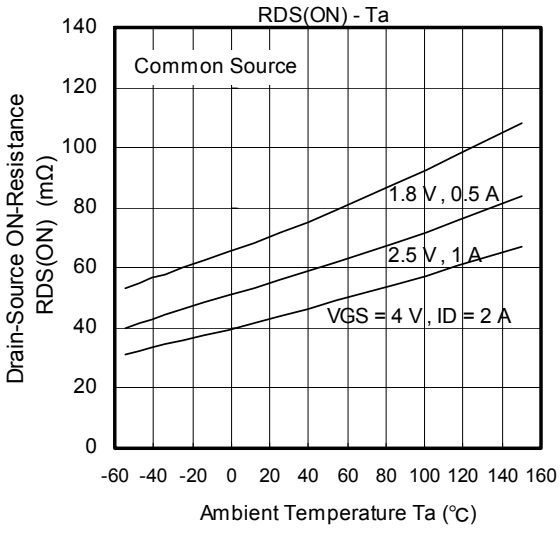
## Handling Precaution

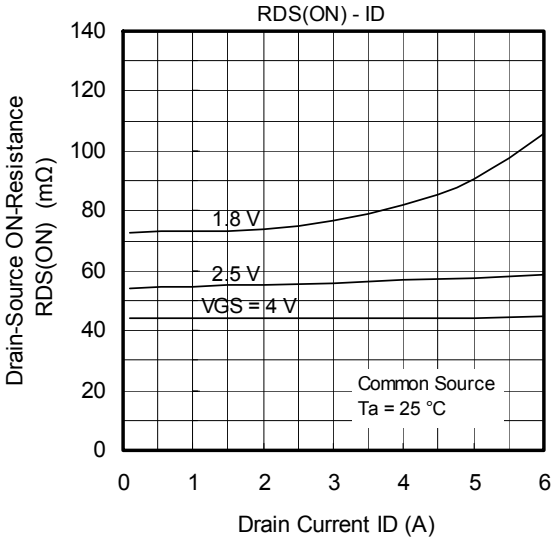
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

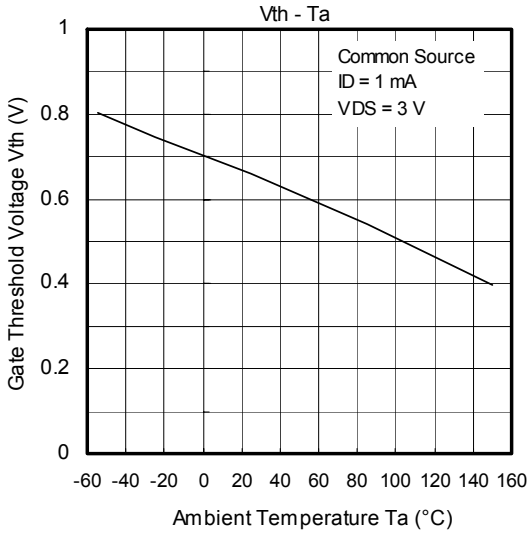

ID - VDS
10
4.0
2.5
1.8
1.5
VGS = 1.2 V
Common Source
Ta = 25 °C
Drain Current ID (A)
Drain-Source Voltage VDS (V)

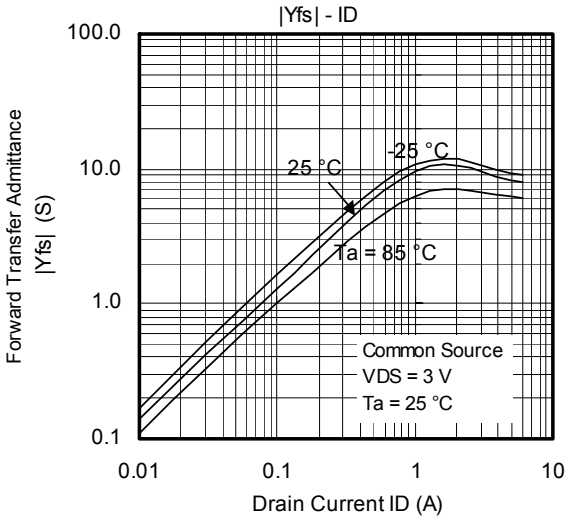

ID - VGS
Ta = 85 °C
25 °C
25 °C
Common Source
VDS = 3 V
Drain Current ID (A)
Gate-Source Voltage VGS (V)

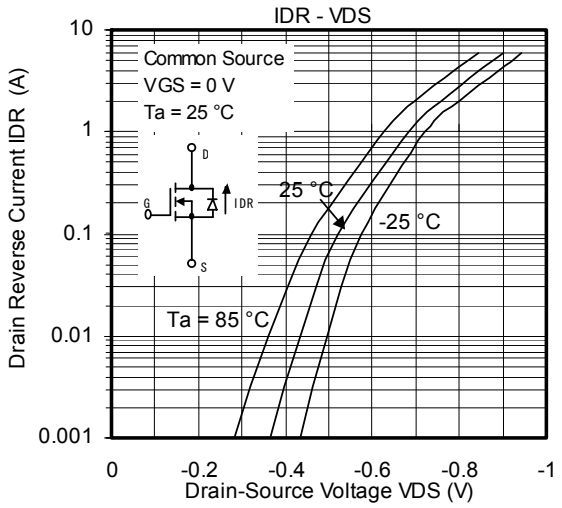

RDS(ON) - VGS
Common Source
Ta = 25 °C
1 A
2 A
ID = 0.5 A
Drain-Source ON-Resistance RDS(ON) (mΩ)
Gate-Source Voltage VGS (V)

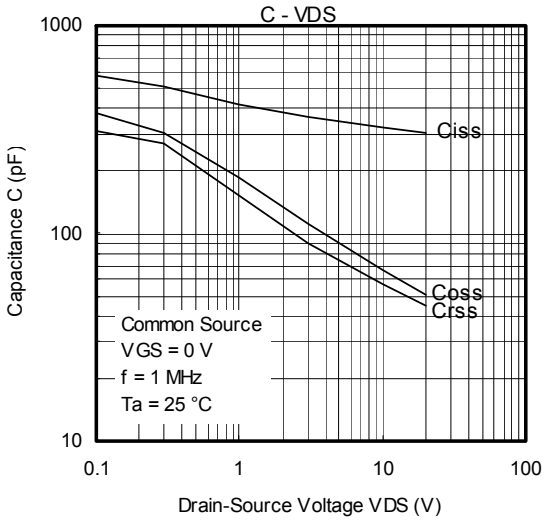

RDS(ON) - Ta
Common Source
1.8 V , 0.5 A
2.5 V , 1 A
VGS = 4 V , ID = 2 A
Drain-Source ON-Resistance RDS(ON) (mΩ)
Ambient Temperature Ta (°C)

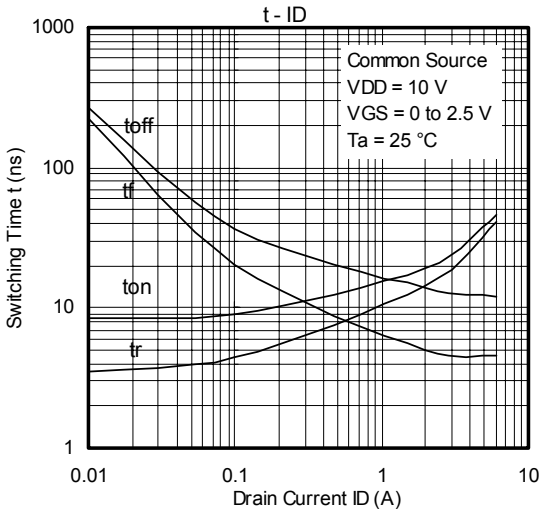

RDS(ON) - ID
1.8 V
2.5 V
VGS = 4 V
Common Source
Ta = 25 °C
Drain-Source ON-Resistance RDS(ON) (mΩ)
Drain Current ID (A)

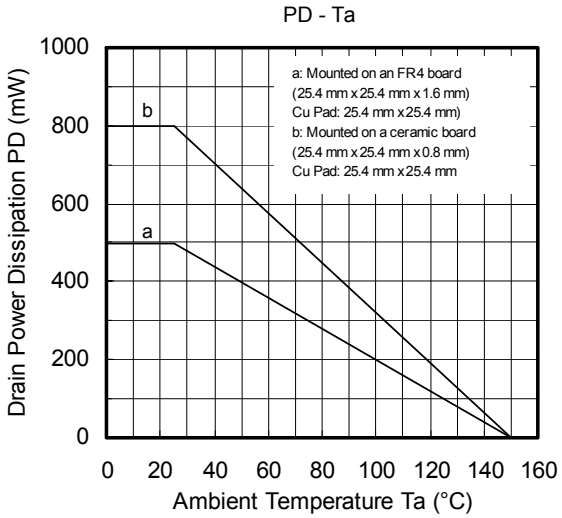

Vth - Ta
Common Source
ID = 1 mA
VDS = 3 V
Gate Threshold Voltage Vth (V)
Ambient Temperature Ta (°C)

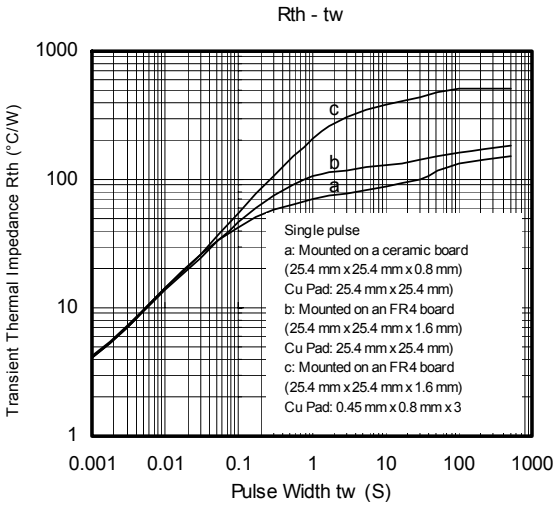

|Yfs| - ID
Forward Transfer Admittance |Yfs| (S)
Drain Current ID (A)
100.0
10.0
1.0
0.1
0.01
0.1
1
10
25 °C
-25 °C
Ta = 85 °C
Common Source
VDS = 3 V
Ta = 25 °C


IDR - VDS
Drain Reverse Current IDR (A)
Drain-Source Voltage VDS (V)
10
1
0.1
0.01
0.001
0
-0.2
-0.4
-0.6
-0.8
-1
Common Source
VGS = 0 V
Ta = 25 °C
25 °C
-25 °C
Ta = 85 °C
D
G
S
IDR


C - VDS
Capacitance C (pF)
Drain-Source Voltage VDS (V)
1000
100
10
0.1
1
10
100
Ciss
Coss
Crss
Common Source
VGS = 0 V
f = 1 MHz
Ta = 25 °C


t - ID
Switching Time t (ns)
Drain Current ID (A)
1000
100
10
1
0.01
0.1
1
10
Common Source
VDD = 10 V
VGS = 0 to 2.5 V
Ta = 25 °C
toff
tf
ton
tr


PD - Ta
Drain Power Dissipation PD (mW)
Ambient Temperature Ta (°C)
1000
800
600
400
200
0
0
20
40
60
80
100
120
140
160
a: Mounted on an FR4 board
(25.4 mm x 25.4 mm x 1.6 mm)
Cu Pad: 25.4 mm x 25.4 mm)
b: Mounted on a ceramic board
(25.4 mm x 25.4 mm x 0.8 mm)
Cu Pad: 25.4 mm x 25.4 mm
b
a


Rth - tw
Transient Thermal Impedance Rth (°C/W)
Pulse Width tw (S)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
c
b
a
Single pulse
a: Mounted on a ceramic board
(25.4 mm x 25.4 mm x 0.8 mm)
Cu Pad: 25.4 mm x 25.4 mm)
b: Mounted on an FR4 board
(25.4 mm x 25.4 mm x 1.6 mm)
Cu Pad: 25.4 mm x 25.4 mm)
c: Mounted on an FR4 board
(25.4 mm x 25.4 mm x 1.6 mm)
Cu Pad: 0.45 mm x 0.8 mm x 3

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