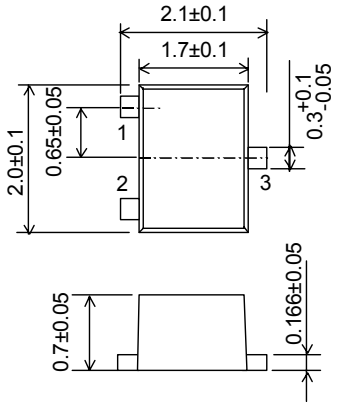
TOSHIBA Field Effect Transistor Silicon P-Channel MOS Type

SSM3J113TU

High Speed Switching Applications

- 2.0V drive
- Low on-resistance: R_{on} = 449mΩ (max) (@V_{GS} = −2.0 V)
  R_{on} = 249mΩ (max) (@V_{GS} = −2.5 V)
  R_{on} = 169mΩ (max) (@V_{GS} = −4.0 V)
- Lead(Pb)-free

Unit: mm



1 :Gate
2 :Source
3 :Drain

UFM

JEDEC	―
JEITA	―
TOSHIBA	2-2U1A

Weight: 6.6 mg (typ.)

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	−20	V
Gate-Source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	−1.7	A
	Pulse	I_{DP}	−3.4	
Drain power dissipation		$P_{D\ (Note1)}$	800	mW
		$P_{D\ (Note2)}$	500	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note1: Mounted on ceramic board.
(25.4 mm × 25.4 mm × 0.8 mm, Cu Pad: 645 mm^2)
Note2: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

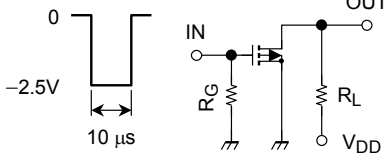
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−20	―	―	V
		$V_{(BR)\ DSX}$	I_D = −1 mA, V_{GS} = +12V	−8	―	―	
Drain cut-off current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0	―	―	−1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±12V, V_{DS} = 0	―	―	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −0.1 mA	−0.5	―	−1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = − 0.65 A (Note3)	1.3	2.7	―	S
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = −0.65 A, V_{GS} = −4.0 V (Note3)	―	129	169	mΩ
			I_D = −0.65 A, V_{GS} = −2.5 V (Note3)	―	189	249	
			I_D = −0.65 A, V_{GS} = −2.0 V (Note3)	―	249	449	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	―	370	―	pF
Output capacitance		C_{oss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	―	116	―	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	―	73	―	pF
Switching time	Turn-on time	t_{on}	V_{DD} = −10 V, I_D = −0.65 A,	―	33	―	ns
	Turn-off time	t_{off}	V_{GS} = 0~−2.5 V, R_G = 4.7 Ω	―	47	―	
Drain-Source forward voltage		V_{DSF}	I_D = 1.7 A, V_{GS} = 0 V (Note3)	―	0.77	1.2	V

Note3: Pulse test

Switching Time Test Circuit

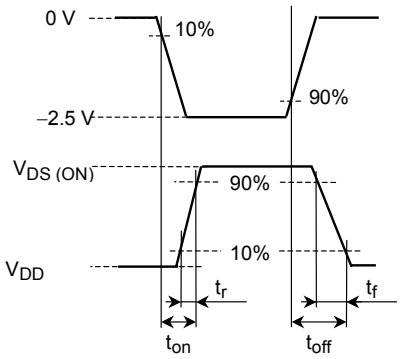
(a) Test circuit



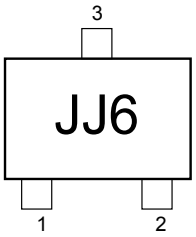
V_{DD} = -10 V
R_G = 4.7 Ω
D.U. ≦ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

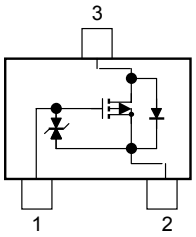
(c) V_{OUT}



Marking



Equivalent Circuit (top view)



Precaution

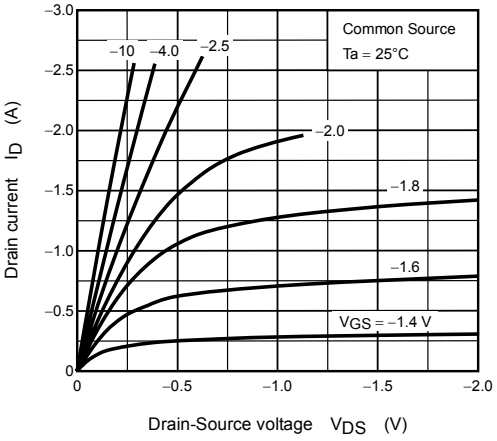
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D=−0.1mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th}, and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\ (off)}$ < V_{th} < $V_{GS\ (on)}$)
Take this into consideration when using the device.
The recommended V_{GS} voltage for turning on this product is −2 V or higher.

Handling Precaution

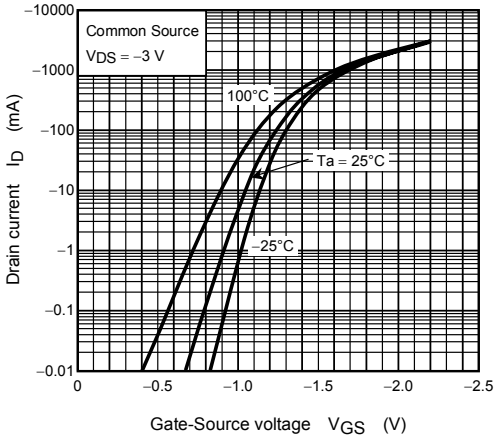
When handling individual devices which are not yet mounted on a circuit board, be sure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

+

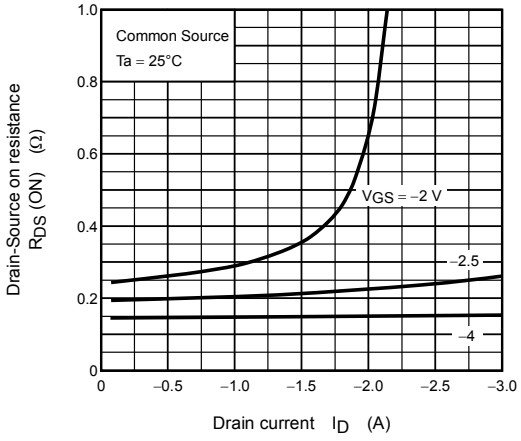
$I_D - V_{DS}$



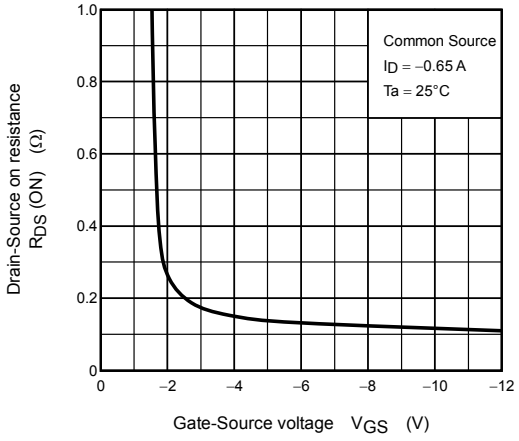
$I_D - V_{GS}$



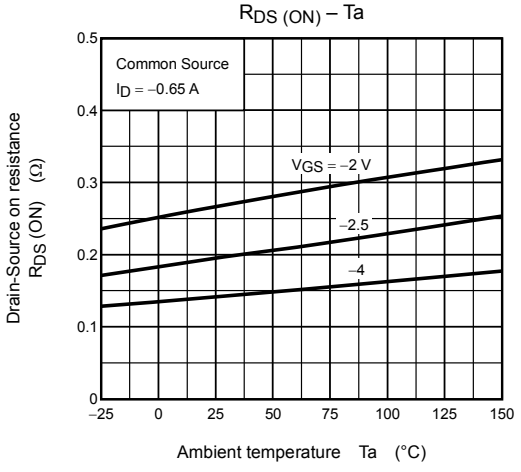
$R_{DS\ (ON)} - I_D$



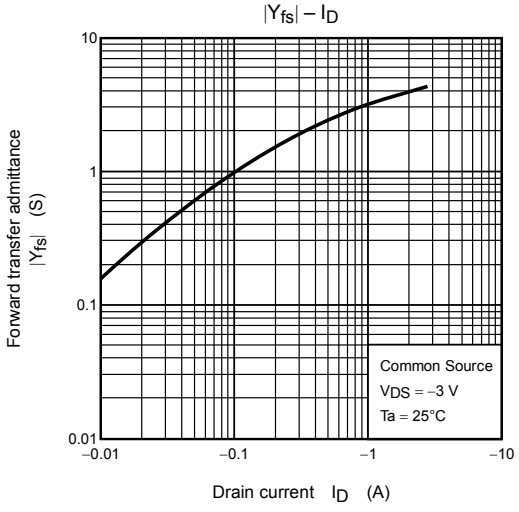
$R_{DS\ (ON)} - V_{GS}$



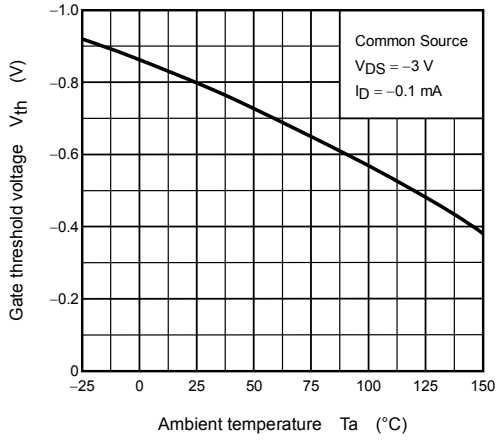
$R_{DS\ (ON)} - Ta$



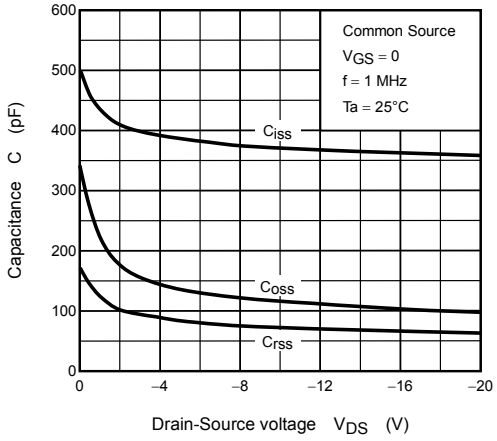
$|Y_{fs}| - I_D$



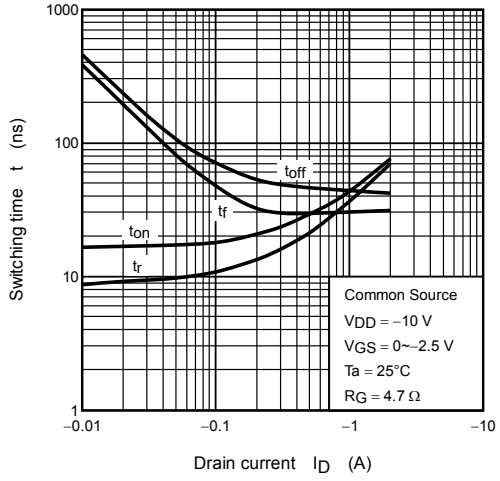
V_{th} – Ta



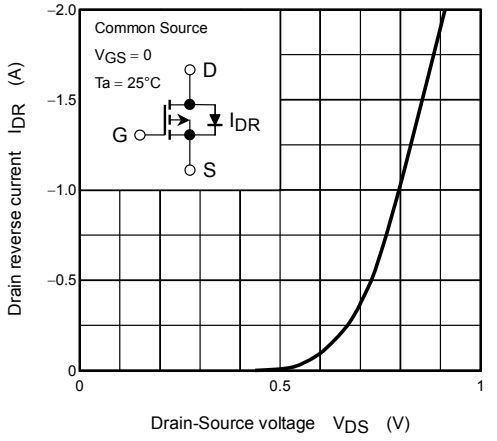
C – V_{DS}



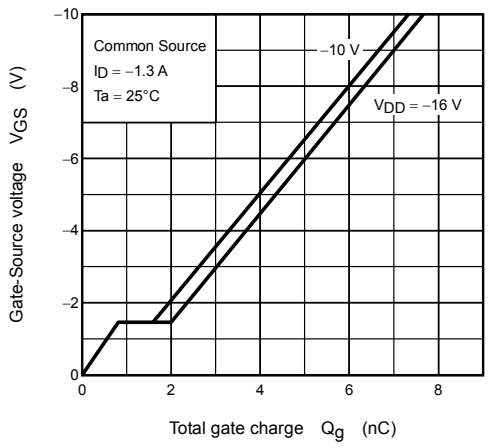
t – I_D



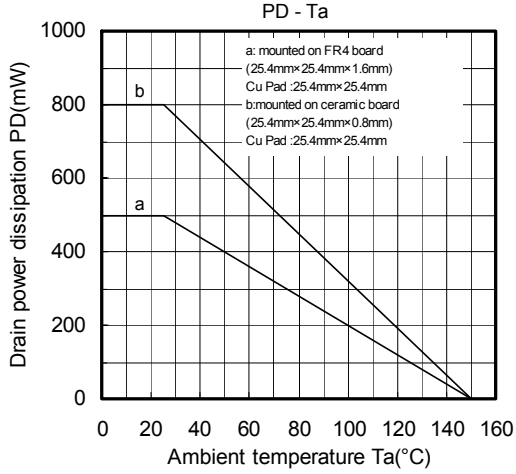
I_{DR} – V_{DS}

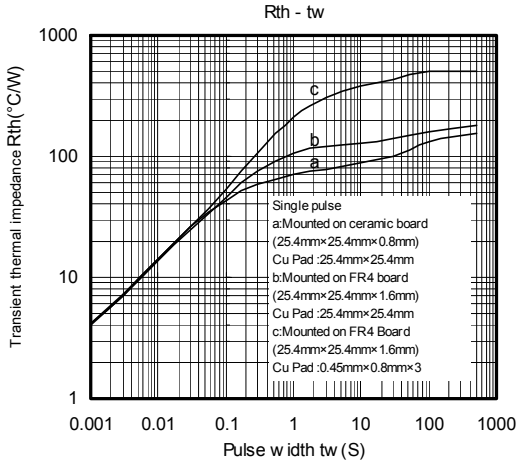


Dynamic Input Characteristic



PD - Ta




Rth - tw
Transient thermal impedance Rth(°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse w idth tw (S)
c
b
a
Single pulse
a:Mounted on ceramic board
(25.4mm×25.4mm×0.8mm)
Cu Pad :25.4mm×25.4mm
b:Mounted on FR4 board
(25.4mm×25.4mm×1.6mm)
Cu Pad :25.4mm×25.4mm
c:Mounted on FR4 Board
(25.4mm×25.4mm×1.6mm)
Cu Pad :0.45mm×0.8mm×3

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