PCI Express GenII 1:19 Geared Differential Buffer -18 and 1 Outputs

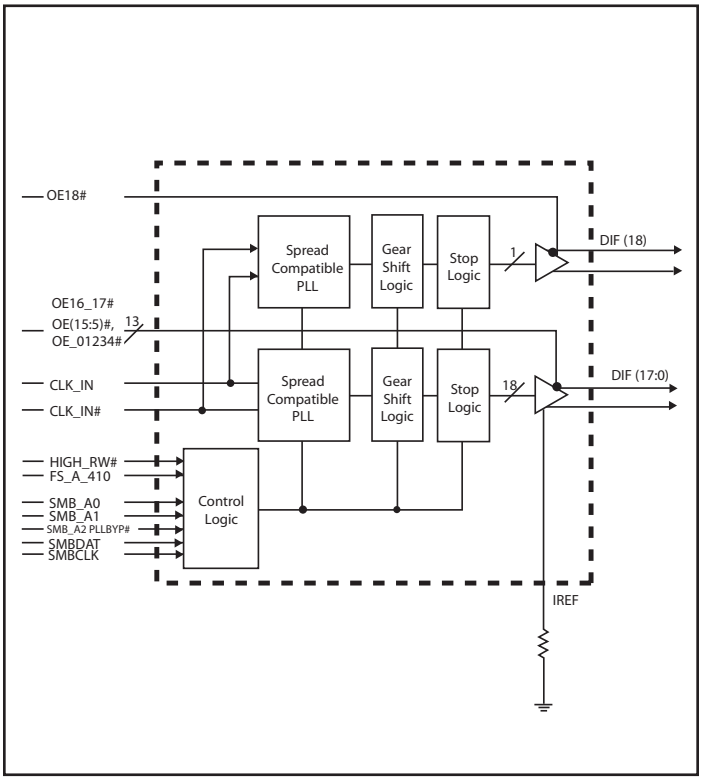
Features

- Phase jitter filter for PCIe GenII application
- Nineteen Pairs of differential HCSL buffers
  -18 and 1 outputs
- Low skew < 100ps within Dif (16:0) group
- Low phase jitter < 108ps (PLL mode)
- Output Enable (OE) pins for all outputs
- Outputs tristate control via SMBus
- Power Management Control
- Programmable PLL Bandwidth
- PLL or PLL Bypass (Fanout) mode
- Gear Ratios for different input to output frequencies
  - Input: 100, 133, 166, 200, 266, 333, or 400 MHz
  - Output: 100, 133, 166 or 200 MHz
- 3.3V Operation
- Packaging (Pb-Free and Green):
  —72-pin TQFN (ZD)

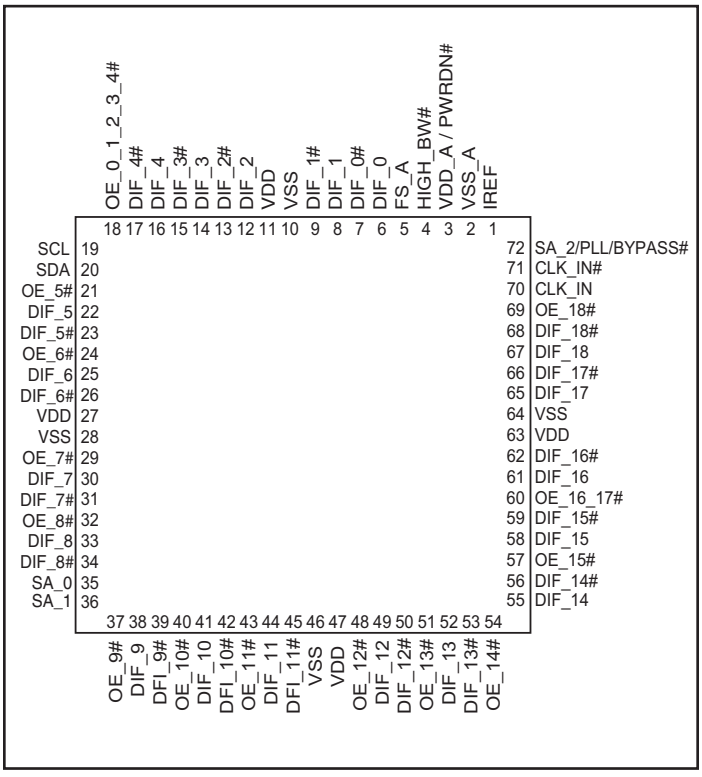
Description

PI6C21900S is a PCI Express Gen-II complient, high-speed, low-noise PCI-Express and FBDIMM differential clock buffer designed to be a companion to the workstation/server clock synthesizer such as PI6C410B. The device distributes nineteen copies of the differential SRC clock, such as the one sourced from PI6C410B. To adapt to different systems and to offer various performance platforms, the PI6C21900S outputs can be programmed to different frequency. The output frequency ratio can be modified to offer various derivative frequency from the input frequency. Most of the output pair is controlled by individual OE pin. Some OE# pins service multiple differential output pairs. The clock outputs are controlled by the input selection bits: SA_0, SA_1, SA_2 through external select pins or via SMBus, using SCL (SMBus Clock) and SDA (SMBus Data) pins.

Block Diagram



Pinout Configuration



Pin Description

Pin Name	Type	Pin #	Description
CLK_IN, CLK_IN#	I, DIF	70,71	0.7V Differential input (eg. from PI6C410B clock synthesizer)
DIF & DIF# [16:5]	O, DIF	22,23,25,26,30,31,33,34, 38,39,41,42,44,45,49,50, 52,53,55,56,58,59,61,62	0.7V Differential clock outputs, geared to the a ratio of the input clock.
DIF & DIF# [18:17]	O, DIF	65,66,67,68	0.7V Differential clock outputs, which can be configured to be 1:1 instead of geared. Default is geared same as 0-16 outputs.
DIF & DIF# [4:0]	O, DIF	6,7,8,9,12,13, 14,15,16,17	0.7V Differential clock outputs, geared to the a ratio of the input clock.
OE#_[15:5]	I, SE	21,24,29,32,37,40,43,48, 51,54,57	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
OE_16_17#	I, SE	60	3.3V LVTTL active low input for enabling differential outputs. The pin controls both DIF_16 and DIF_17 pairs. Individual disables are available via SMBus.
OE_18#	I, SE	69	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
OE_0_1_2_3_4#	I, SE	18	3.3V LVTTL active low input for enabling differential outputs. The pin controls both DIF_0 through DIF_4 pairs. Individual disables are available via SMBus.
HIGH_BW#	I, SE	4	3.3V LVTTL input for selecting the PLL bandwidth (high = low BW)
SCL	I, SE	19	SMBus slave clock input
SDA	I/O, OC	20	Open collector SMBus data
IREF	I	1	A precision resistor is attached to this pin to set the differential output current. Default is 475Ω
SA_[0:1]	I	35,36	3.3V LVTTL input selecting the address for SMBus address
SA_2/PLL_BYPASS#	I	72	3.3V LVTTL input for PLLbypass and SMBus address
FS_A	I	5	GTL level input to establish a high(>=200 MHz) or low frequency (<200 MHz) range. This is a low-voltage threshold input. Please see the VIL_FS and VIH_FS specifications.
VDD_A / PWRDN#	3.3V	3	3.3V Power Supply for PLL / Input to power down the device. When this input is low, outputs are hi-Z and PLL off.
VSS_A	GND	2	Ground for PLL
VSS	I	10,28,46,64	Ground for outputs
VDD	3.3V	11,27,47,63	3.3 V power supply for outputs

Signals and Features Description

Gear Ratio

Gear ratio defines the relationship between input to output frequency. The input frequencies are normally 100.00, 133.33, 166.67, 200.00, 266.67, 333.33 and 400.00 MHz. The outputs are also range between 100 to 400 MHz. Gear ratio gives the flexibility to select the desired output frequency based on the input frequency. Gear Ratio is programmable througn the SMBus interface and FS_A pin. FS_A pin informs the PI6C21900 about the input frequency range. FS_A = 1 indicates input frequency between 100.0 MHz and 166.67 MHz. FS_A = 0 indicates input frequency range of 200.00 MHz to 400 MHz.

Table 1. DB 1900 G Programmable Gear Ratio Table

Case	FS_A	SMBus 3	SMBus 2	SMBus 1	SMBus 0	Input (M)	Output (N)	Gear Ratio (N/M)	Input/Output Frequencies (MHs)				
									200.0	266.7	320.0	333.3	400.0
1	0	0	0	0	0	3	1	0.333					**133.3**
2	0	0	0	0	1	5	2	0.400				**133.3**	**160.0**
3	0	0	0	1	0	12	5	0.417					**167.7**
4	0	0	0	1	1	2	1	0.500	**100.0**	**133.3**		**166.7**	**200.0**
5	0	0	1	0	0	5	3	0.600				**200.0**	
6	0	0	1	0	1	8	5	0.625		**166.7**			
7	0	0	1	1	0	3	2	0.667	**133.3**				**266.7**
8	0	0	1	1	1	4	3	0.750		**200.0**			
9	0	1	0	0	0	6	5	0.833	**1.677**				**333.3**
10	0	1	0	0	1	1	1	1.000	**200.0**	**266.7**	**320.0**	**333.3**	**400.0**
11	0	1	0	0	1	4	5	1.250		**333.3**			
12	0	1	1	0	0	3	4	1.333	**266.7**				
13	0	1	1	1	0	3	5	1.667	**333.3**				
14	0	1	1	1	1	1	2	2.000	**400.0**				
									Input/Output Frequencies (MHs)				
									100.0	133.3	160.0	166.7	
15	1	0	1	1	1	5	4	0.800				**133.3**	
16	1	1	0	0	1	1	1	1.000	**100.0**	**133.3**	**160.0**	**166.7**	
17	1	1	0	1	0	5	6	1.200				**200.0**	
18	1	1	0	1	1	4	5	1.250		**166.7**			
19	1	1	1	0	1	2	3	1.500		**200.0**			
20	1	1	1	1	1	1	2	2.000		**266.7**	**320.0**		

Note: Shaded lines are Power-up defaults for FS_A=0 and 1 repectively. Output frequency numbers in **BOLD** are valid operating frequencies.

Default conditions

Default conditions are defined in conjunction with the power up sequence to ensure system operation sufficient to configure the timing parameters of the system. Default conditions have also been defined to account for the typical use of component to support platform debug or analysis.

Outputs are enabled as a default. To prevent over drive of high speed input clock configurations, explicit system control of pin level output enables are recommended. General purpose I/O gates or controls can be used to gate the output via pin level OE numbers. One can then use system controls to program the desired gear ratio before enabling the outputs.

OE# and Output enables

Output enables are asynchronous asserted - low signals. Outputs are enabled by default. Two mechanisms exist to disable the outputs, either by pin or by programming the control registers via the SMBus.

OE Functionality Table

OE (Pin)	OE (SMBus bit)	DIFF	Diff #	Note
0	1	Normal	Normal	
1	0	Tristate	Tristate	
1	1	Tristate	Tristate	
0	0	Tristate	Tristate	

FS_A

The FS_A pin is a low-threshold latched input to the buffer to designate whether the input frequency is greater than/equal to or less than 200 MHz. The signal is consistant with the FS_A input to the main clock synthesizer.

Functionality at Power Up (PLL Mode) Table

FS_A	CLK_IN (CPU FSB) MHz	DIFF[16:0]
1	$100 \leq CLK\_IN < 200$	CLK_IN
0	$200 \leq CLK\_IN \leq 400$	CLK_IN

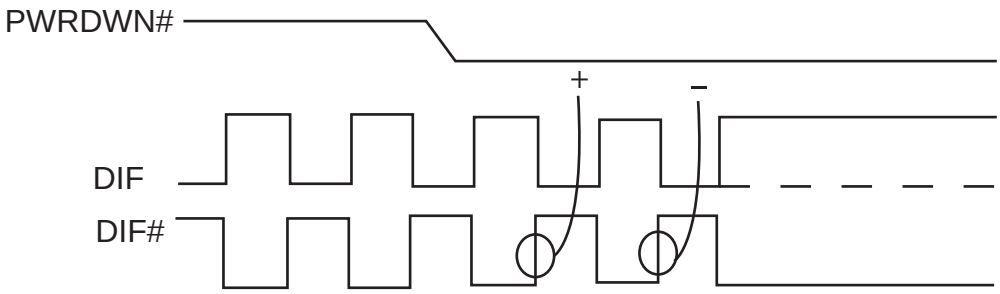
VDD_A/PWRD WN#

3.3V power for the PLL core also functions as a Power Down. Collapsing this power supply places the device in Power Down mode. Pulling the VDD_A/PWRDN# (Power Down) pin low can be used to shut off all clocks cleanly and instruct the device to evoke power savings mode.

VDD_A/PWRDWN# Functionality Table

INPUTS		OUTPUTS		PLL STATE
VDD_A	CLK_IN/CLK_IN#	DIF	DIF#	
3.3V(NCM)	Running	Running		ON
GND	X	Hi-Z		OFF

Power Down Timing Sequence (PWRDWN# - Assertion)



HIGH_BW#

The HIGH_BW# input is used to set the PLL bandwidth. This mode is intended to minimize PLL peaking when two or more buffers are cascaded by staggering device bandwidths. The default condition is in a low bandwidth mode.The PLL high bandwidth mode may be selected in two ways, via writing a '0' to SMBus register bit or by asserting the HIGH_BW# pin low. In both methods, if the SMBus register bit has been written low or the HIGH_BW# pin low or both, the device will be configured for high bandwidth operation.

HIGH_BW# Fynctionality Table

HIGH_BW# (Pin)	HIGH_BW# (SMBus bit)	PLL Operating Bandwidth	Note
0	1	High	SMBus bit defaults to '1'
1	1	Low	SMBus bit defaults to '1'
1	0	High	
0	0	High	

PLL_BYPASS#

The PLL/BYPASS# input is used to select between bpass mode (no PLL) and PLL mode. In bypass mode, the input clock is passed directly to the output. In the case of PLL mode, the input clock is passed through a PLL ot reduce high frequency jitter.The PLL_Bypass# mode may be selected in two ways, via writing a '0' to SMBus register bit or by asserting the SA_2/PLL/BYPASS# pin low or both, the device will be configurized for BY-PASS operation.

SA_[0:1], SA_2 / PLL_Bypass#

The SA pins define the SM_Bus address to which the device is to respond. Multiple addresses are required to support multiple clock devices especially for large system configurations. The SA_2 pin shares functionality with PLL_bypass# mode setting.
The SA pins select up to 8 unique logical clocking device addresses within an SMBus chain. Accounting for the fixed addresses already used by the synthesizer and PI6C401B, this leaves 6 address available for PI6C21900 devices on the same SMBus chain.

PI6C21900 SMBus Address Selection Table

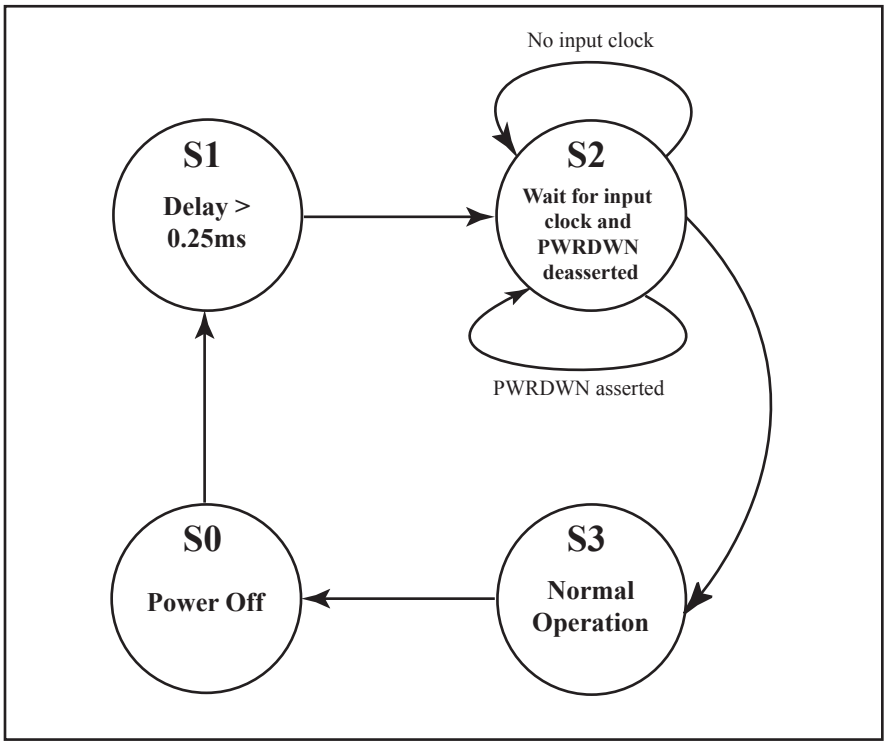
SA_[2:0]	Address	PLL Operating Mode	Note
000	D0	BYPASS (non-PLL)	
001	D2	BYPASS (non-PLL)	Address of Main Clock Synthesizer
010	D4	BYPASS (non-PLL)	
011	D6	BYPASS (non-PLL)	
100	D8	PLL	
101	DA	PLL	
110	DC	PLL	Address of PI6C410B
111	DE	PLL	

Power Up State Diagram

State#	State Name	Description	Notes
S0	Off State	3.3V power to PI6C21900S is OFF	
S1	Power Up Delay	After 3.3V supply voltage is higher than 1.8V, then the device enters state-1, and starts 0.2 ~ 0.3 ms delay	
S2	Pending Valid Clock	Device is waiting for valid clock input	2
S3	Normal Operation		1

Notes:

1. Power up latency is 1.8ms from valid input clock detected to outputs active
2. Prior to enabling output clocks, ensure **all** the conditions are met: (i) power is valid and stable, (ii) PWRDWN is deasserted, (iii) valid input clock detected, and (iv) PLL is locked and stable. Otherwise, the outputs must remain disabled.



SA_[0:1] and SA_2/PLL_BYPASS# pins

SA_[0:2] are used for setting the SMBus address. In some systems there maybe a few similar SMBus devices, to avoid contention each device needs a unique address. These pins are static, dynamic address reallocation is not allowed. SA pins are sampled and latched once the 3.3V rail exceeds 1.8V.

SMBus Address Mapping

Devices	Description	A[7:4]	A[3]	A[2]	A[1]	A[0]	Default Address	Notes
PI6C410B	Server/Workstation Clock Generator	DxH	0	0	1	0	D2H	Fixed address
PI6C20400	1:4 Differential Buffer	DxH	1	1	0	0	DCH	Fixed address
PI6C20800	1:8 Differentiall Buffer	DxH	1	1	0	0	DCH	Fixed address
PI6C21900S	1:19 Differential Buffer	DxH	SA_2	SA_1	SA_0	0	D2H ~ DEH	Address Range
PI6C21900S	1:19 Differential Buffer	DxH	0	x	x	0	D2H ~ D6H	Bypass Mode, default D6H
PI6C21900S	1:19 Differential Buffer	DxH	1	x	x	0	D8H ~ DEH	PLL mode, default addr DEH

Serial Data Interface (SMBus)

PI6C21900S is a slave only SMBus device that supports random byte read and write indexed block read and write protocol using a single 7-bit address and read/write bit as shown below.

Indexed Block Read and Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bits '00000000' Stand for block operation	11:18	Command Code - 8 Bits '00000000' Stand for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count from master - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Datat byte 0 from master - 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Datat byte 1 from master - 8 bits	30:37	Byte count from slave - 8 bits

Indexed Block Read and Write Protocol (contnued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
46	Acknowledge from slave	38	Acknowledge from host
....	Data bytes from master/Acknowledge	39:46	Data byte 0 from slave - 8 bits
....	Data byte N - 8 bits	47	Acknowledge from host
....	Acknowledge from slave	48:55	Data byte 1 from slave - 8 bits
....	Stop	56	Acknowledge from host
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Acknowledge from host
		....	Stop

Random Byte Read and Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write = 0	9	Write - 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed.	11:18	Command Code - 8 bits '100xxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed.
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Acknowledge from master - #38 bit
		39	Stop

Data Byte 0: Control Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	FSB Gear Ratio SMBus	RW	1		N/A
1	FSB Gear Ratio SMBus	RW	0		N/A
2	FSB Gear Ratio SMBus	RW	0		N/A
3	FSB Gear Ratio SMBus	RW	1		N/A
4	FS_A CK410B Latched Input	RW	Depends on FS_A pin(1)		N/A
5		RW	1	Reserved	N/A
6	Group of 1 gear ratio select 0 = Gear Ratio, 1 = 1:1	RW	1	DIF (18) DIF# (18#)	N/A
7	Group of 18 gear ratio select 0 = Gear Ratio, 1 = 1:1	RW	1	DIF(17:0) DIF#(17:0)	N/A

Note:
1. When FS_A = 1, Bit 1 = 0 and Bit 3 = 1; When FS_A = 0, Bit 1 = 1 and Bit 3 = 0

Data Byte 1: Control Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_0 DIF#_0	6,7
1	Output Control 0 = Hi-Z ,1 = Enable	RW	1 = Enable	DIF_1 DIF#_1	8,9
2	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_2 DIF#_2	12,13
3	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_3 DIF#_3	14,15
4	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_4 DIF#_4	16,17
5	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_5 DIF#_5	22,23
6	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_6 DIF#_6	25,26
7	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_7 DIF#_7	30,31

Data Byte 2: Control Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_8 DIF#_8	33,34
1	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_9 DIF#_9	38,39
2	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_10 DIF#_10	41,42
3	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_11 DIF#_11	44,45
4	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_12 DIF#_12	49,50
5	Output Control 0 = Hi-Z, 1 = Enable	RW	1 = Enable	DIF_13 DIF#_13	52,53
6	Bypass and PLL selection 0 = BYPASS, 1 = PLL	RW	1 = PLL	BYPASS# TEST_ MODE / PLL	30
7	PLL Bandwidth Adjust 0 = High Bandwidth, 1=Low Bandwidth	RW	1 = Low BW		1

Data Byte 3: Control Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	SA_2/PLL/BYPASS#	R	Latched input at power up	All	72
1	HIGH_BW#	R	Latched input at power up	All	4
2	OE_01234# Input DIF_01234 Output enable 0 = Enable, 1 = Disable (tristate)	R	Depends on state of pin at power-up	DIF_01234 DIF_01234#	18
3	OE_5# Input DIF_5 Output enable 0 = Enable, 1 = Disable (tristate)	R	Depends on state of pin at power-up	DIF_5 DIF_5#	21
4	OE_6# Input DIF_6 Output enable 0 = Enable, 1 = Disable (tristate)	R	Depends on state of pin at power-up	DIF_6 DIF_6#	24
5	OE_7# Input DIF_7 Output enable 0 = Enable, 1 = Disable (tristate)	R	Depends on state of pin at power-up	DIF_7 DIF_7#	29
6	OE_8# Input DIF_8 Output enable 0 = Enable, 1 = Disable (tristate)	R	Depends on state of pin at power-up	DIF_8 DIF_8#	32
7	OE_9# Input DIF_9 Output enable 0 = Enable, 1 = Disable (tristate)	R	Depends on state of pin at power-up	DIF_9 DIF_9#	37

Data Byte 4: Control Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	OE_10# Input DIF_10 Output enable 0 = Enable, 1 = Disable (Hi-Z)	R	Depends on state of pin at power-up	DIF_10 DIF_10#	40
1	OE_11# Input DIF_11 Output enable 0 = Enable, 1 = Disable (Hi-Z)	R	Depends on state of pin at power-up	DIF_11 DIF_11#	43
2	OE_12# Input DIF_12 Output enable 0 = Enable, 1 = Disable (Hi-Z)	R	Depends on state of pin at power-up	DIF_12 DIF_12#	48
3	OE_13# Input DIF_13 Output enable 0 = Enable, 1 = Disable (Hi-Z)	R	Depends on state of pin at power-up	DIF_13 DIF_13#	51
4	OE_14# Input DIF_14 Output enable 0 = Enable, 1 = Disable (Hi-Z)	R	Depends on state of pin at power-up	DIF_14 DIF_14#	54
5	OE_15# Input DIF_15 Output enable 0 = Enable, 1 = Disable (Hi-Z)	R	Depends on state of pin at power-up	DIF_15 DIF_15#	57
6	OE_16_17# Input DIF_16_17 Output enable 0 = Enable, 1 = Disable (Hi-Z)	R	Depends on state of pin at power-up	DIF_16, DIF_17 DIF_16#, DIF_17#	60
7	OE_17_18# Input DIF_17_18 Output enable 0 = Enable, 1 = Disable (Hi-Z)	R	Depends on state of pin at power-up	DIF_18 DIF_18#	69

Data Byte 5: Pericom ID Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	Vendor ID – VID0	R	0	N/A	N/A
1	Vendor ID – VID1	R	0	N/A	N/A
2	Vendor ID – VID2	R	0	N/A	N/A
3	Vendor ID – VID3	R	0	N/A	N/A
4	Revision ID – RID0	R	0	N/A	N/A
5	Revision ID – RID1	R	1	N/A	N/A
6	Revision ID – RID2	R	0	N/A	N/A
7	Revision ID – RID3	R	0	N/A	N/A

Data Byte 6: Pericom Device ID Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	Device ID 0	R	0	N/A	N/A
1	Device ID 1	R	0	N/A	N/A
2	Device ID 2	R	1	N/A	N/A
3	Device ID 3	R	1	N/A	N/A
4	Device ID 4	R	0	N/A	N/A
5	Device ID 5	R	0	N/A	N/A
6	Device ID 6	R	0	N/A	N/A
7	Device ID 7 (MSB)	R	0	N/A	N/A

Data Byte 7: Byte Counter Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	BC0 - Writing to this register configures how many bytes will be read back	RW	1	N/A	N/A
1	BC1 - Writing to this register configures how many bytes will be read back	RW	0	N/A	N/A
2	BC2 - Writing to this register configures how many bytes will be read back	RW	0	N/A	N/A
3	BC3 - Writing to this register configures how many bytes will be read back	RW	1	N/A	N/A
4	BC4 - Writing to this register configures how many bytes will be read back	RW	0	N/A	N/A
5	BC5 - Writing to this register configures how many bytes will be read back	RW	0	N/A	N/A
6	BC6 - Writing to this register configures how many bytes will be read back	RW	0	N/A	N/A
7	BC7 - Writing to this register configures how many bytes will be read back	RW	0	N/A	N/A

Data Byte 8: Control Register

Bit	Description / Function Center	Type	Power up Condition	Output(s) Affected	Source Pin
0	Output Control 0 = Hi-Z 1 = Enable	RW	1 = Enable	DIF_14 DIF#_14	55, 56
1		RW	1 = Enable	DIF_15 DIF#_15	58, 59
2		RW	1 = Enable	DIF_16 DIF#_16	61, 62
3		RW	1 = Enable	DIF_17 DIF#_17	65, 66
4		RW	1 = Enable	DIF_18 DIF#_18	67, 68
5				Reserved	
6				Reserved	
7	FS_A	R	Latched Value at power up	All	5

Current-mode output buffer characteristics of OUT[0:18], OUT[0:18]#

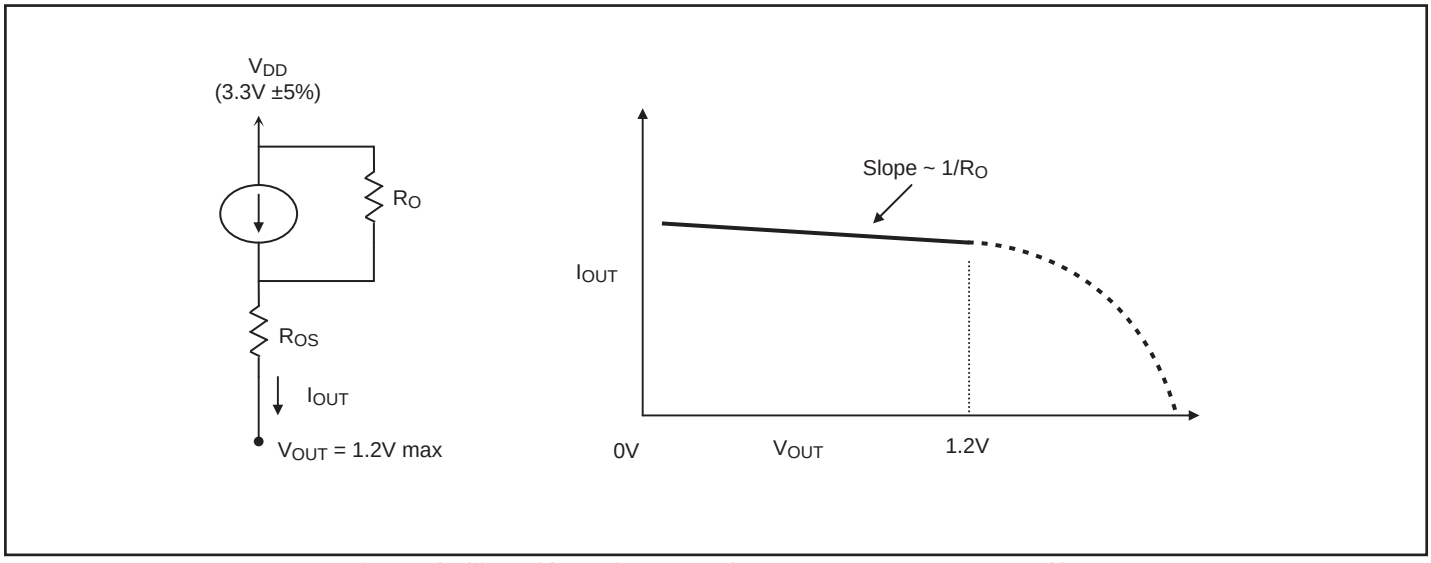


Figure 3. Simplified diagram of current-mode output buffer

Differential Clock Buffer Characteristics

Symbol	Minimum	Maximum
R_O	3000Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	850mV

Current Accuracy

Symbol	Conditions	Configuration	Load	Min.	Max.
I_{OUT}	V_{DD} = 3.30 ±5%	R_{REF} = 475Ω 1% I_{REF} = 2.32mA	Nominal test load for given configuration	-12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Note: $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Differential Clock Output Current

Board Target Trace/Term Z	Reference R, Iref = V_{DD}/(3xRr)	Output Current	V_{OH} @ Z
100Ω differential	R_{REF}= 475Ω 1%, I_{REF} = 2.32mA	I_{OH} = 6 x Iref	0.7V @ 50-Ohm

Absolute Maximum Ratings (Over free-air operating temperature range)

Symbol	Parameters	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage	-0.5	4.6	V
V_{DD}	3.3V I/O Supply Voltage	-0.5	4.6	
V_{IH}	Input High Voltage		4.6	
V_{IL}	Input Low Voltage	-0.5		
Ts	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V

Note: Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3 ±5%)

Symbol	Parameters	Condition	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage		3.135	3.465	V
V_{DD}	3.3V I/O Supply Voltage		3.135	3.465	
V_{IH}	3.3V Input High Voltage		2.0	V_{DD} + 0.3	
V_{IL}	3.3V Input Low Voltage		V_{SS} – 0.3	0.8	
I_{IL}	Input Leakage Current (1)	0 < V_{IN} < V_{DD}	-5	+5	µA
V_{IH_FS}	FS_A Input High Voltage (2)		0.7	V_{DD} + 0.3	V
V_{IL_FS}	FS_A Input High Voltage (2)		V_{SS} – 0.3	0.35	

DC Electrical Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3 ±5%, continued)

Symbol	Parameters	Condition	Min.	Max.	Units
V_{OH}	3.3V Output High Voltage	I_{OH} = -1mA	2.4		V
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1mA		0.4	
C_{IN}	Input Pin Capacitance (3)		2.5	4.5	pF
C_{OUT}	Output Pin Capacitance (3)		2.5	4.5	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No air flow	0	70	°C
I_{DD}	Power Supply Current	V_{DD} = 3.465V, F_{CPU} = 400MHz		600	mA
I_{SS}	Power Down Current	Tristate outputs		36	

Notes:
1. Input Leakage Current does not include inputs with pullups or pulldowns.
2. Internal voltage reference is used to guarantee these thresholds
3. Internal silicon capacitance, does not include pin capacitance

Skew and Jitter Characteristics

Input to output relationships are applicable only in 1:1 mode. Output to output relationships are applicable when all outputs are the same frequency.

In PLL mode, DIF_18 can be configured as 1:1, different from the others. The default is same gear ratio. This group of two and group of five may incur additional skew from the others.

Skew and Jitter Timing Parameters (Ta = 0 ~ 70C, Vdd = 3.3V, 5%)

Symbol	Description	Conditions	Min	Max	Unit	Notes
Tpd_PLL_nom	CLK to DIF_xx Skew in 1:1 PLL mode	Nominal Voltage and Temperature		1.0	ns	1,2,4,5
Tpd_Bypass_nom	CLK to DIF_xx Skew in 1:1 Bypass mode		2.5	5.5	ns	2,3,5
Tskew1	DIF_[0:17] output to output Skew			100	ps	1,2
Tskew_all	DIF_[0:18] output to output Skew	Same gear ratio or Bypass mode		250	ps	1,2,3

Notes:
1. Measured across 2pF.
2. Measured between differential crosspoints
3. Applicable to same edges; i.e. rising to rising, or falling to falling
4. Deterministic values
5. Measured mean values with scope averaging on

PLL Bandwidth and Peaking

Parameter	Target	Min	Max	Unit	Notes
PLL Peaking (HIGH_BW# = 0)	< 1.0		< 2.5	dB	2
PLL Peaking (HIGH_BW# = 1)	< 1.0		< 2.0	dB	2
PLL Bandwidth (HIGH_BW# = 0)	3	2	4	MHz	1
PLL Bandwidth (HIGH_BW# = 1)	1	0.7	1.4	MHz	1

Notes:
1. Measured @ 3dB down or Half Power point
2. Measured as max pass band gain
3. Post processed evaluation through Intel FB-DIMM Draft Spec Rev. 0.5.
4. These jitter are needed to achieve BER of 1E-12. Measured values with smaller sample size have to ve extrapolated to acheive 1E-12 BER.

Differential AC Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3 ±5%, SSC=-0.5%)

Symbol	Parameters	Min.	Max.	Unit	Notes
T_{stab}	Clock Stabilization Time		1.8	ms	9
T_{period}	Average Period (variation from ideal period), non-SSC	-0.3	+0.3	%	4,5,8
	Average Period (variation from ideal period), SSC mode	-0.3	+0.53		
T_{abs_min}	Absolute Minimum Period, non-SSC (from ideal period)	-2.5			
	Absolute Minimum Period, SSC mode	T_{period} - 0.125		ns	
T_{rise} / T_{fall}	Rise and Fall Time (between 0.175V to 0.525V)	175	700	ps	2,4,7,21
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation		75		4,7,18
Edge_rate	Edge rate	0.5	2.0	V/ns	
V_{high}	Voltage High (typ. = 0.7V)	660	850	mV	4,7,10,11
V_{low}	Voltage Low (typ. = 0.0V)	-150			
V_{x_abs}	Absolute Crossing Point Voltages	200	550		1,3,4,7,14
V_{x_rel}	Relative Crossing Point Voltages	Calc	Calc		4,6,7,14
Total ΔV_x	Total Variation of (Vx) Vcross over all edges		140		4,7,15
$T_{ccjitter}$	Cycle to Cycle Jitter		50	ps	4,8,20,22
T_{dc}	Duty Cycle	45	55	%	4,8,21
V_{ovs}	Overshoot Voltage		Voh + 0.3	V	4,7,12
V_{uds}	Undershoot Voltage		-0.3		4,7,13
V_{rb}	Ringback Voltage, Non SSC	0.2			4,7
	Ringback Voltage, SSC mode	Vx-0.2	Vx+0.2		
T_{jadd}	Additive RMS phase jitter		0.7	ps	23

Differential AC Characteristics (V_{DD} = 3.3±5%, V_{DD_A} = 3.3 ±5%, SSC=-0.5%, continued)

Notes:

1. Instantenous voltage crossing point where "rising edge CLK" = "falling edge CLK#"
2. Measured from Vol = 0.175 V to Voh = 0.525 V. Only valid for Rising clock and Falling clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
3. Total variation from the lowest to the highest crossing point, on both differential rising and falling edges
4. Test configuration is Rs = 33.2 Ohm, Rp = 49.9 Ohm, and 2pF.
5. The average period over any 1 µs period of time must be greater than the minimum and less than the maximum specified period
6. Vx_rel_min = 0.25 + 0.5 * (Vh_avg - 0.70); Vx_rel_max = 0.55 - 0.5*(Vh_avg - 0.70)
7. Single ended waveform measurement
8. Differential waveform measurement
9. Measured from: (i) power supply ramp up, or (ii) valid CLK clock input; to stable output clock (PLL is locked)
10. Vhigh = Statistical Average High value from the oscilloscope Vhigh Math function
11. Vlow = Statistical Average Low value from the oscilloscope Vlow Math function
12. Overshoot = Absolute Maximum Voltage
13. Undershoot = Absolute Minimum Voltage
14. Crossing Point must simultaneously meet absolute and relative crossing point specifications
15. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system
16. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 100,000,000 Hz, 133,333,333 Hz, 166,666,666 Hz and 200,000,000 Hz
17. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz, 166,250,000 Hz and 199,500,000 Hz
18. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
19. Measured with oscilloscope, averaging on, The difference between the rising edge rate (average) of clock verses the falling edge rate (average) of clock#
20. Measured in PLL mode; in Bypass mode, jitter is additive
21. Measured at < 270 mHz
22. Measure with M1•
23. Additive jitter is calculated from input and output RMS phase jitter by using PCIe GenII filter. ($T_{jadd} = \sqrt{(\text{output jitter})^2-(\text{input jitter})^2}$

Configuration Test Load Board Termination

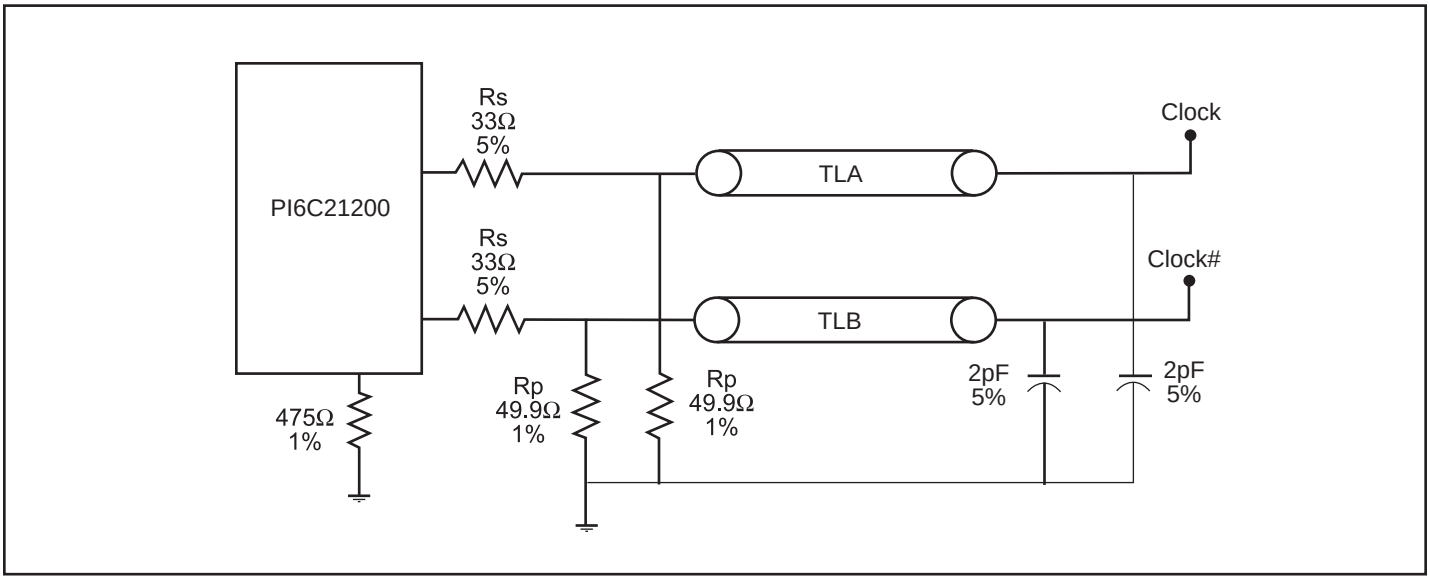
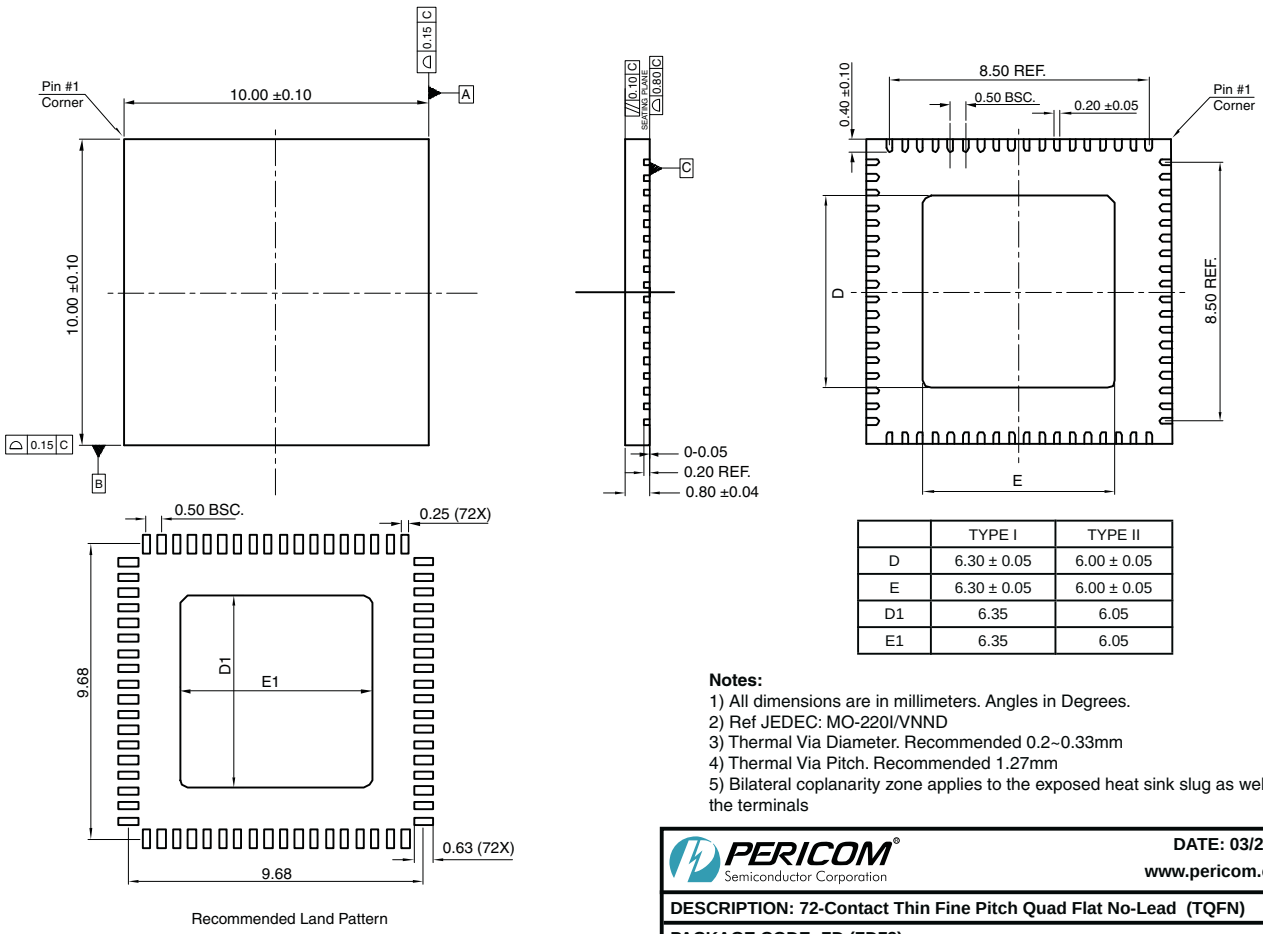


Figure 4. Configuration test load board termination

Note: TLA and TLB are 3" transmission lines.

Packaging Mechanical: 72-lead, TQFN (ZD)



Recommended Land Pattern

	TYPE I	TYPE II
D	6.30 ± 0.05	6.00 ± 0.05
E	6.30 ± 0.05	6.00 ± 0.05
D1	6.35	6.05
E1	6.35	6.05

Notes:
1) All dimensions are in millimeters. Angles in Degrees.
2) Ref JEDEC: MO-220I/VNND
3) Thermal Via Diameter. Recommended 0.2~0.33mm
4) Thermal Via Pitch. Recommended 1.27mm
5) Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals

PERICOM Semiconductor Corporation
DATE: 03/27/06
www.pericom.com

DESCRIPTION: 72-Contact Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD72)

DOCUMENT CONTROL #: PD-2037 **REVISION: C**

Ordering Information:

Ordering Code	Packaging Code	Package Type
PI6C21900SZDE	ZD	72-Lead TQFN, Pb-Free and Green

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X Suffix = Tape/Reel