M36L0T7060T2
M36L0T7060B2

128 Mbit (Multiple Bank, Multilevel, Burst) Flash memory and 64 Mbit (4 Mb x16) PSRAM, multichip package

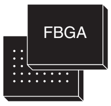
Preliminary Data

Features

- Multichip package
  - 1 die of 128 Mbit (8 Mb x16, Multiple Bank, Multilevel, Burst) Flash Memory
  - 1 die of 32 Mbit (2 Mb x16) Pseudo SRAM
- Supply voltage
  - V_{DDF} = 1.7 to 2.0 V
  - V_{CCP} = V_{DDQ} = 2.7 to 3.5 V
  - V_{PPF} = 9 V for fast program
- Electronic signature
  - Manufacturer Code: 20h
  - Device Code (Top Flash Configuration) M36L0T7060T2: 88C4h
  - Device Code (Bottom Flash Configuration) M36L0T7060B2: 88C5h
- ECOPACK® packages available

Flash memory

- Synchronous / Asynchronous Read
  - Synchronous Burst Read mode: 52 MHz
  - Random Access: 85 ns
- Synchronous Burst Read Suspend
- Programming time
  - 2.5 µs typical Word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple Bank Memory Array: 8 Mbit Banks
  - Parameter Blocks (Top or Bottom location)
- Dual operations
  - program/erase in one Bank while read in others
  - No delay between read and write operations



TFBGA88 (ZAQ)
8 × 10 mm

- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}$ for Block Lock-Down
  - Absolute Write Protection with $V_{PP} = V_{SS}$
- Security
  - 64 bit unique device number
  - 2112 bit user programmable OTP Cells
- Common Flash Interface (CFI)
- 100,000 program/erase cycles per block

PSRAM

- Access time: 65 ns
- Low standby current: 90 µA ($T_A \leq 40$°C)
- Deep Power-Down current: 10 µA
- Byte control: $\overline{UB}_P$/$\overline{LB}_P$
- Compatible with standard LPSRAM
- Power-Down modes
  - Deep Power-Down

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1 Description

The M36L0T7060T2 and M36L0T7060B2 combine two memory devices in a multichip package:

- a 128-Mbit, Multiple Bank, Multilevel, Burst, Flash memory, the M58LT128HT or M58LT128HB
- a 64-Mbit PseudoSRAM, the M69KW096B.

The purpose of this document is to describe how the two memory components operate with respect to each other. It should be read in conjunction with the M58LT128HTB and M69KW096B datasheets, where all specifications required to operate the Flash memory and PSRAM components are fully detailed. These datasheets are available from your local STMicroelectronics distributor.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA88 (8 x 10 mm, 8x10 ball array, 0.8 mm pitch) package. The devices are supplied with all the bits erased (set to ‘1’).

Figure 1. Logic diagram

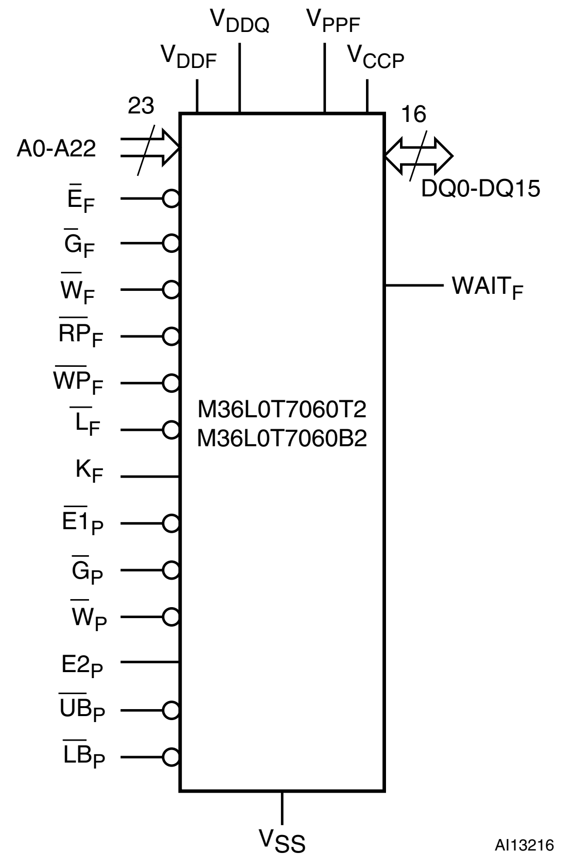
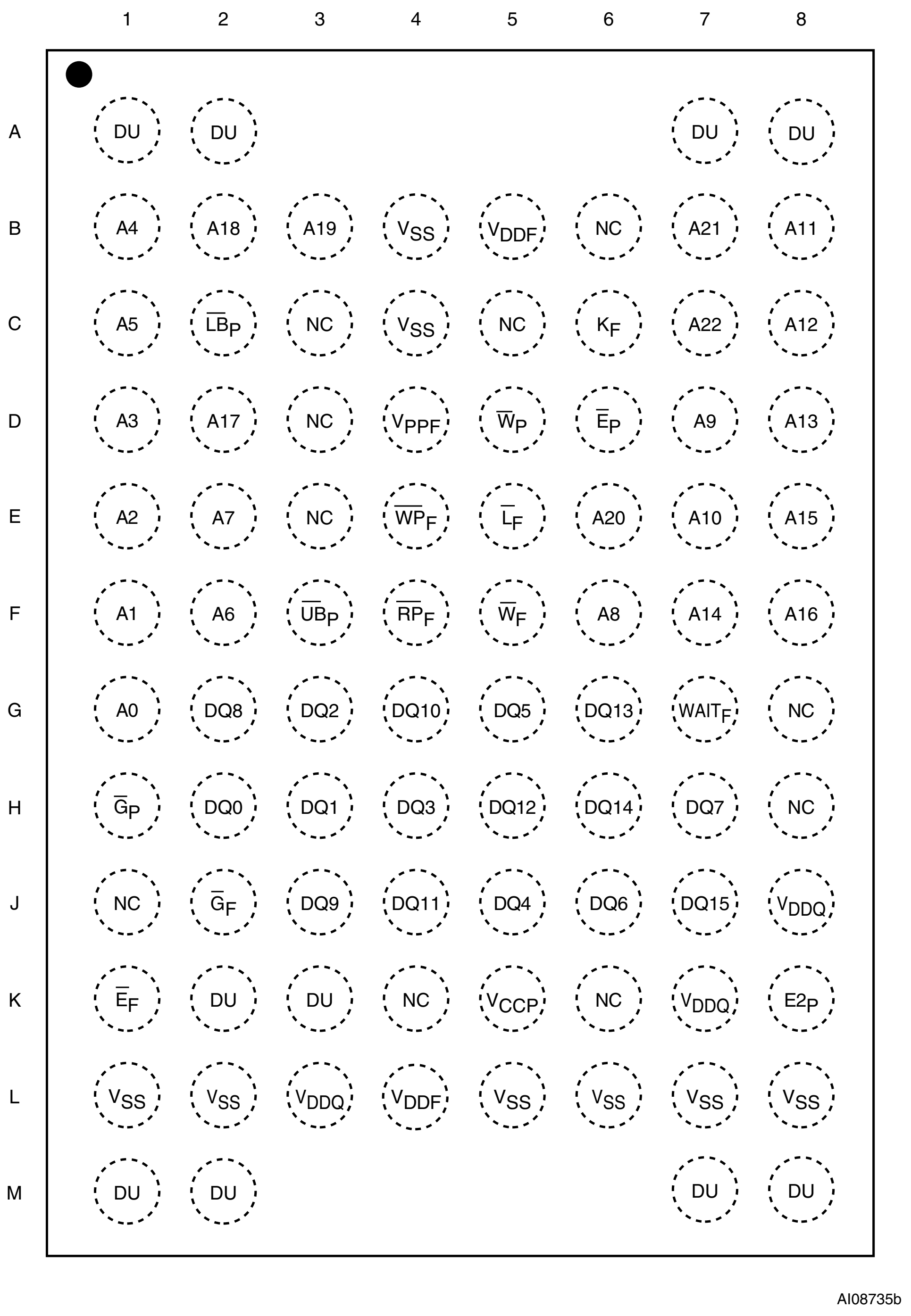


Table 1. Signal names

A0-A22(1)	Address Inputs
DQ0-DQ15	Common Data Input/Output
V_{DDF}	Power Supply for Flash Memory
V_{DDQ}	Flash Memory Power Supply for I/O Buffers
V_{PPF}	Flash Optional Supply Voltage for Fast Program and Erase
V_{SS}	Ground
V_{CCP}	PSRAM Power Supply
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash memory signals	
$\overline{L}_{F}$	Latch Enable Input
$\overline{E}_{F}$	Chip Enable Input
$\overline{G}_{F}$	Output Enable Input
$\overline{W}_{F}$	Write Enable Input
$\overline{RP}_{F}$	Reset Input
$\overline{WP}_{F}$	Write Protect Input
K_{F}	Burst Clock
$WAIT_{F}$	Wait Data in Burst Mode
PSRAM signals	
$\overline{E1}_{P}$	Chip Enable Input
$\overline{G}_{P}$	Output Enable Input
$\overline{W}_{P}$	Write Enable Input
$E2_{P}$	Power-down Input
$\overline{UB}_{P}$	Upper Byte Enable Input
$\overline{LB}_{P}$	Lower Byte Enable Input

1. A22 is not connected to the PSRAM component.

Figure 2. TFBGA connections (top view through package)



	1	2	3	4	5	6	7	8
A	DU	DU					DU	DU
B	A4	A18	A19	V_{SS}	V_{DDF}	NC	A21	A11
C	A5	$\overline{LB}_P$	NC	V_{SS}	NC	K_F	A22	A12
D	A3	A17	NC	V_{PPF}	$\overline{W}_P$	$\overline{E}_P$	A9	A13
E	A2	A7	NC	$\overline{WP}_F$	$\overline{L}_F$	A20	A10	A15
F	A1	A6	$\overline{UB}_P$	$\overline{RP}_F$	$\overline{W}_F$	A8	A14	A16
G	A0	DQ8	DQ2	DQ10	DQ5	DQ13	$WAIT_F$	NC
H	$\overline{G}_P$	DQ0	DQ1	DQ3	DQ12	DQ14	DQ7	NC
J	NC	$\overline{G}_F$	DQ9	DQ11	DQ4	DQ6	DQ15	V_{DDQ}
K	$\overline{E}_F$	DU	DU	NC	V_{CCP}	NC	V_{DDQ}	$E2_P$
L	V_{SS}	V_{SS}	V_{DDQ}	V_{DDF}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
M	DU	DU					DU	DU

2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A22)

Addresses A0-A21 are common inputs for the Flash memory and the PSRAM components. The other line (A22) is an input for the Flash memory component only.

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller in the Flash memory, and they select the cells to be accessed in the PSRAM.

2.2 Data input/output (DQ0-DQ15)

In the Flash memory, the Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Write Bus operation.

In the PSRAM DQ0-DQ7 and/or DQ8-DQ15 carry the data to or from the upper and/or lower part(s) of the selected address during a Write or Read operation, when Upper Byte Enable ($\overline{UB}_P$) and/or Lower Byte Enable ($\overline{LB}_P$) is/are driven Low.

2.3 Flash Chip Enable ($\overline{E}_F$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to set $\overline{E}_F$ at V_{IL}, $\overline{E1}_P$ at V_{IL} and $E2_P$ at V_{IH} at the same time.

2.4 Flash Output Enable ($\overline{G}_F$)

The Output Enable input controls data output during Flash memory Bus Read operations.

2.5 Flash Write Enable ($\overline{W}_F$)

The Write Enable controls the Bus Write operation of the Flash memories' Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.6 Flash Write Protect ($\overline{WP}_F$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH}, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See the Lock Status Table in the M58LT128HTB datasheet).

2.7 Flash Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to M58LT128HTB datasheet for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

2.8 Flash Latch Enable ($\overline{L}_F$)

Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is Low, V_{IL}, and it is inhibited when Latch Enable is High, V_{IH}. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

2.9 Flash Clock (K_F)

The Clock input synchronizes the Flash memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is don't care during Asynchronous Read and in write operations.

2.10 Flash Wait ($WAIT_F$)

WAIT is a Flash output signal used during Synchronous Read to indicate whether the data on the output bus are valid. This output is high impedance when Flash Chip Enable is at V_{IH} or Flash Reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance. The $WAIT_F$ signal is not gated by Output Enable.

2.11 PSRAM Chip Enable input ($\overline{E1}_P$)

When asserted (Low), the Chip Enable, $\overline{E1}_P$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power Standby mode.

It is not allowed to set $\overline{E}_F$ at V_{IL}, $\overline{E1}_P$ at V_{IL} and $E2_P$ at V_{IH} at the same time.

2.12 PSRAM Chip Enable input ($E2_P$)

The Chip Enable, $E2_P$, puts the device in Deep Power-down mode when it is driven Low. This is the lowest power mode.

2.13 PSRAM Write Enable ($\overline{W}_P$)

The Write Enable, $\overline{W}_P$, controls the Bus Write operation of the memory.

2.14 PSRAM Output Enable ($\overline{G}_P$)

The Output Enable, $\overline{G}_P$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

2.15 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte Enable, $\overline{UB}_P$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

2.16 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

2.17 V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal cores of the Flash memory component. It is the main power supply for all Flash operations (Read, Program and Erase).

2.18 V_{CCP} supply voltage

The V_{CCP} Supply Voltage supplies the power for all operations (Read or Write) and for driving the refresh logic, even when the device is not being accessed.

2.19 V_{DDQ} supply voltage

V_{DDQ} provides the power supply for the Flash memory I/O pins. This allows all Outputs to be powered independently of the Flash Memory core power supply, V_{DDF}.

2.20 V_{PPF} Program supply voltage

V_{PPF} is both a Flash control input and a Flash power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQ}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLKF} gives an absolute protection against Program or Erase, while $V_{PPF} > V_{PP1}$ enables these functions (see the M58LT128HTB datasheet for the relevant values). V_{PPF} is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

2.21 V_{SS} ground

V_{SS} is the common ground reference for all voltage measurements in the Flash (core and I/O Buffers) and PSRAM chips.

Note: *The Flash memory device in a system should have their supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1 µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 5: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.*

3 Functional description

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E1}_P$ and $E2_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations in the Flash memory and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other device in the high impedance state when reading the selected device.

Figure 3. Functional block diagram

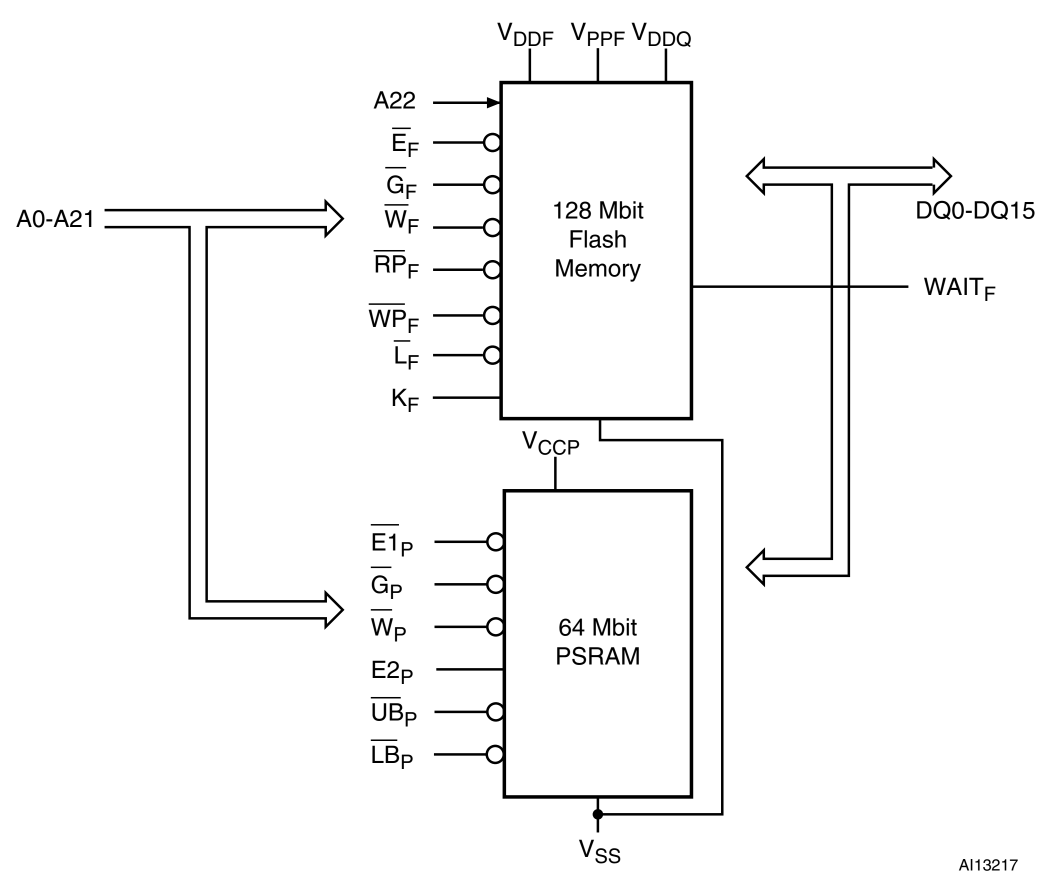


Table 2. Operating modes[1]

Operation	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{L}_F$	$\overline{RP}_F$	$WAIT_F$[2]	$E2_P$	$\overline{E1}_P$	$\overline{W}_P$	$\overline{G}_P$	$\overline{LB}_P$	$\overline{UB}_P$	A21	DQ0-DQ7	DQ8-DQ15
Flash Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}[3]	V_{IH}			PSRAM must be disabled						Data Out	
Flash Write	V_{IL}	V_{IH}	V_{IL}	V_{IL}[3]	V_{IH}									Data In	
Flash Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}									Data Out or Hi-Z[4]	
Flash Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	Hi-Z		Any PSRAM mode is allowed						Hi-Z	
Flash Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z								Hi-Z	
Flash Reset	X	X	X	X	V_{IL}	Hi-Z								Hi-Z	
Deep Power-Down[5]	Flash memory must be disabled						V_{IL}	X	X	X	X	X	X	Hi-Z	Hi-Z
Standby (Deselected)							V_{IH}	V_{IH}	X	X	X	X	X	Hi-Z	
Output Disable							V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	[6]	Hi-Z	
										V_{IL}	V_{IH}	V_{IH}	Valid	Hi-Z	
No Read	Any Flash memory mode is allowed										V_{IH}	V_{IH}		Hi-Z	Hi-Z
Upper Byte Read											V_{IH}	V_{IL}		Hi-Z	Data Output
Lower Byte Read											V_{IL}	V_{IH}		Data Output	Hi-Z
Word Read											V_{IL}	V_{IL}		Data Output	Data Output
No Write									V_{IL}	V_{IH}[7]	V_{IH}	V_{IH}		Invalid	Invalid
Upper Byte Write											V_{IH}	V_{IL}		Invalid	Data Input
Lower Byte Write											V_{IL}	V_{IH}		Data Input	Invalid
Word Write											V_{IL}	V_{IL}		Data Input	Data Input

1. X = Don't care.
2. WAIT signal polarity is configured using the Set Configuration Register command. See the M58LT128HTB datasheet for details.
3. $\overline{L}_F$ can be tied to V_{IH} if the valid address has been previously latched.
4. Depends on $\overline{G}_F$.
5. Deep Power-Down mode can be entered from Standby state and all DQ pins are in High-Z state.
6. A0 to A21 can be either V_{IH} or V_{IL} but must valid before the read or write operation.
7. $\overline{G}_P$ can be V_{IL} during the Write operation if the following conditions are satisfied:
   a- Write pulse is initiated by $\overline{E1}_P$ ($\overline{E1}_P$ Controlled Write timing), or cycle time of the previous operation cycle is satisfied.
   b- $\overline{G}$ stays V_{IL} during the entire Write cycle.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–25	85	°C
T_{BIAS}	Temperature Under Bias	–25	85	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{IO}	Input or Output Voltage	–0.5	3.6	V
V_{DDF}	Flash Memory Core Supply Voltage	–0.2	2.5	V
V_{DDQ}, V_{CCP}	PSRAM and Input/Output Supply Voltages	–0.2	3.6	V
V_{PPF}	Flash Program Voltage	–0.2	10	V
I_O	Output Short Circuit Current	–	100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Flash memories		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} Supply Voltage	1.7	2.0	–	–	V
V_{CCP} Supply Voltage	–	–	2.7	3.5	V
V_{DDQ} Supply Voltage	2.7	3.5	–	–	V
V_{PPF} Supply Voltage (Factory environment)	8.5	9.5	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQ} +0.4	–	–	V
Ambient Operating Temperature	–25	85	–30	85	°C
Load Capacitance (C_L)	30		50		pF
Output Circuit Resistors (R_1, R_2)	22		22		kΩ
Input Rise and Fall Times		5	5		ns
Input Pulse Voltages	0 to V_{DDQ}		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		$V_{DDQ}/2$		V

Figure 4. AC measurement I/O waveform

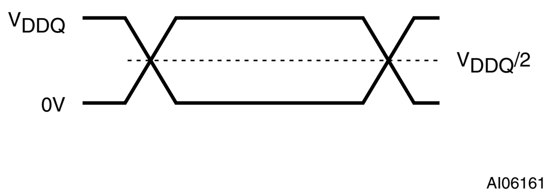


Figure 5. AC measurement load circuit

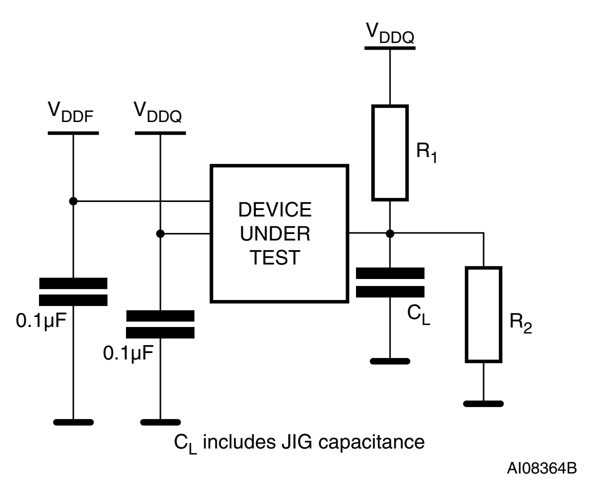


Table 5. Device capacitance[1]

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		15	pF

1. Sampled only, not 100% tested.

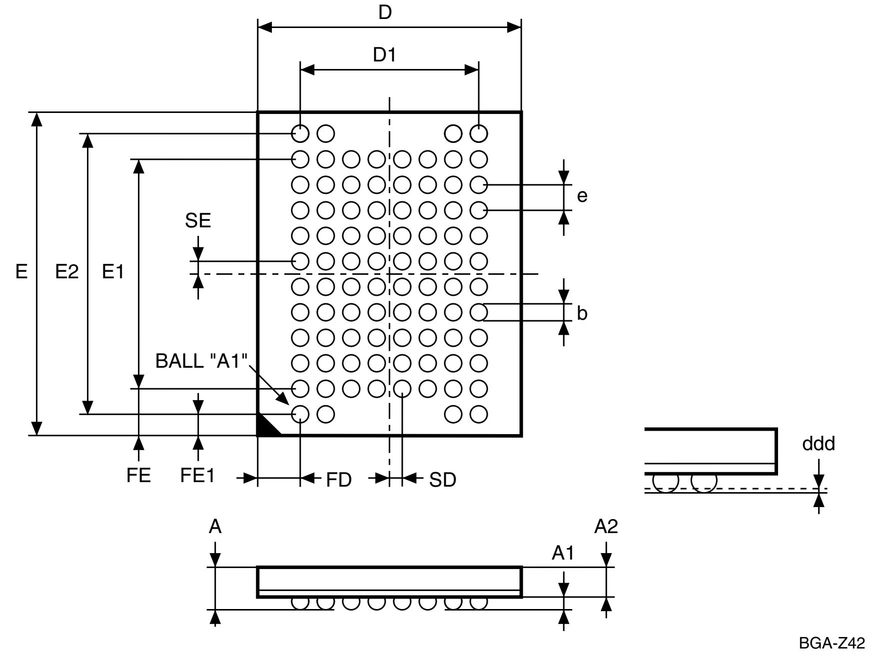
Please refer to the M58LT128HTB and M69KW096B datasheets for further DC and AC characteristic values and illustrations.

6 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 6. Stacked TFBGA88 8x10 mm - 8x10 active ball array, 0.8 mm pitch, bottom view outline



1. Drawing is not to scale.

Table 6. Stacked TFBGA88 8x10 mm - 8x10 active ball array, 0.8 mm pitch, package data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

7 Part numbering

Table 7. Ordering information scheme

Example: M36 L 0 T 7 0 6 0 T 2 ZAQ F

Device Type
M36 = Multichip package (Flash + RAM)

Flash 1 Architecture
L = Multilevel, Multiple Bank, Burst mode

Flash 2 Architecture
0 = No Die

Operating Voltage
T = V_{DDF} = 1.7 to 2.0 V; V_{DDQ} = V_{CCP} = 2.7 to 3.5 V

Flash 1 Density
7 = 128 Mbit

Flash 2 Density
0 = No Die

RAM 1 Density
6 = 64 Mbit

RAM 0 Density
0 = No Die

Parameter Blocks Location
T = Top Boot Block Flash
B = Bottom Boot Block Flash

Product Version
2 = 90 nm Flash technology and Multilevel design, 85 ns speed; 0.13 µm RAM, 65 ns speed

Package
ZAQ = Stacked TFBGA88 8x10 mm - 8x10 active ball array, 0.8 mm pitch

Option
Blank = Standard Packing
T = Tape & Reel Packing
E = ECOPACK® package, standard packing
F = ECOPACK® package, tape and reel packing

Devices are shipped from the factory with the memory content bits erased to ’1’. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
30-May-2006	0.1	Initial release.
20-Apr-2007	1	Document status changed from Target Specification to Preliminary Data. Updated V_{DDF}, V_{CCP} and V_{DDQ} voltage ranges. *Section 2.7: Flash Reset (RP_F)* updated.

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