

Low drop voltage regulator

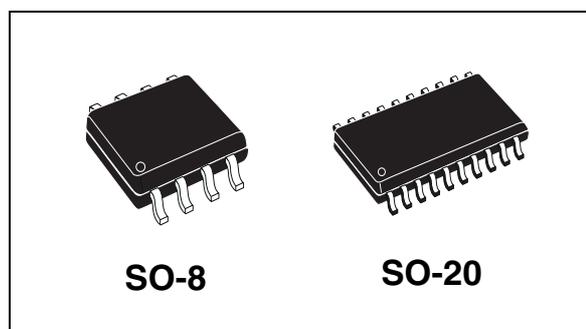
Preliminary Data

Features

Max DC supply voltage	V_S	40V
Max output voltage tolerance	ΔV_O	+/-2%
Max dropout voltage	V_{dp}	500mV
Output current	I_O	150mA
Quiescent current	I_{qn}	70 μ A ⁽¹⁾

1. Typical value with regulator disabled

- Operating DC supply voltage range 5.6V to 31V
- Reset circuit sensing the output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external capacitor
- Enable input for enabling/disabling the watchdog functionality
- Thermal shutdown and short circuit protection
- Wide temperature range ($T_j = -40^\circ\text{C}$ to 150°C)



Description

The L4993 is a monolithic integrated 5V Voltage regulator with a low drop voltage at currents up to 150mA.

The output voltage regulating element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40V.

The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The L4993 is protected against short circuit and an over-temperature protection switches off the device in case of extremely high power dissipation. The L4993 is active when the Enable is high. State of the art features like reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.

Table 1. Device summary

Package	Tube	Tape & reel
SO8	L4993D	L4993DTR
SO20 (16+2+2)	L4993MD	L4993MDTR

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1 Block diagram and pins description

Figure 1. Block diagram

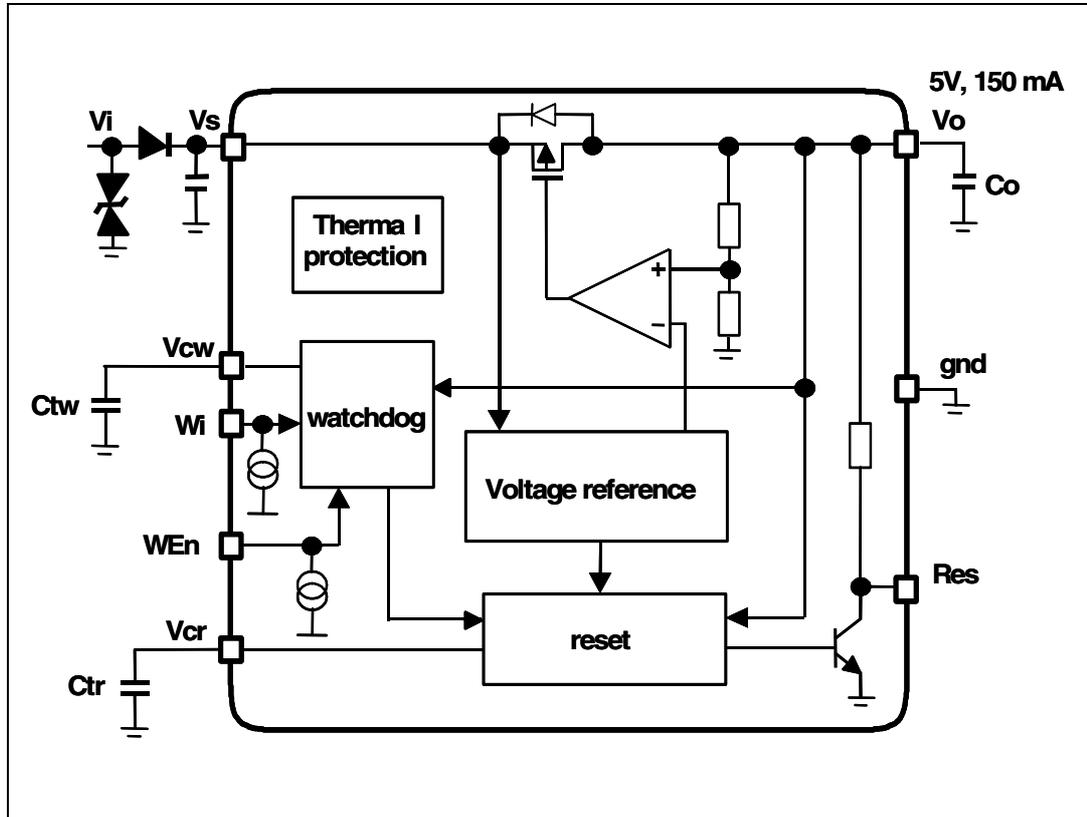
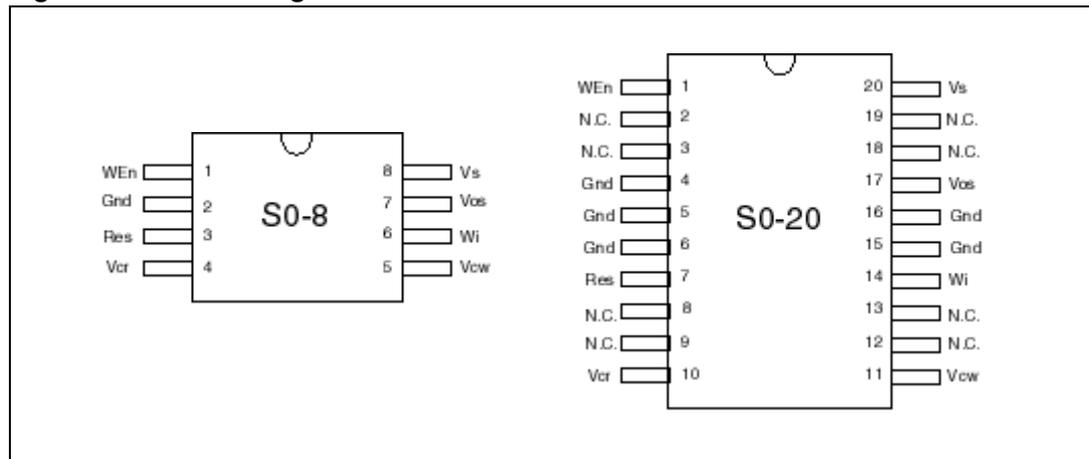


Table 2. Pins description

Pin name	SO8(D)	S020(MD)	Function
WEn	1	1	Watchdog Enable input If high watchdog functionality is active
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below V_{o_th} or frequency at W_i is too low.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
V_{o_s}	7	17	Voltage regulator output Block to ground with a capacitor >100nF (needed for regulator stability)
V_s	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

Figure 2. Pins configuration



2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{VSDC}	DC supply voltage	-0.3 to 40	V
I_{VSDC}	Input current	Internally limited	
V_{Vo}	DC output voltage	-0.3 to 6	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{Od}	Open drain output voltage	-0.3 to $V_{Vo} + 0.3$	V
I_{Od}	Open drain output current	Internally limited	
V_{Cr}	Reset delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{Cw}	Watchdog delay voltage	-0.3 to $V_{Vo} + 0.3$	V
V_{WEn}	Watchdog Enable input voltage	-0.3 to $V_{Vo} + 0.3$	V
T_j	Junction temperature	-40 to 150	°C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	S08	S016+2+2	Unit
$R_{th-jamb}$	Thermal resistance Junction to Ambient (S08)	130-180	50 ⁽¹⁾	°C/W

1. With 6 sq. cm on board heatn sink

2.3 Electrical characteristics

Table 5. Electrical characteristics
($V_s = 5.6V$ to $31V$, $T_j = -40^\circ C$ to $+150^\circ C$ unless otherwise specified)

Pin	Symbol	Parameter	Test condition	min	typ	max	Unit
5V Voltage regulator							
Vo	V_{o_ref}	Output voltage	$V_s = 6$ to $31V$ $I_o = 1$ to $150mA$	4.9	5.0	5.1	V
Vo	I_{short}	Short circuit current	$V_s = 13.5V^{(1)}$	160	210	250	mA
Vo	I_{lim}	Output current limitation	$V_s = 13.5V^{(1)}$	150	250	350	mA
V_s, V_o	V_{line}	Line regulation voltage	$V_s = 6$ to $31V$ $I_o = 1$ to $150mA$			25	mV
Vo	V_{load}	Load regulation voltage	$I_o = 1$ to $150mA$			25	mV
V_s, V_o	V_{dp}	Drop voltage	$I_o = 150mA$		200	400	mV
V_s, V_o	SVR	Ripple rejection	$f_r = 100 Hz^{(2)}$	55			dB
General							
V_s, V_o	I_q	Quiescent current	$V_s=13.5V,$ $I_o=150mA,$ $WEn = high$		1.45	2	mA
V_s, V_o	I_q	Quiescent current	$V_s=13.5V, I_o=$ $50mA,$ $WEn = high$		538	1000	μA
V_s, V_o	I_q	Quiescent current	$V_s=13.5V, I_o<$ $1mA,$ $WEn = high$		110	170	μA
V_s, V_o	I_q	Quiescent current	$V_s=13.5V, I_o<$ $1mA,$ $WEn = low$		69	115	μA
	T_w	Thermal protection temperature		150		190	$^\circ C$
	T_w_hy	Thermal protection temperature hysteresis			10		$^\circ C$
Reset							
Res	V_{res_l}	Reset output low voltage	$R_{ext} = 5k\Omega$ to $V_o,$ $V_o > 1V$			0.4	V
Res	I_{Res_h}	Reset output high leakage current	$V_{Res} = 5V$			1	μA
Res	R_{p_u}	Pull up internal resistance	with respect to V_o	12	25	50	$k\Omega$
Res	V_o_th	V_o out of regulation threshold	$V_s = 6$ to $31V,$ $I_o = 1$ to $150mA$	6%	8%	10%	below V_{o_ref}

Table 5. Electrical characteristics (continued)
 ($V_s = 5.6V$ to $31V$, $T_j = -40^\circ C$ to $+150^\circ C$ unless otherwise specified)

Pin	Symbol	Parameter	Test condition	min	typ	max	Unit
Vcr	Vrlth	Reset timing low threshold	$V_s = 13.5V$	10%	13%	16%	V_{o_ref}
Vcr	Vrhth	Reset timing high threshold	$V_s = 13.5V$	44%	47%	50%	V_{o_ref}
Vcr	Icr	Charge current	$V_s = 13.5V$	8	17.6	30	μA
Vcr	Idr	Discharge current	$V_s = 13.5V$	8	17.6	30	μA
Res	Trr_2	Reset reaction time ⁽³⁾	$V_o = V_{o_th} - 100mV$	100	250	700	μs
Res	Trd	Reset delay time	$V_s = 13.5V$, $C_{tr} = 1nF$	65		150	ms
Watchdog							
Wi	Vih	Input high voltage	$V_s = 13.5V$	3.5			V
Wi	Vil	Input low voltage	$V_s = 13.5V$			1.5	V
Wi	Vih	Input hysteresis	$V_s = 13.5V$		300		mV
Wi	Ii	Pull down current	$V_s = 13.5V$		10	20	μA
Vcw	Vwhth	High threshold	$V_s = 13.5V$	2.20	2.35	2.50	V
Vcw	Vwlth	Low threshold	$V_s = 13.5V$	0.50	0.65	0.80	V
Vcw	Icwc	Charge current	$V_s = 13.5V$, $V_{cw} = 0.1V$	4	8	14	μA
Vcw	Icwd	Discharge current	$V_s = 13.5V$, $V_{cw} = 2.5V$	1.0	2.13	4.5	μA
Vcw	Twop	Watchdog period	$V_s = 13.5V$, $C_{tw} = 47nF$	25	50	90	ms
Res	twol	Watchdog output low time	$V_s = 13.5V$, $C_{tw} = 47nF$	6	10.5	22	ms
Watchdog Enable							
WEn	V_{En_l}	Enable input low voltage				1	V
WEn	V_{En_h}	Enable input high voltage		3			V
WEn	V_{En_hy}	Enable input hysteresis		500	800	1100	mV
WEn	I_leak	Pull down current	$WEn = 5V$	2	8	20	μA

1. See [Figure 3](#)
2. Guaranteed by design
3. When V_o becomes lower than $4V$, the reset reaction time decreases down to $2\mu s$ assuring a faster reset condition in this particular case.

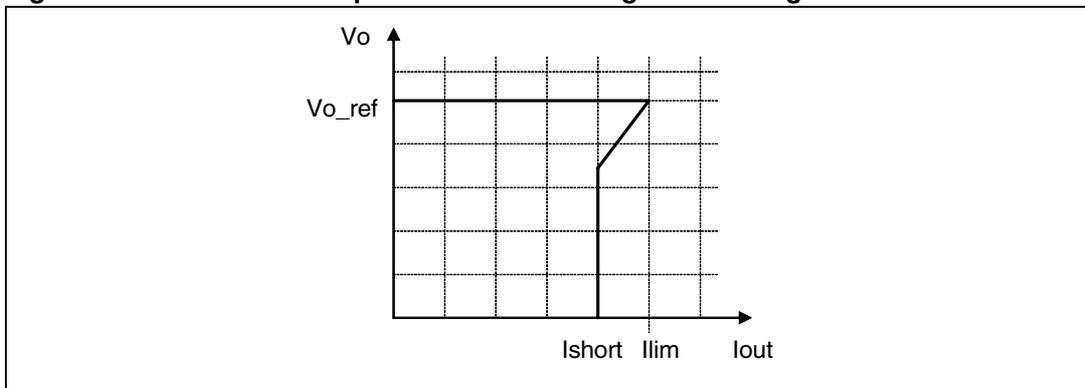
3 Application information

The input capacitor $C_s > 200\text{nF}$ is necessary for the smoothing of line disturbances. The output capacitor $C_{O1} > 100\text{nF}$ is necessary for the stability of the regulation loop. In order to damp output voltage oscillations during high load current surges, it is recommended put an additional electrolytic capacitor $C_{O2} > 10\mu\text{F}$ at the output pin.

3.1 Voltage regulator

Voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at current up to 150mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. A short circuit protection to GND is provided.

Figure 3. Behavior of output current versus regulated voltage V_o



3.2 Reset

The reset circuit monitors the output voltage V_o . If the output voltage becomes lower than V_{o_th} then Res goes low with a delay time t_{rr} . If the output voltage becomes lower than 2.0 V (typ) than Res goes immediately low. The reset low signal is guaranteed for an output voltage V_o greater than 1V.

When the output voltage becomes higher than V_{o_th} then Res goes high with a delay t_{rd} . This delay is obtained by 512 periods of oscillator. The oscillator period is given by :

$$T_{osc} = [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{cr} + [(V_{rhth} - V_{rlth}) \times C_{tr}] / I_{dr}$$

and reset pulse delay t_{rd} is given by:

$$t_{rd} = 512 \times T_{osc}$$

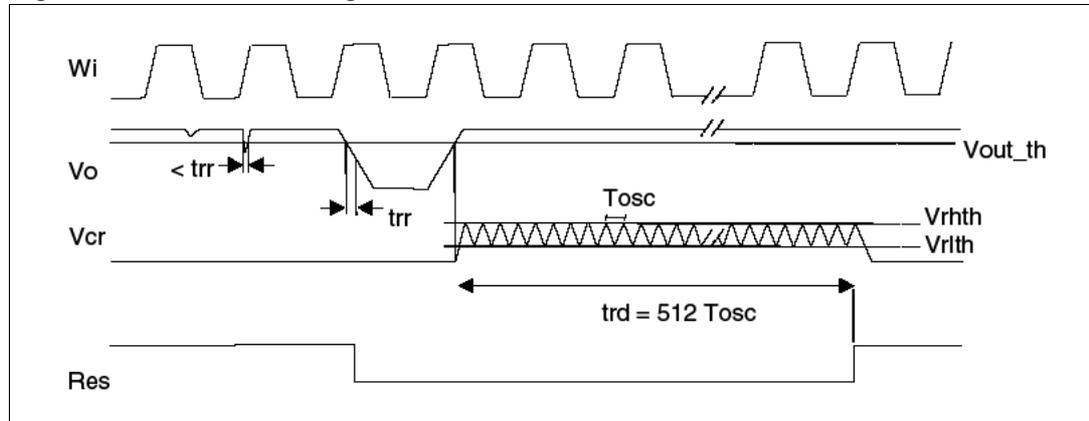
where:

$I_{cr} = 17.6 \mu\text{A}$ is an internally generated charge current,

$I_{dr} = 17.6 \mu\text{A}$ is an internally generated discharge current,

Vrhth = 2.35 V (typ) and Vrlth =0.65 V (typ) are two voltage thresholds
 Ctr is an external capacitance.

Figure 4. Reset time diagram



3.3 Watchdog

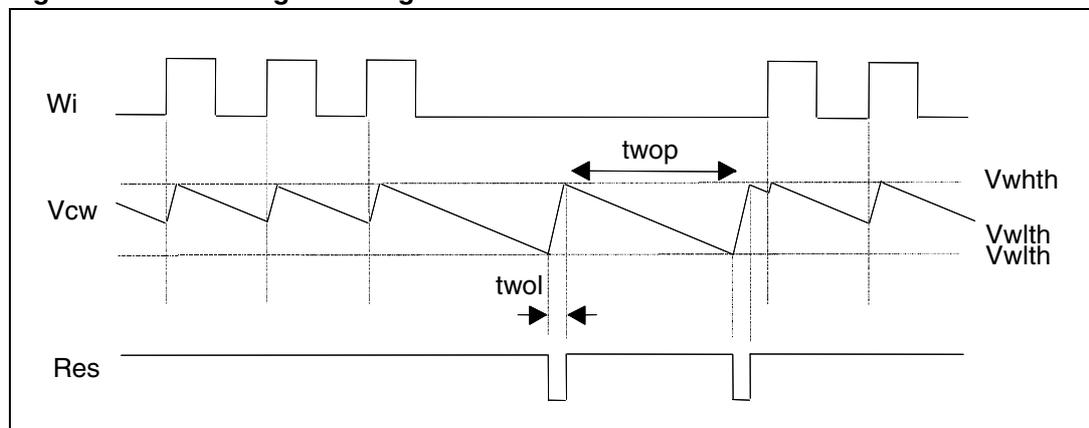
The watchdog input **Wi** monitors a connected microcontroller. If pulses are missing, the Reset output pin is set to low. This functionality can be disabled setting **WEn** input to a level low. The pulse sequence time can be adjusted within a wide range with the external capacitor **Ctw**. The watchdog circuit discharges the capacitor **Ctw** with a constant current **Icwd**. If the lower threshold **Vwlth** is reached, a watchdog reset is generated. To prevent this reset condition, the microcontroller must generate a positive edge during the discharge phase of the capacitor before the voltage reaches the threshold **Vwlth**.

In order to calculate the minimum time **Tdis** during which the microcontroller must provide the positive edge, the following equation can be used:

$$(Vwhth - Vwlth) \times Ctw = Icwd \times Tdis$$

Every **Wi** positive edge switches the current source from discharging to charging, the same happens when the lower threshold is reached. When the voltage reaches the upper threshold **Vwhth** the current switches from charging to discharging. The result is a sawtooth waveform at the watchdog timer capacitor **Ctw**.

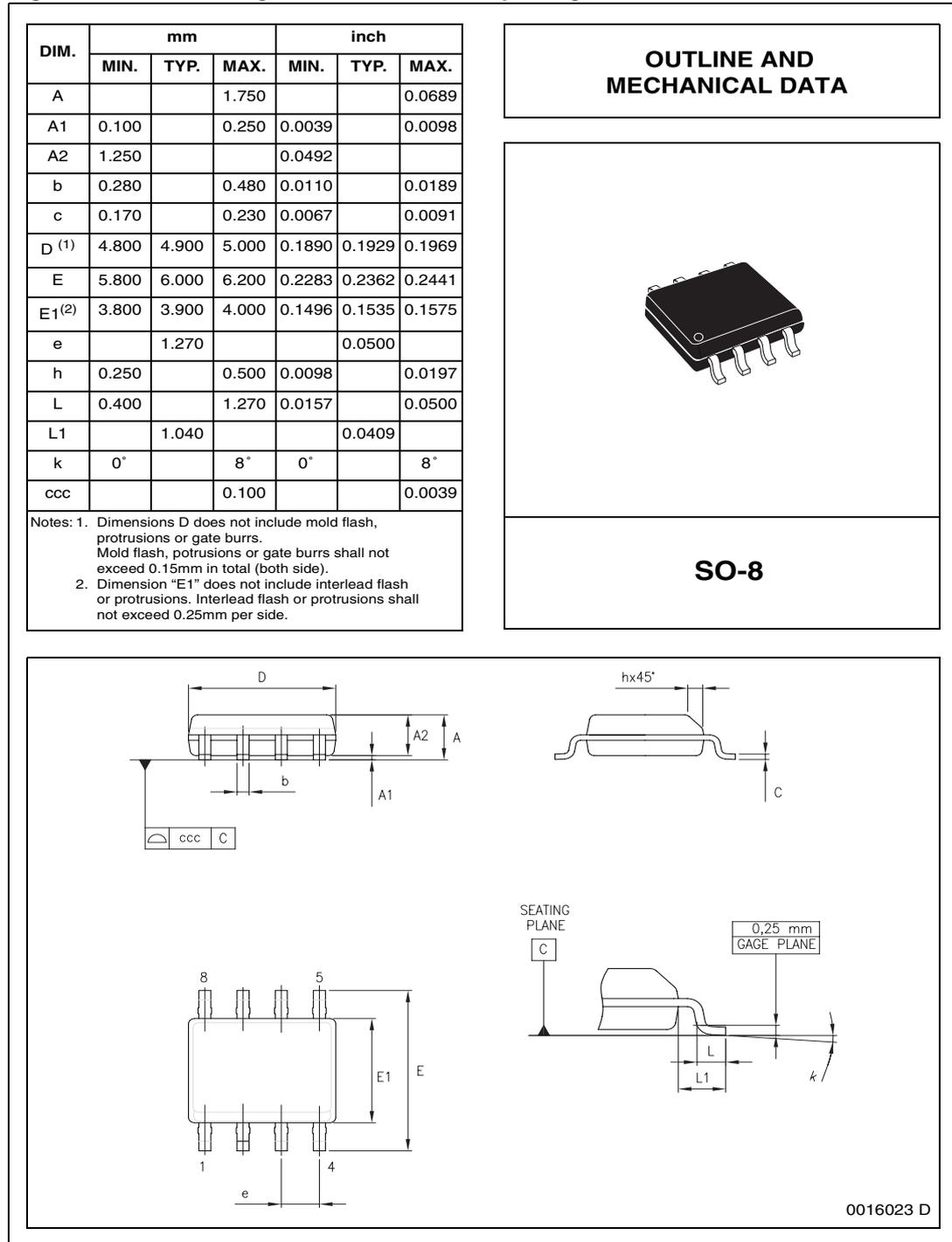
Figure 5. Watchdog time diagram



4 Package and packing information

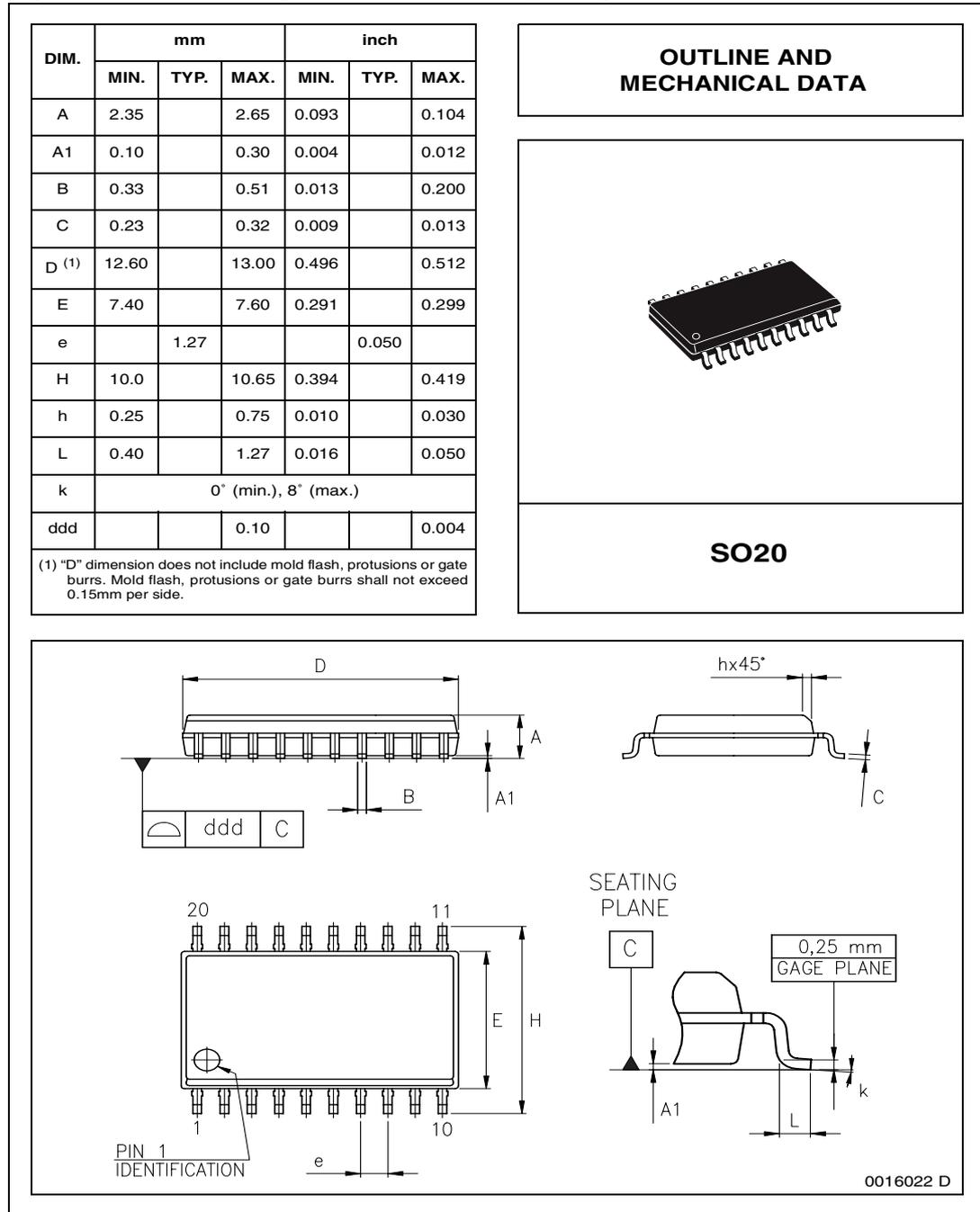
4.1 SO8 Package mechanical data

Figure 6. SO8 Package mechanical data & package outline



4.2 SO20 Package mechanical data

Figure 7. SO20 Package mechanical data & package outline



4.3 SO8 Packing information

Figure 8. SO-8 Tube shipment (no suffix)

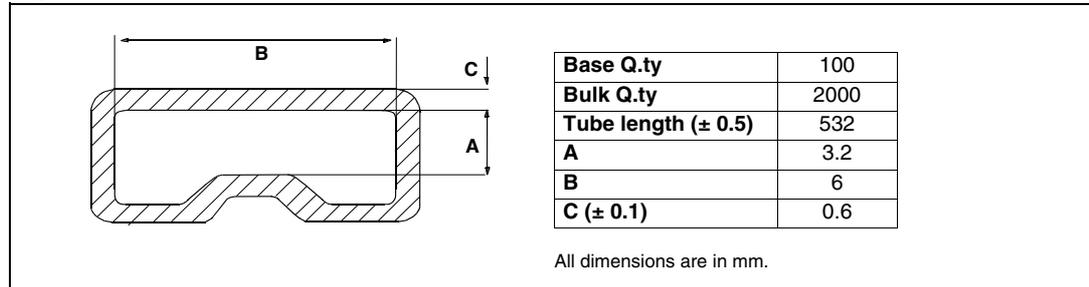
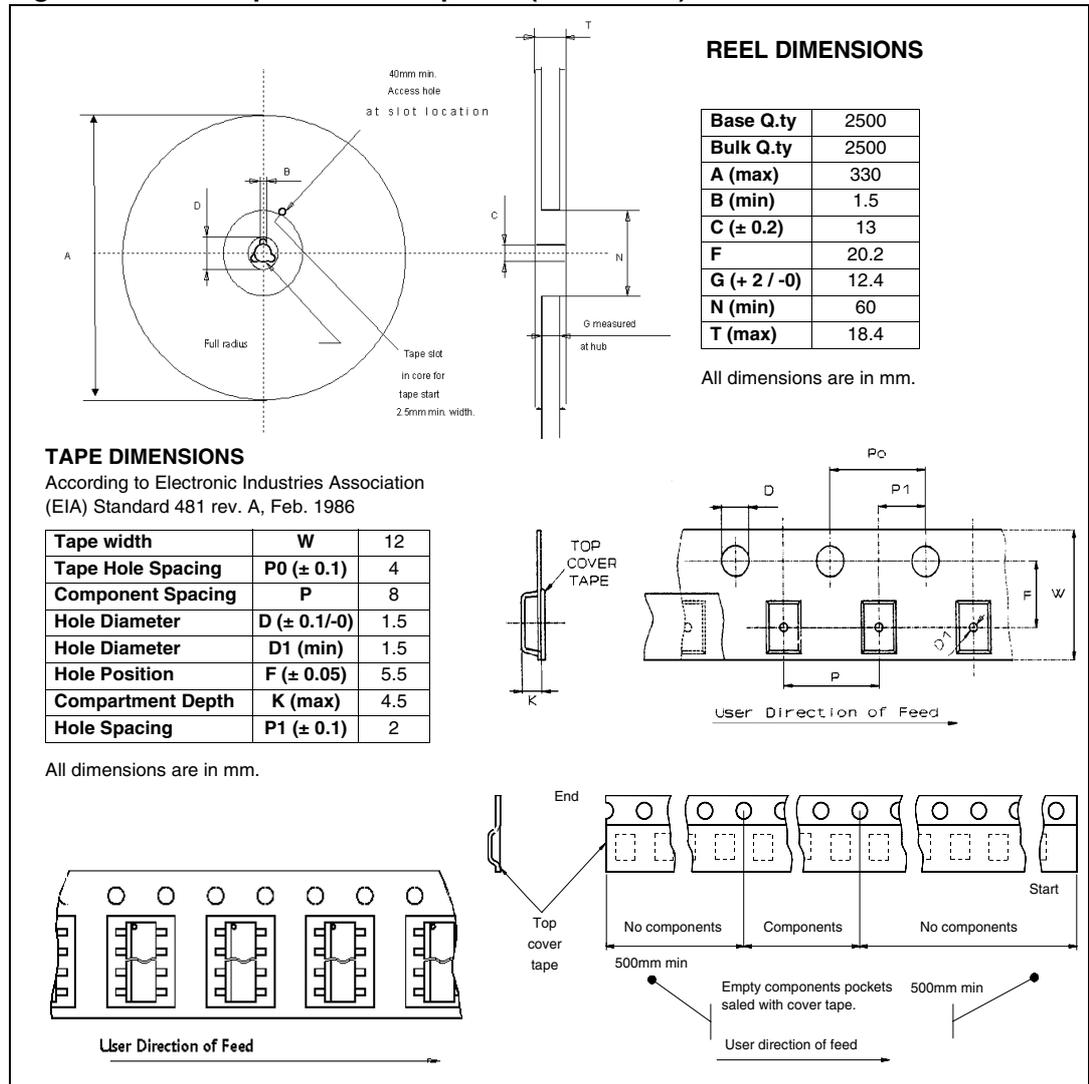


Figure 9. SO-8 Tape and reel shipment (suffix "TR")



4.4 SO-20 Packing information

Figure 10. SO-20 Tube shipment (no suffix)

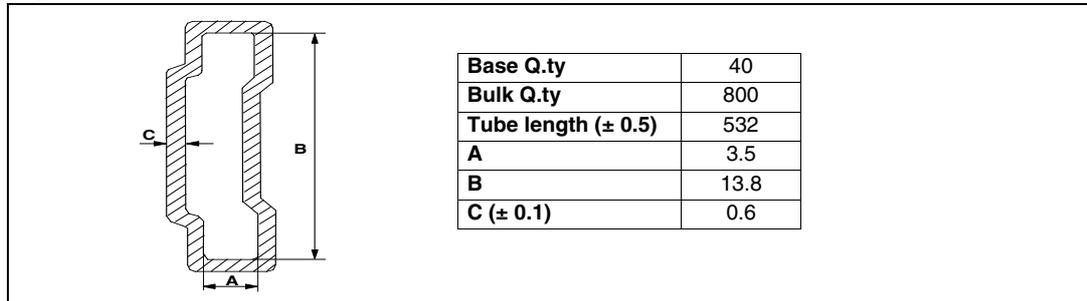
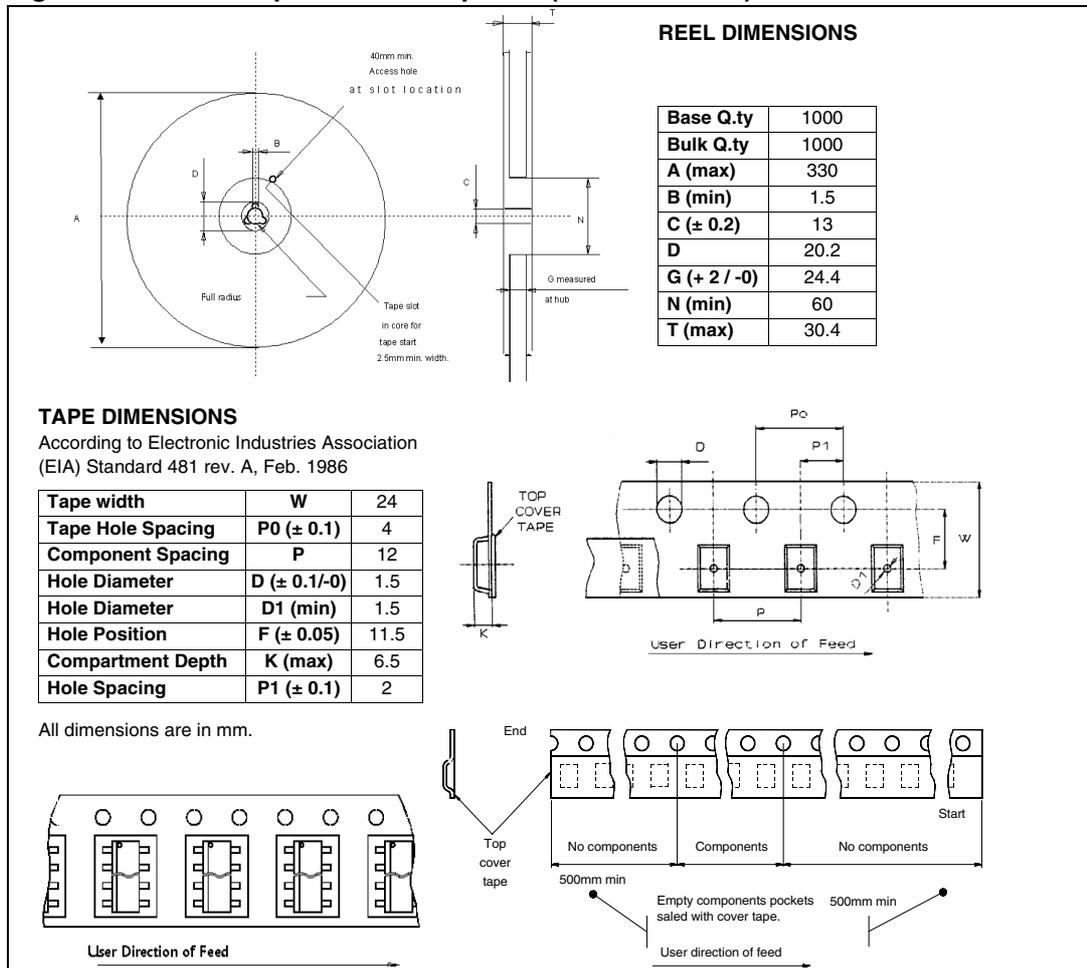


Figure 11. SO-20 Tape and reel shipment (suffix "013TR")



5 Revision History

Table 6. Document revision history

Date	Revision	Changes
June-2004	1	Initial release.
18-Jan-2007	2	Table 5, 6, 7 and 8 updated
01-Jun-2007	3	Document put in corporate technical literature template. Table 4 updated

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