# ESDARF01-1BM2

## ESD protection for AM and FM antenna

## Main applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Portable audio systems
- Communication systems
- Cellular phone handsets and accessories
- Audio and video equipment

## Features

- 1 line bi-directional protection
- Very low capacitance (3 pF typical)
- Lead-free package

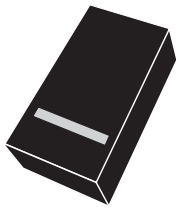
## Description

The ESDARF01-1BM2 is a monolithic application specific device dedicated to ESD protection of the AM and FM antenna in cell phones and portable equipment.

The device is ideal for applications where both reduced printed circuit board space and power absorption capability are required.

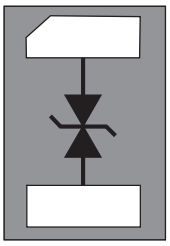
## Benefits

- Very low capacitance, line to ground, for optimized data integrity
- Low PCB space consumption: 0.6 mm² max
- Enhanced ESD protection, IEC 61000-4-2 level4 compliant
  - > 15 kV Air discharge
  - > 8 kV Contact discharge
- No insertion loss in AM and FM Band
- High reliability offered by monolithic integration



**SOD-882**

### Functional diagram



### Order code

| Part number | Marking |
|---|---|
| ESDARF01-1BM2 | D |

### Complies with the following standards:

**IEC 61000-4-2 level 4**

15 kV (air discharge)

8 kV (contact discharge)

**MIL STD 883G - Method 3015-7: class 3B**

# 1 Characteristics

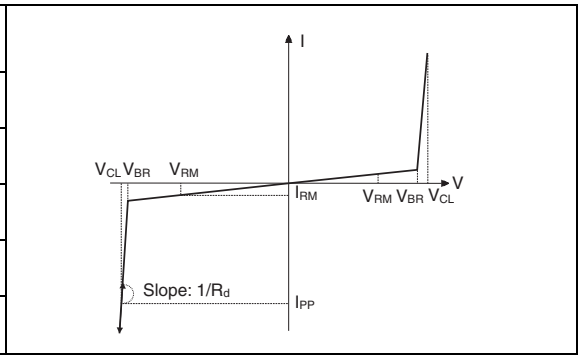
**Table 1. Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{PP}$ (1) | Peak pulse voltage | IEC 61000-4-2 contact discharge<br>IEC 61000-4-2 air discharge | 8<br>15 | kV |
| $T_j$ | Maximum operating junction temperature | | 125 | °C |
| $T_{stg}$ | Storage temperature range | | - 55 to +150 | °C |
| $T_L$ | Maximum lead temperature for soldering during 10 s at 5 mm for case | | 260 | °C |

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

**Table 2. Electrical characteristics**

| Symbol | Parameter |
|---|---|
| $V_{RM}$ | Stand-of voltage |
| $V_{BR}$ | Breakdown voltage |
| $V_{CL}$ | Clamping voltage |
| $I_{RM}$ | Leakage current @ $V_{RM}$ |
| $I_{PP}$ | Peak pulse current |




| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ. | Max. | |
| $V_{BR}$ | Breakdown voltage | $I_R$ = 1 mA | 0.7 | 1.0 | 1.3 | V |
| $I_{RM}$ | Leakage Current | $V_{RM}$ = 100 mV | | | 0.3 | µA |
| $C_{i/o-i/o}$ | Capacitance between I/O and GND | $V_R$ = 0 V, F = 1 MHz,<br>any I/O pin to GND | | 3 | 3.5 | pF |

**Figure 1. Relative variation of leakage current versus junction temperature (typical values)**

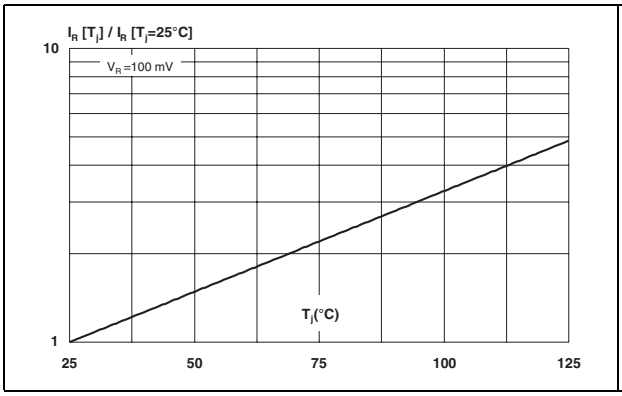



**Figure 2. S21 attentuation measurements (50 Ω / 50 Ω)**

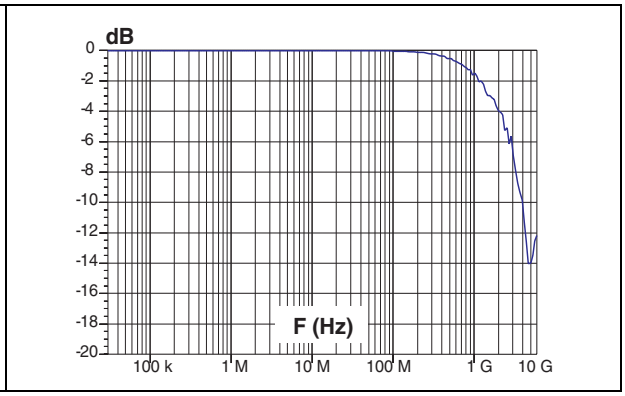



**Figure 3. ESD response to IEC 61000-4-2 (+15 kV air discharge)**

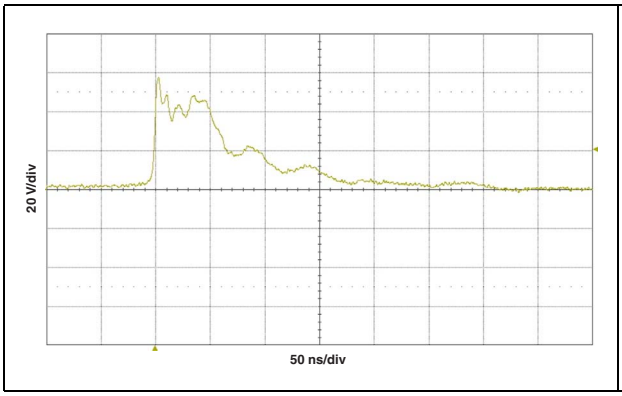



**Figure 4. ESD response to IEC 61000-4-2 (-15 kV air discharge)**

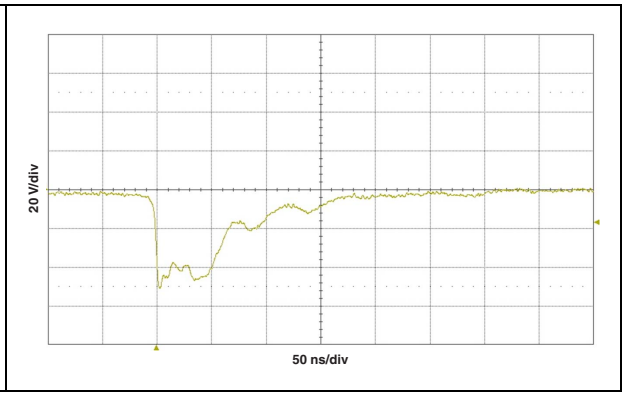
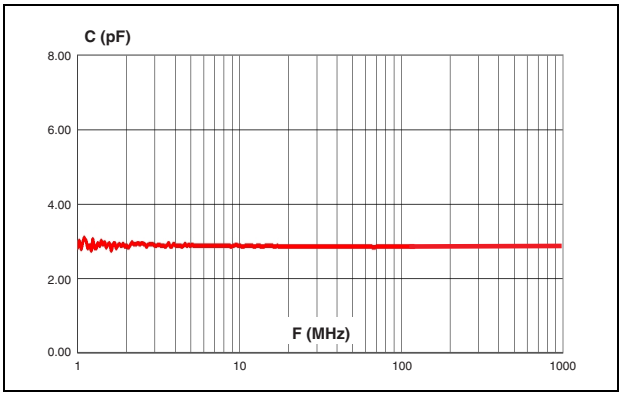
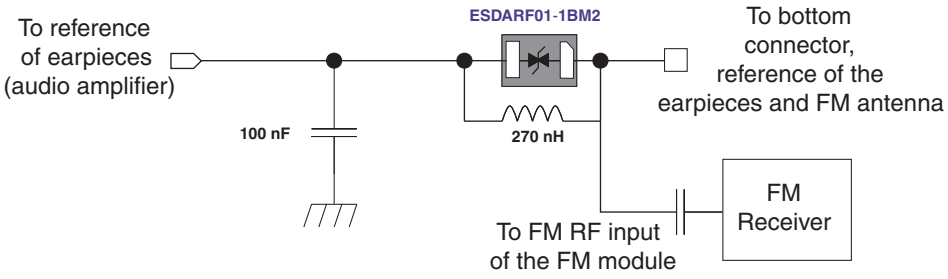



**Figure 5. Junction capacitance versus frequency (typical values)**

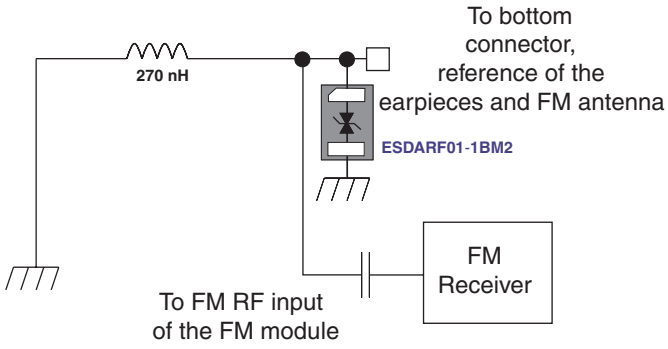


# 2 Application schematics

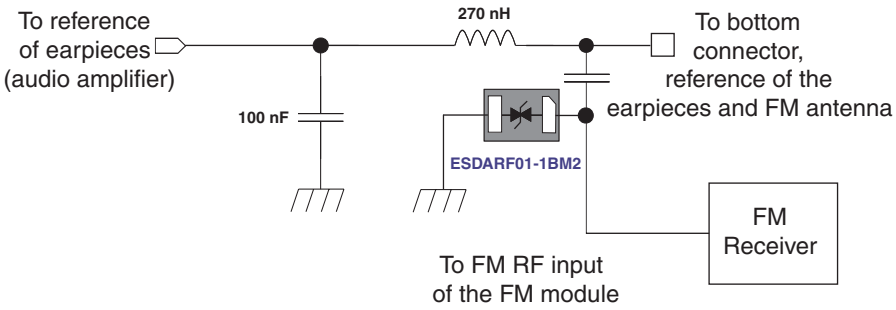
**When the reference of earpieces (audio amplifier) is different from 0 V**



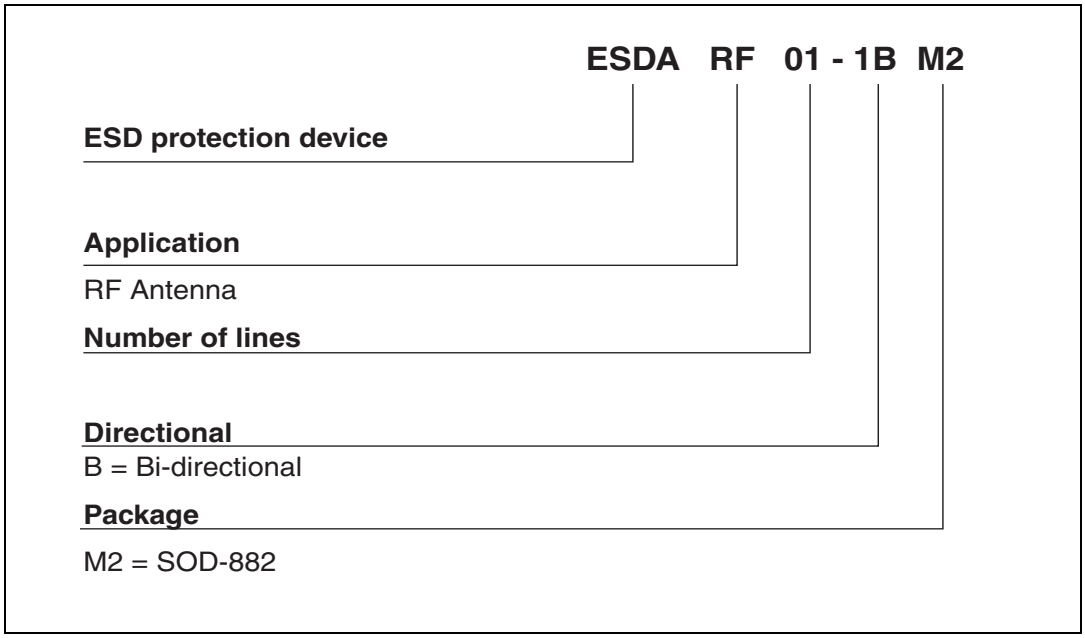

**When the reference of earpieces (audio amplifier) is 0 V**




**Whatever the reference of earpieces (audio amplifier)**



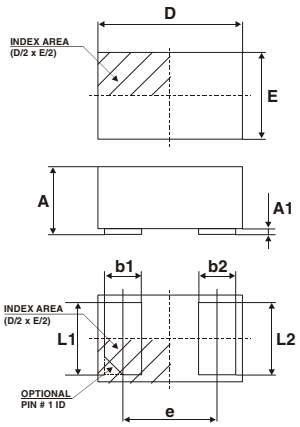
# 3 Ordering information scheme




# 4 Package information

- Epoxy meets UL94, V0

**Table 3. SOD-882 dimensions**




| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.40 | 0.47 | 0.50 | 0.016 | 0.019 | 0.020 |
| A1 | 0.00 | | 0.05 | 0.000 | | 0.002 |
| b1 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| b2 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | | 1.00 | | | 0.039 | |
| E | | 0.60 | | | 0.024 | |
| e | | 0.65 | | | 0.026 | |
| L1 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| L2 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |

**Figure 6. SOD-882 footprint (dimensions in mm)**

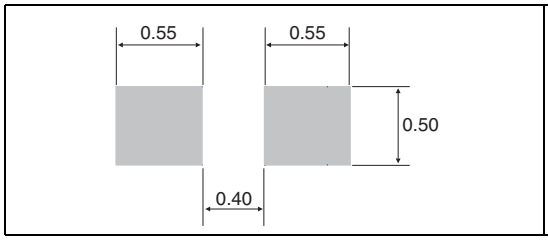
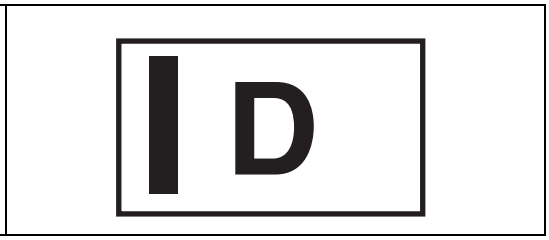
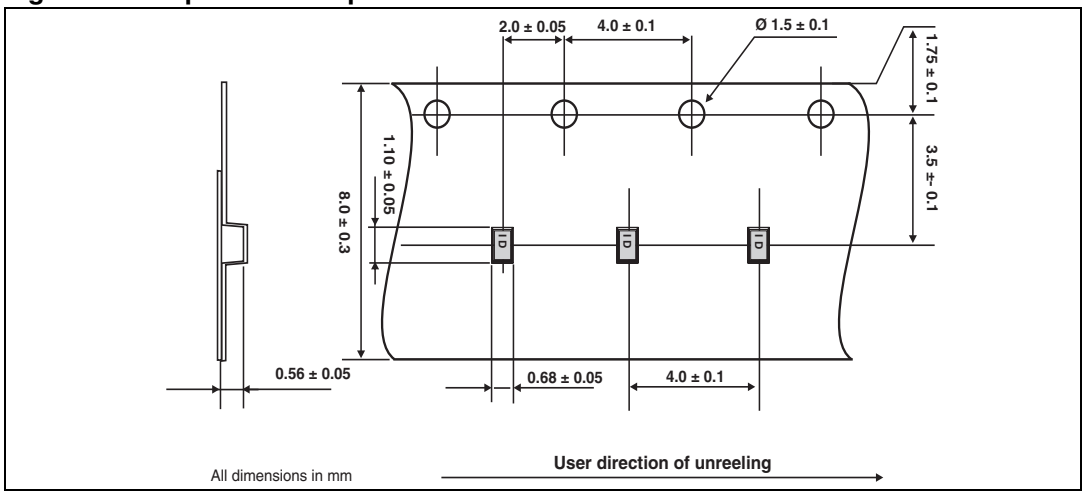



**Figure 7. Marking**




*Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.*

**Figure 8. Tape and reel specifications**

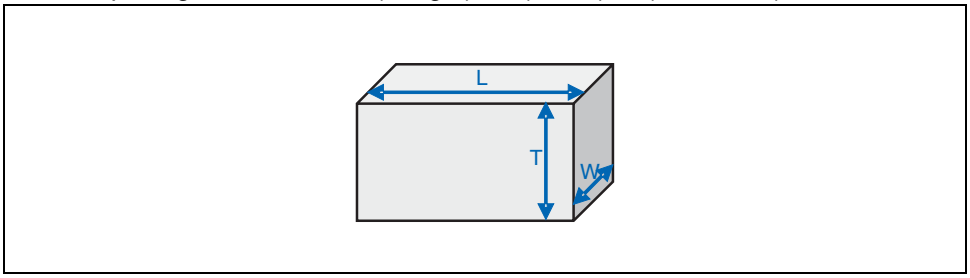



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

# 5 Recommendation on PCB assembly

## 5.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil Opening Dimensions: L (Length), W (Width), T (Thickness).




   b) General Design Rule

   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

## 5.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

## 5.3 Placement

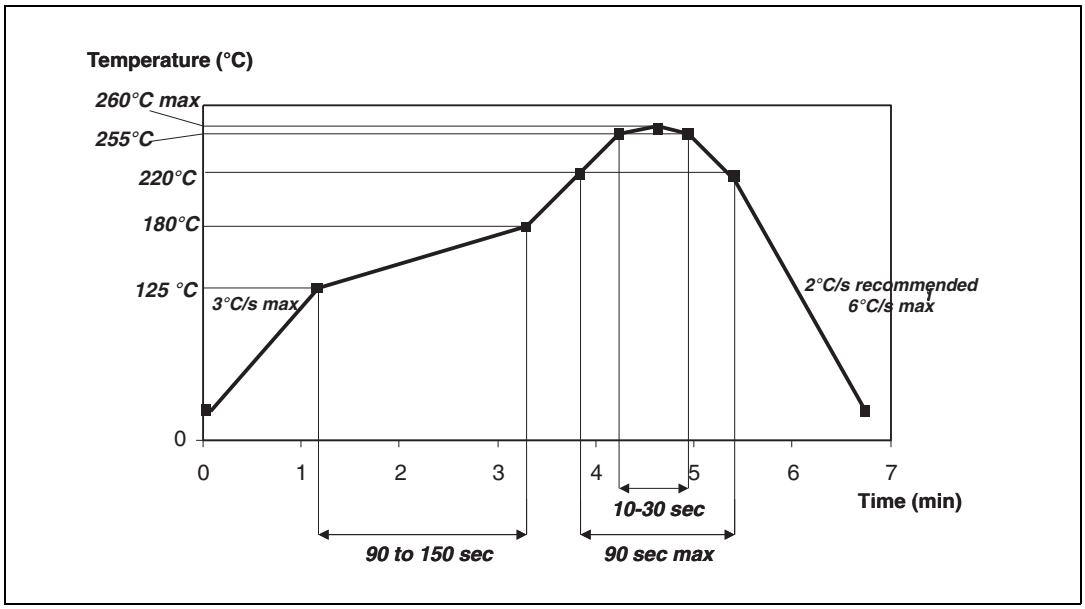
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 5.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

## 5.5 Reflow profile

ST Ecopack® recommended soldering reflow profile for PCB mounting




*Note: Minimize air convection currents in the reflow oven to avoid component movement.*

# 6 Ordering information

| Part number | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| ESDARF01-1BM2 | D | SOD882 | 0.9 mg | 3000 | Tape and reel |

# 7 Revision history

| Date | Revision | Changes |
|---|---|---|
| 17-Apr-2007 | 1 | First issue |

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