## Features

- 5.8 GHz Transceiver
- 5 dBm TX Output Power
- –97 dBm Sensitivity
- 1152 kBit/s Data-rate
- Supply-voltage Range 2.9V to 3.6V
- Low IF Receiver
- Low Current Consumption
- Few Low Cost External Components
- No Mechanical Adjustment Required
- Small 32 pin 5 mm × 5 mm QFN Package

## Applications

- 5.8 GHz Digital Cordless Phones
- Game Controllers
- Wireless Head Set
- FCC Part 15 Compliant Radio Link

## 1. Description

The ATR2820 is a single chip RF-transceiver for applications in the 5.8 GHz ISM band. The QFN32 packaged IC is a complete transceiver including image rejection mixer, low IF filter, FM demodulator, RSSI, TX preamplifier, integrated PLL with fully integrated VCO. No mechanical adjustment is necessary in production.

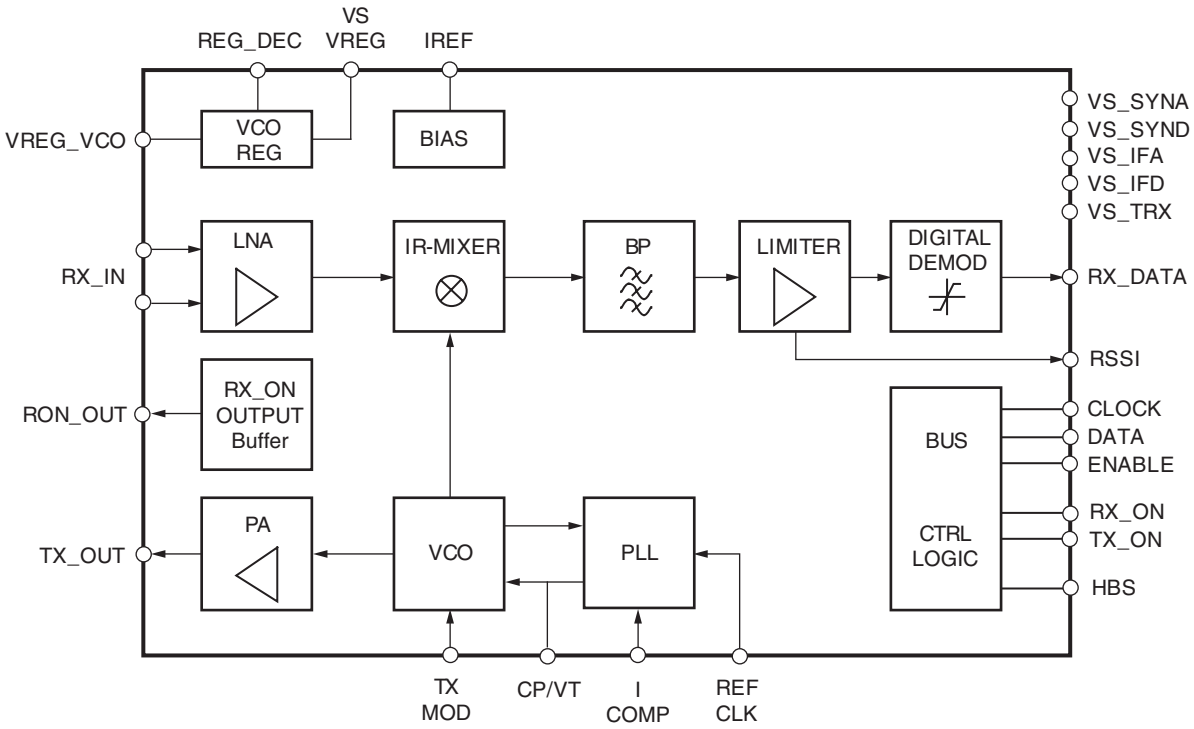
# Low IF WDCT 5.8 GHz Transceiver

# ATR2820

# Preliminary

4704D–DECT–11/06

**Figure 1-1.** Block Diagram




## 2. Pin Configuration

**Figure 2-1.** Pinning QFN32 – 5 mm × 5 mm

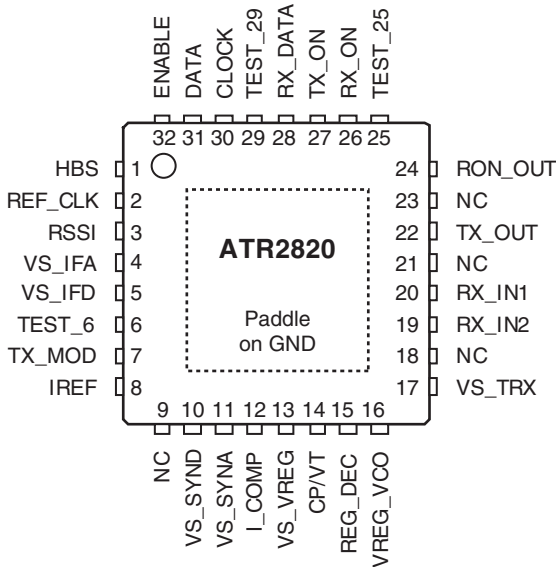


**Table 2-1.** Pin Description

| Pin | Symbol | Function |
|---|---|---|
| Paddle | GND | Ground |
| 1 | HBS | Handset/Basemode select: High = Basemode; Low = Handsetmode |
| 2 | REF_CLK | Reference frequency input |
| 3 | RSSI | Received signal strength indicator output |
| 4 | VS_IFA | Supply voltage for analog part of the IF circuit |
| 5 | VS_IFD | Supply voltage for digital part of the IF circuit |
| 6 | TEST_6 | Test pin |
| 7 | TX_MOD | Input for analog TX data signal |
| 8 | IREF | External resistor for bias circuit |
| 9 | NC | Not connected |
| 10 | VS_SYND | Supply voltage for digital part of the PLL |
| 11 | VS_SYNA | Supply voltage for analog part of the PLL |
| 12 | I_COMP | External resistor for compensation current reference |
| 13 | VS_VREG | Supply voltage for VCO voltage regulator |
| 14 | CP/VT | Charge-pump output / VCO tuning voltage input |
| 15 | REG_DEC | Decoupling pin for VCO voltage regulator |
| 16 | VREG_VCO | VCO voltage regulator output |
| 17 | VS_TRX | Supply voltage for transmitter and receiver |
| 18 | NC | Not connected |
| 19 | RX_IN2 | Differential receiver input 2 |
| 20 | RX_IN1 | Differential receiver input 1 |
| 21 | NC | Not connected |
| 22 | TX_OUT | TX driver amplifier output |
| 23 | NC | Not connected |
| 24 | RON_OUT | RXON output |
| 25 | TEST_25 | Test pin |
| 26 | RX_ON | RX control input |
| 27 | TX_ON | TX control input |
| 28 | RX_DATA | RX data output |
| 29 | TEST_29 | Test pin |
| 30 | CLOCK | 3-wire-bus: Clock input |
| 31 | DATA | 3-wire-bus: Data input |
| 32 | ENABLE | 3-wire-bus: Enable input |

**Table 2-2.** Pin Description Input/Output Circuits

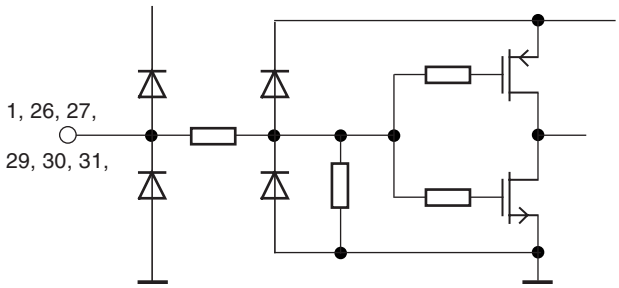
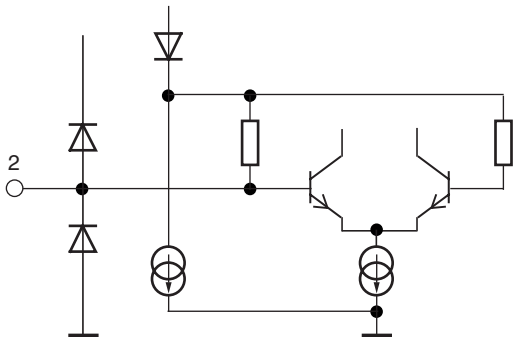
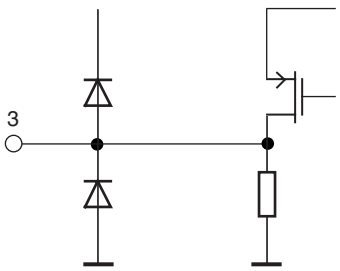
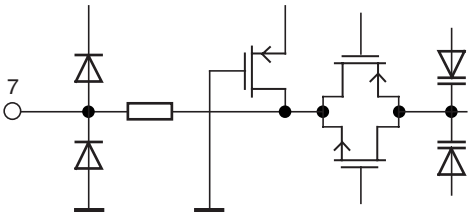
| Pin | Symbol | Function | Configuration |
|---|---|---|---|
| Paddle | GND | Ground | |
| 1<br>26<br>27<br>29<br>30<br>31 | HBS<br>RX_ON<br>TX_ON<br>TEST_29<br>CLOCK<br>DATA | Digital Input<br>(internal pull down resistor) |  |
| 2 | REF_CLK | Reference frequency input |  |
| 3 | RSSI | Receive signal strength indicator output |  |
| 4 | VS_IFA | Supply voltage for analog part of the IF circuit | |
| 5 | VS_IFD | Supply voltage for digital part of the IF circuit | |
| 6 | TEST_6 | Test pin | |
| 7 | TX_MOD | Modulation input for analog TX data |  |

**Table 2-2.** Pin Description Input/Output Circuits

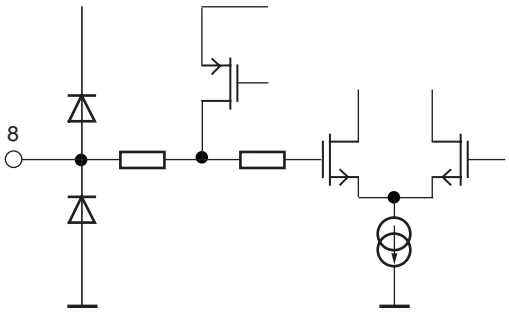
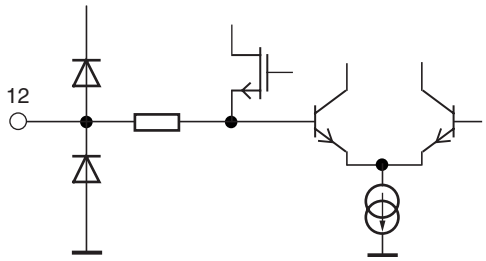
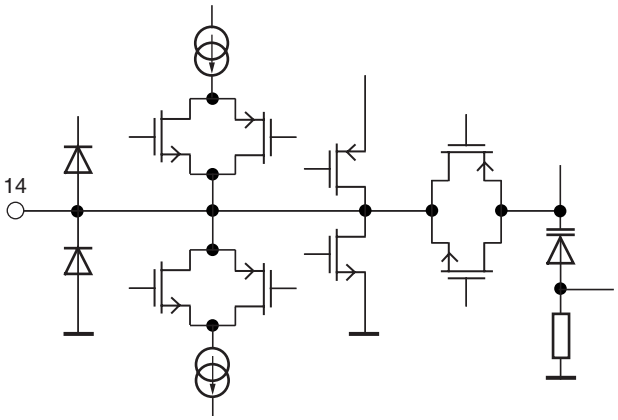
| Pin | Symbol | Function | Configuration |
|---|---|---|---|
| 8 | IREF | External resistor for bias circuit |  |
| 9 | NC | Not connected | |
| 10 | VS_SYND | Supply voltage for digital part of the PLL | |
| 11 | VS_SYNA | Supply voltage for analog part of the PLL | |
| 12 | I_COMP | External resistor for compensation current reference |  |
| 13 | VS_VREG | Supply voltage for VCO voltage regulator | |
| 14 | CP/VT | Charge-pump output / VCO tuning voltage input |  |

**Table 2-2.** Pin Description Input/Output Circuits

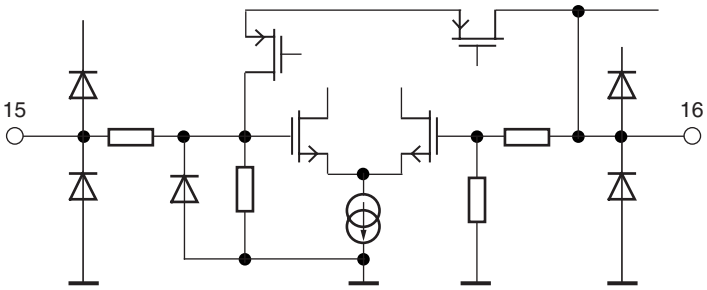
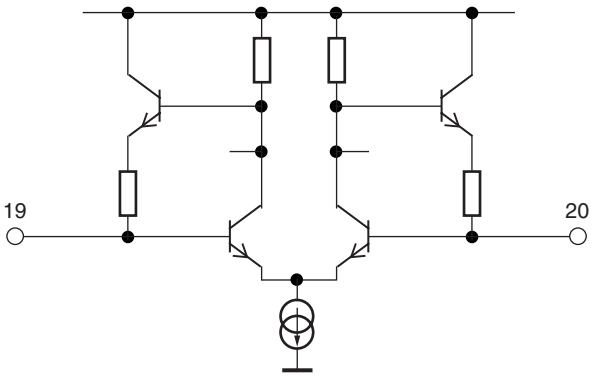
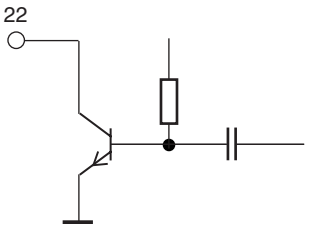
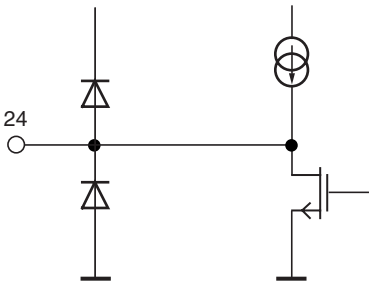
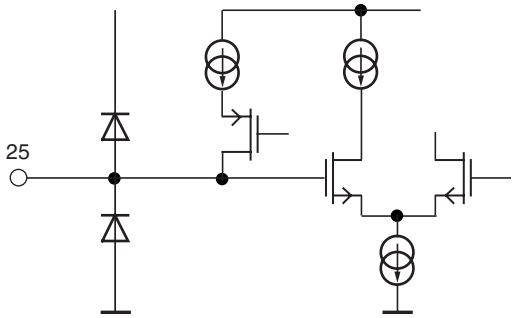
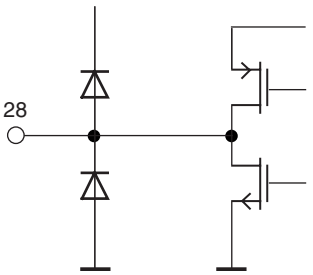
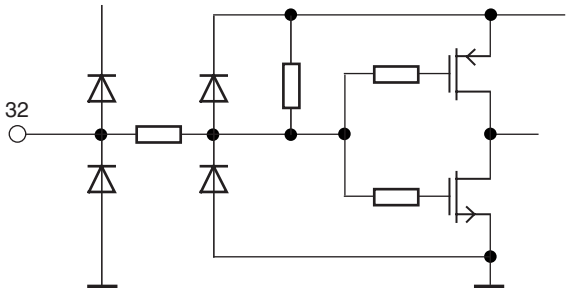
| Pin | Symbol | Function | Configuration |
|---|---|---|---|
| 15<br>16 | REG_DEC<br>VREG_VCO | Decoupling pin for VCO_REG<br>VCO voltage regulator output |  |
| 17 | VS_TRX | Supply voltage for transmitter receiver | |
| 18 | NC | Not connected | |
| 19<br>20 | RX_IN2<br>RX_IN1 | Differential receiver input 2<br>Differential receiver input 1 |  |
| 21 | NC | Not connected | |
| 22 | TX_OUT | TX driver amplifier output |  |
| 23 | NC | Not connected | |
| 24 | RON_OUT | RXON output |  |

**Table 2-2.** Pin Description Input/Output Circuits

| Pin | Symbol | Function | Configuration |
|---|---|---|---|
| 25 | TEST_25 | Test input |  |
| 28 | RX_DATA | RX data output |  |
| 32 | ENABLE | 3-wire-bus: Enable input<br>(internal pullup resitor) |  |

# 3. Functional Description

## 3.1 General

The 5.8 GHz transceiver supports a data rate of 1152 kBit/s.

## 3.2 Transmitter

The analog transmit data at TX_MOD (externally Gaussian filtered) is fed to the fully integrated VCO operating at the output frequency. The VCO signal is buffered by an internal preamplifier PA. This preamplifier supplies typically 5 dBm output power at TX_OUT.

## 3.3 Receiver

The receiver consists of an LNA followed by the IR_MIXER. The IR_MIXER is driven by a 0/90 degree phase shifter from the VCO. The channel filtering of the IF signal (1.728 MHz) is done in the active polyphase filter. After a limiting amplifier the signal is converted from analog to digital by an ADC. Digital signal processing extracts the frequency information and delivers receive data.

## 3.4 PLL

The PLL consists of a 8 bit main counter, a 5 bit swallow counter with a 32/33 modulus prescaler. The frequency/phase detector comparison frequency is 864 kHz. Open loop modulation is supported.

The VCO is fully integrated, using on-chip inductors and varactors. The output signal is buffered to the TX_PA, 0/90 degree phase shifter for the IR_MIXER and to the modulus prescaler of the PLL.

## 3.5 Serial Bus Programming

The transceiver is programmed by the 3-wire bus (CLOCK, DATA and ENABLE). After setting enable signal to low condition, on the rising edge of the clock signal, the data is transferred bit by bit into the shift register, starting with the MSB-bit. When the enable signal has returned to high condition, the programmed information is active. Additional leading bits are ignored and there is no check made about the number of clock pulses during enable low condition.

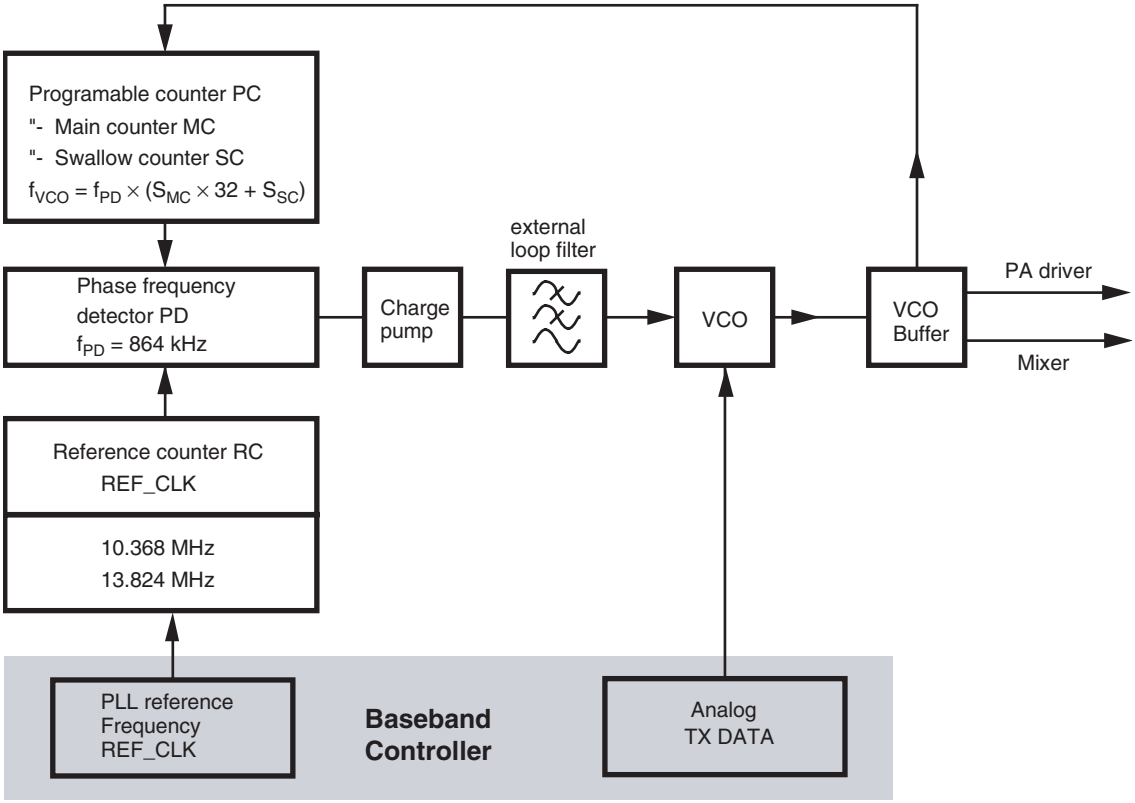
The programming of the transceiver is done by a 16 bit data word in Normal Mode or by a 24 bit data word in Enhanced Mode. Normal Mode uses TX_ON respectively RX_ON pin to switch on the TX respectively RX blocks. The Enhanced Mode does this internally by programming the delay time bits D16 to D23.

## 3.6 Power Supply

An integrated bandgap-stabilized voltage regulator supplies the VCO. Power up state is activated by the first rising edge of the CLOCK signal on the 3-wire bus interface. Power down state is activated either on the rising edge of the ENABLE signal on the 3-wire bus interface (Enhanced Mode) or by the falling edge of the TX_ON resp. RX_ON control signal (Normal Mode).

If the transceiver supply voltage is switched off e.g., by means of an external regulator, all digital inputs must be kept on low level to insure the low standby current and not to provide supply current via the ESD protection devices.

**Figure 3-1.** PLL Principle




The following table shows the possible LO frequencies for RX and TX in the 5.8 GHz ISM band. There are 142 channels available. Every second channel can be used without overlap in the spectrum.

**Table 3-1.** Channel Table

| Mode | $f_{IF}$/kHz | Channel | $f_{ANT}$/MHz | $f_{VCO}$/MHz | $S_{MC}$ | $S_{SC}$ | N |
|---|---|---|---|---|---|---|---|
| TX | – | C0 | 5725.728 | 5725.728 | 207 | 3 | 6627 |
| | | C1 | 5726.592 | 5726.592 | 207 | 4 | 6628 |
| | | ... | ... | ... | ... | ... | ... |
| | | C140 | 5846.688 | 5846.688 | 211 | 15 | 6767 |
| | | C141 | 5847.552 | 5847.552 | 211 | 16 | 6768 |
| RX | 1728 | C0 | 5725.728 | 5727.456 | 207 | 5 | 6629 |
| | | C1 | 5726.592 | 5728.320 | 207 | 6 | 6630 |
| | | ... | ... | ... | ... | ... | ... |
| | | C140 | 5846.688 | 5848.416 | 211 | 17 | 6769 |
| | | C141 | 5847.552 | 5849.280 | 211 | 18 | 6770 |

Formula:

TX: $f_{ANT} = f_{VCO} = 864\ kHz \times (32 \times S_{MC} + S_{SC})$
RX: $f_{ANT} = 864\ kHz \times (32 \times S_{MC} + S_{SC} - 2)$

## 3.7 Bus Protocol Formats

### 3.7.1 Normal Mode

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Byte2 | | | | | | | | Byte1 | | | | | | | |
| Data bits | | | | | | | | | | | | | | | |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | DR | 0 | 0 | 0 | TX | RC | MC | | | SC | | | | |

### 3.7.2 Enhanced Mode

| MSB | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Byte3 | | | | | | | | Byte2 | | | | | | | | Byte1 | | | | | |
| Data bits | | | | | | | | | | | | | | | | | | | | | |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DELAY | | | | | | | | 1 | 1 | DR | 0 | 0 | 0 | TX | RC | MC | | | SC | | | | |

### 3.7.3 PLL Settings

RC, MC and SC bits are controlling the PLL frequency according to Table 3-2, Table 3-3 and Table 3-4.

**Table 3-2.** Reference Counter Bit D8

| RC (Reference Counter) | |
|---|---|
| **D8** | **REF_CLK** |
| 0 | 10.368 MHz |
| 1 | 13.824 MHz |

**Table 3-3.** Main Counter Bits D5-D7

| MC (Main Counter) | | | |
|---|---|---|---|
| **D7** | **D6** | **D5** | **$S_{MC}$** |
| 0 | 0 | 0 | 206 |
| 0 | 0 | 1 | 207 |
| 0 | 1 | 0 | 208 |
| 0 | 1 | 1 | 209 |
| 1 | 0 | 0 | 210 |
| 1 | 0 | 1 | 211 |
| 1 | 1 | 0 | 212 |
| 1 | 1 | 1 | 213 |

**Table 3-4.** Swallow Counter Bits D0-D4

| SC (Swallow Counter) | | | | | |
|---|---|---|---|---|---|
| **D4** | **D3** | **D2** | **D1** | **D0** | **$S_{SC}$** |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 2 |
| ... | ... | ... | ... | ... | ... |
| 1 | 1 | 1 | 0 | 1 | 29 |
| 1 | 1 | 1 | 1 | 0 | 30 |
| 1 | 1 | 1 | 1 | 1 | 31 |

### 3.7.4 TX Mode ON/OFF

The TX bit is used to prepare the ATR2820 for a TX or RX slot. The transmit or receive mode is later activated by the TX_ON respectively RX_ON signal.

**Table 3-5.** With Bit D9

| D9 | TRX |
|---|---|
| 0 | RX |
| 1 | TX |

### 3.7.5 Data Recovery

The DR bit switches the internal data recovery circuit on.

**Table 3-6.** With Bit D13

| D13 | Data Recovery |
|---|---|
| 0 | off |
| 1 | on |

### 3.7.6 TX_ON / RX_ON Delay for Enhanced Interface Mode

The DELAY bits set the internal delay time. The delay counter is starting with the ENABLE high edge at the end of the programming.

Delay Time: $T_{Delay}$ = DELAY $\times$ 2.315 µs

The minimum delay time is 70 µs, which corresponds to a Delay value of 31.

**Table 3-7.** Delay Setting

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | DELAY |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 32 |
| ... | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 |

## 3.8 3-wire Bus Protocol Timing

**Figure 3-2.** 3-wire Bus Protocol Timing Diagram

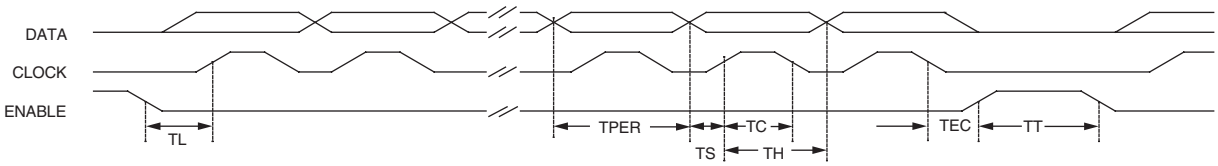



**Table 3-8.** 3-wire bus Protocol Table

| Description | Symbol | Minimum Value | Unit |
|---|---|---|---|
| Clock period | TPER | 100 | ns |
| Set time data to clock | TS | 20 | ns |
| Hold time data to clock | TH | 20 | ns |
| Clock pulse width | TC | 60 | ns |
| Set time enable to clock | TL | 100 | ns |
| Hold time enable to data | TEC | 0 | ns |
| Time between two protocols | TT | 250 | ns |

## 3.9 Control Signals

**Table 3-9.** Control Signals – Functions

| Signal | Functions |
|---|---|
| RX_ON (external or internal signal) | Activates RX circuits: LNA, IR MIXER, BP, LIMITER, DEMOD |
| TX_ON (external or internal signal) | Activates TX circuit: PA |
| HBS | Selects the handset or basemode: Low = Handset, High = Basemode |

## 4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply voltage | $V_S$ | –0.3 | +3.6 | V |
| Control voltages | $V_{contr}$ | –0.3 | $V_S$ | V |
| Junction temperature | $T_{jmax}$ | | 125 | °C |
| Storage temperature | $T_{stg}$ | –40 | +125 | °C |
| Input RF level | $P_{RF}$ | | 10 | dBm |
| ESD protection | $V_{ESD\_anal}$ | | TBD | V |
| | $V_{ESD\_dig}$ | | TBD | V |

## 5. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Junction ambient | $R_{thJA}$ | TBD | K/W |

## 6. Handling

Do not operate this part near strong electrostatic fields. This IC meets class 0 ESD test requirement (HBM in accordance to EIA/JESD22-A114-A (October 97).

## 7. Operating Range

| Parameters | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply voltage | $V_S$ | 2.9 | 3.6 | V |
| Temperature ambient | $T_{amb}$ | –10 | +60 | °C |

# 8. Electrical Characteristics

$V_S$ = 3.2V, $T_{amb}$ = 25°C, unless otherwise specified.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| Supply voltage | | $V_S$ | 2.9 | 3.2 | 3.6 | V | D |
| PLL supply current | | $I_S$ | | 25 | | mA | A |
| RX supply current | | $I_S$ | | 65 | | mA | A |
| TX supply current | | $I_S$ | | 22 | | mA | A |
| Supply current in power-down mode | | $I_S$ | | < 1 | | µA | A |
| **PLL** | | | | | | | |
| Scaling factor prescaler | | $S_{PSC}$ | | 32/33 | | | A |
| Scaling factor main counter | | $S_{MC}$ | | 206, 207, ..., 212, 213 | | | A |
| Scaling factor swallow counter | | $S_{SC}$ | | 0 ... 31 | | | A |
| Scaling factor reference counter | RC = 0, 1 | $S_{RC}$ | | 12, 16 | | | A |
| External reference input frequency | RC = 0<br>RC = 1 | Ref_CLK | | 10.368<br>13.824 | | MHz<br>MHz | A |
| Sinusoidal input signal level | AC coupled sinewave | Ref_CLK | 500 | | 1200 | $mV_{P-P}$ | A |
| Phase detector comparison frequency | | $f_{PD}$ | | 864 | | kHz | A |
| Charge-pump output current | $V_{CP}$ = 1/2 $V_S$ | $I_{CP}$ | | ±2 | | mA | A |
| Leakage current | $V_{CP}$ = 1/2 $V_S$ | $I_L$ | | ±100 | | pA | A |
| **VCO** | | | | | | | |
| Oscillator frequency | Over full temperature range(1) | | 5725 | | 5875 | MHz | A |
| Frequency control voltage range | | $V_{VTUNE}$ | 0.5 | | $V_S$ – 0.5 | V | A |
| VCO tuning input gain | Defined at TX output(1) | $G_{VCO}$ | | 120 | | MHz/V | A |
| Modulation control voltage range | | $V_{TX\_MOD}$ | 0 | | $V_S$ | V | A |
| Modulation input gain | DC bias: $V_{TX\_MOD}$=750 mV<br>Defined at TX output(1) | $G_{TX\_MOD}$ | | 800 | | kHz/V | A |
| VCO phase noise | PN at 1 MHz offset | | | –105 | –100 | dBc/Hz | C |
| **Transmiter** | | | | | | | |
| TX data rate | | | | 1152 | | kBit/s | C |
| Frequency deviation | Analog modulation signal at TX_MOD | | | ±400 | | kHz | A |
| TX preamplifier output power | Over full temperature range, from 5725 MHz to 5875 MHz(1) | $P_{TX}$ | 0 | 5 | | dBm | A |
| TX output impedance | | $Z_{OUT}$ | | 24–j107 | | Ω | C |
| Frequency drift during a slot | 400 µs slot length | $\Delta f_{o\ (drift)}$ | | | ±20 | kHz | C |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Measured and guaranteed only on the Atmel evaluation board.

## 8. Electrical Characteristics (Continued)

$V_S$ = 3.2V, $T_{amb}$ = 25°C, unless otherwise specified.

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|
| **Receiver** | | | | | | | |
| RX input frequency range | | $f_{RX}$ | 5725 | | 5875 | MHz | C |
| RX input impedance | Differential | $Z_{IN}$ | | 94–j3 | | Ω | C |
| Sensitivity at input for BER ≤$10^{-3}$ | $f_{dev}$ = 400 kHz(1) at 1152 kBit/s | S | | –97 | | dBm | C |
| Third order input intercept point | | IIP3 | | –15 | | dBm | C |
| Intermodulation rejection | BER < $10^{-3}$, wanted at -83 dBm, level of interferers in channels N–2 and N–4(1) | $IM_3$ | 32 | | | dBc | C |
| Co-channel rejection | BER < $10^{-3}$, wanted at –76 dBm(1) | $R_{CO}$ | –11 | –7 | | dBc | C |
| Adjacent channel rejection ±1.728 MHz | BER < $10^{-3}$, wanted at –76 dBm, adjacent level referred to wanted channel level(1) | $R_{i\,(N\pm1)}$ | 13 | 19 | | dBc | C |
| Bi-adjacent channel rejection +3.456 MHz (Image frequency) –3.456 MHz | BER < $10^{-3}$, wanted at –76 dBm, bi-adjacent level referred to wanted channel level(1) | $R_{i\,(N\pm2)}$ | 13<br>34 | 19<br>43 | | dBc | C |
| Rejection with ≥ 3 channels separation ≥ ±5.128 MHz | BER < $10^{-3}$, wanted at –76 dBm, n ≥ 3 adjacent level referred to wanted channel level(1) | $R_{i\,(n\pm\geq3)}$ | 40 | 46 | | dBc | C |
| Out of band rejection > 6 MHz | BER < $10^{-3}$, wanted at –83 dBm at 5.8 GHz(1) | $BI_{df>6MHz}$ | 38 | 53 | | dBc | C |
| Out of band rejection 5670 MHz to 5690 MHz 5881 MHz to 5900 GHz | BER < $10^{-3}$, wanted at –83 dBm at 5.8 GHz(1) | $BI_{near}$ | 47 | 58 | | dBc | C |
| Out of band rejection 30 MHz to 5670 MHz 5900 MHz to 8GHz | BER < $10^{-3}$, wanted at –83 dBm at 5.8 GHz(1) | BIfar | 54 | 65 | | dBc | C |
| Maximum RSSI output voltage | Under high RX input signal level | $V_{RSSImax}$ | | 1.9 | | V | A |
| RSSI output voltage, monotonic over range –96 dBm to –36 dBm | with –33 dBm at RF input<br>with –96 dBm at RF input | $V_{RSSI}$ | | 1.7<br>0.1 | | V<br>V | A |
| Wake-up time from power-up signal to correct RSSI output | 150 pF load on RSSI output pin 3 | $T_{on}$ | | 20 | 40 | µs | C |
| **Interface Logic Input and Output Signal Levels, Pins DATA, CLOCK, ENABLE, RX_ON, TX_ON, RX_DATA, HBS** | | | | | | | |
| HIGH-level input voltage | Logic 1 | $V_{IH}$ | 1.4 | | $V_S$ | V | A |
| LOW-level input voltage | Logic 0 | $V_{IL}$ | –0.3 | | +0.4 | V | A |
| HIGH-level output voltage | Logic 1 | $V_{OH}$ | | | $V_S$ | V | A |
| LOW-level output voltage | Logic 0 | $V_{OL}$ | 0 | | | V | A |
| Input bias current | Logic 1 or logic 0 | $I_{bias}$ | –5 | | +5 | µA | A |
| Maximum 3-wire bus frequency | | $f_{CLKmax}$ | 10 | | | MHz | C |
| **Output Pin RON_OUT** | | | | | | | |
| LOW-level output voltage | $I_{SINK}$ = 10 mA | $V_{OL}$ | | | 0.5 | V | A |
| High-level output current | $V_{OL}$ = 2.7V | $I_{OL}$ | | 100 | 120 | µA | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Measured and guaranteed only on the Atmel evaluation board.

# 9. Application

**Figure 9-1.** Application Circuit

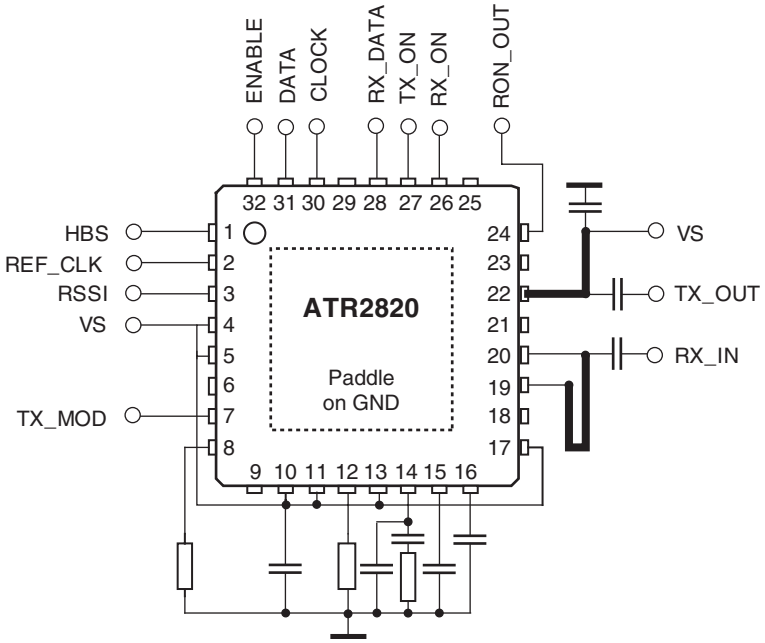
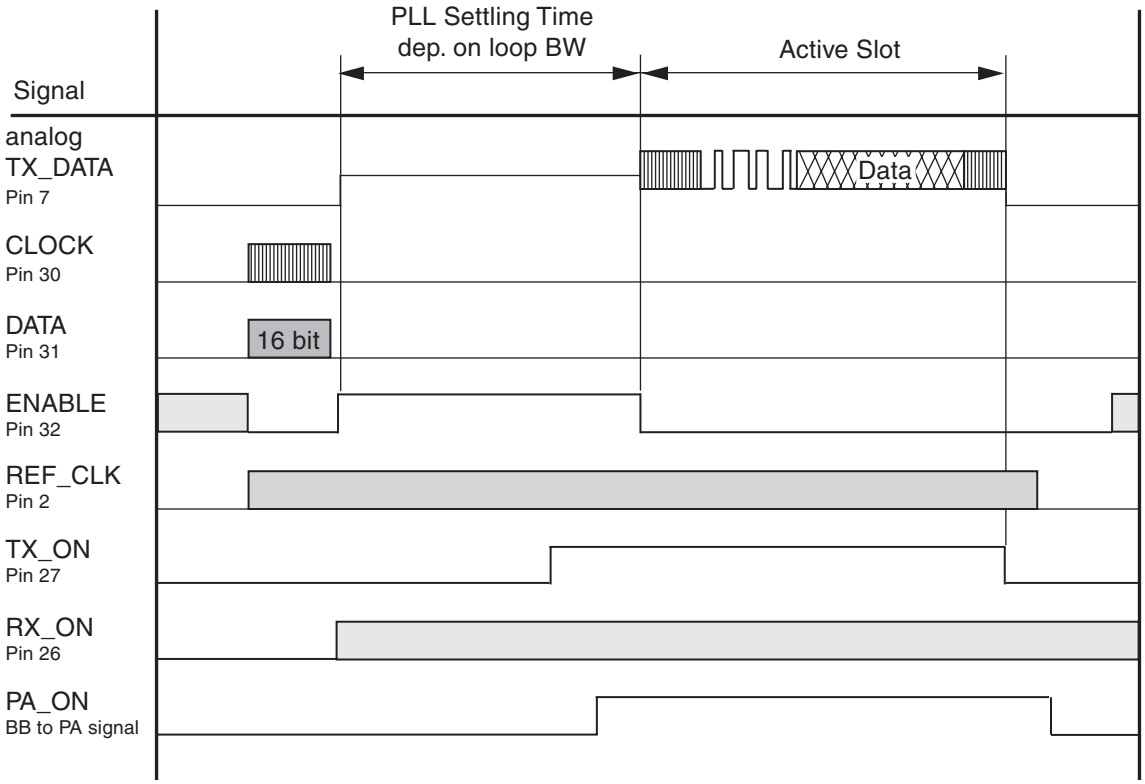


**Figure 9-2.** TX Timing (Normal Mode)



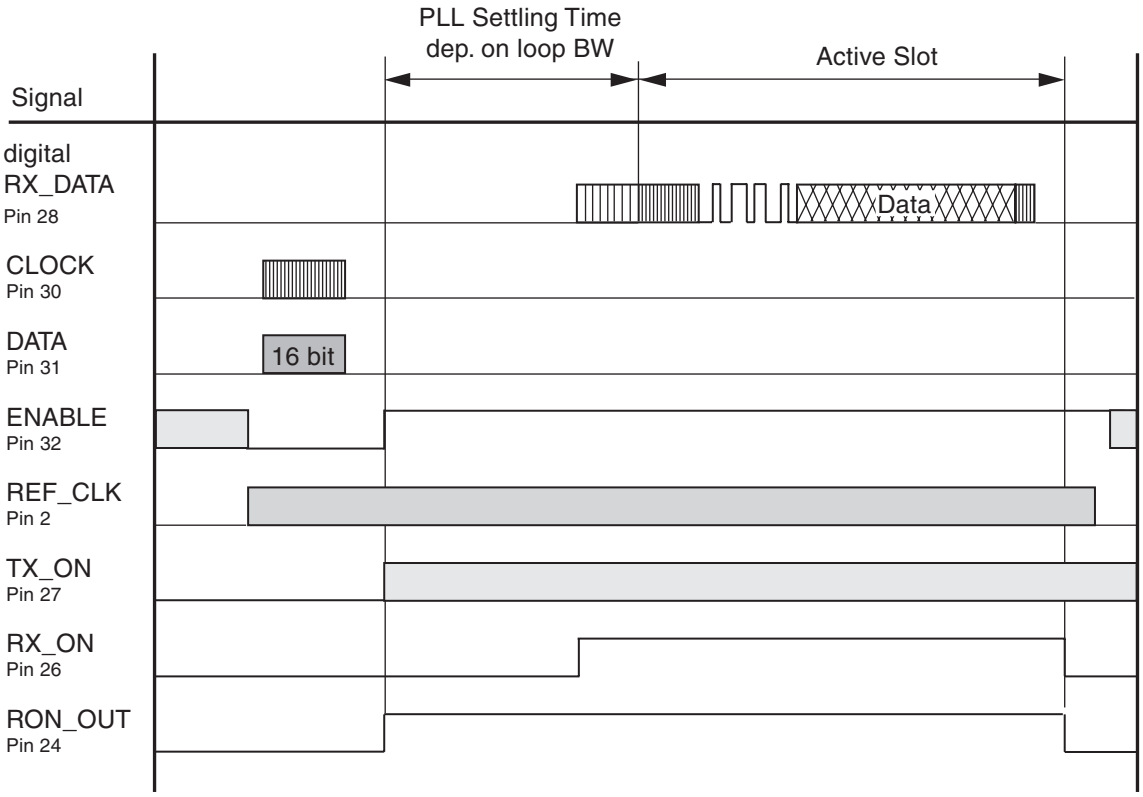

**TX Control Sequence Normal Mode:**

- Programming of 3 wire bus (16bit word)
- First rising edge of CLOCK signal activates power up mode of TRX
- TX_ON high signal (≈ 100 µs before active slot) activates TX PreAmplifier
- PA_ON high signal (≈ 50 µs before active slot) activates external Power Amplifier (e.g. ATR7040)
- ENABLE low signal activates open loop mode of PLL
- Start of Analog Modulation
- TX_ON low signal deactivates TX PreAmplifier and sets TRX in power down
- PA_ON low signal turns external Power Amplifier off

**Remark:**

- Minimum distance between different signal edges > 4 µs
- REF_CLK must be active before the first CLOCK edge and at least 4 us after TX_ON low signal

**Figure 9-3.** RX Timing (Normal Mode)



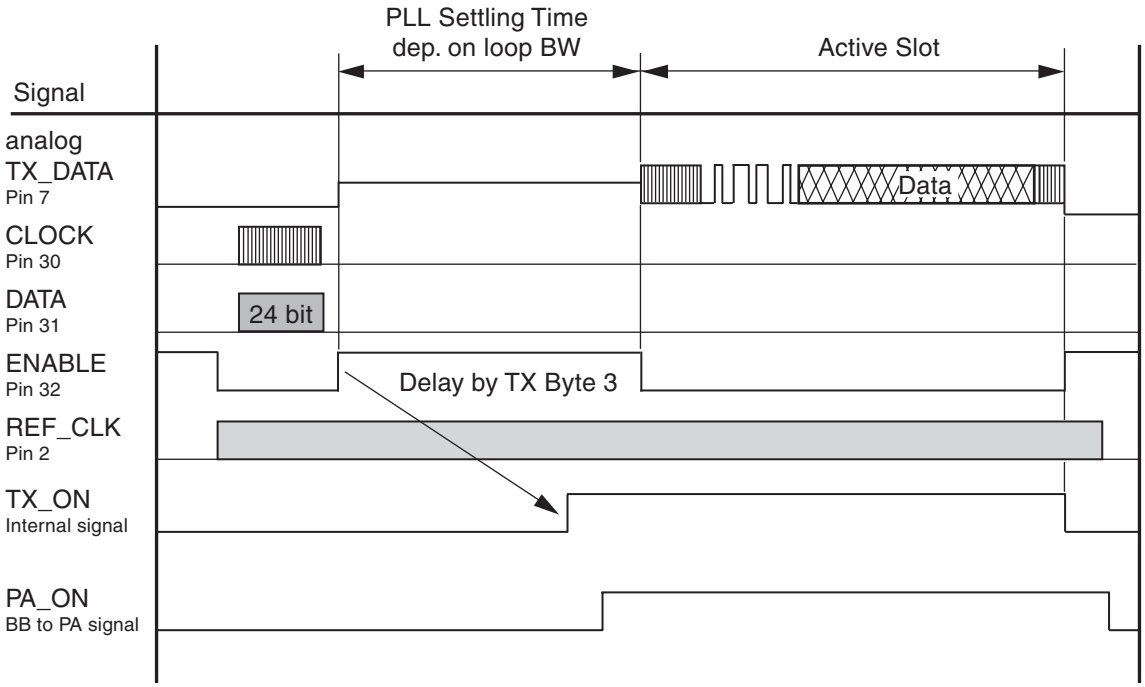

**RX Control Sequence Normal Mode:**

- Programming of 3 wire bus (16 bit word)
- First rising edge of CLOCK signal activates power up mode of TRX
- RON_OUT output signal can be used to switch external LNA on
- RX_ON high signal (≈ 50 µs before active slot) activates RX blocks
- RX_DATA (digital) is delivered 25 µs after RX_ON high
- RX_ON low signal deactivates RX blocks and sets TRX in power down

**Remark:**

- Minimum distance between different signal edges > 4 µs
- REF_CLK must be active before the first CLOCK edge and at least 4 us after TX_ON low signal

**Figure 9-4.** TX Timing (Enhanced Mode)



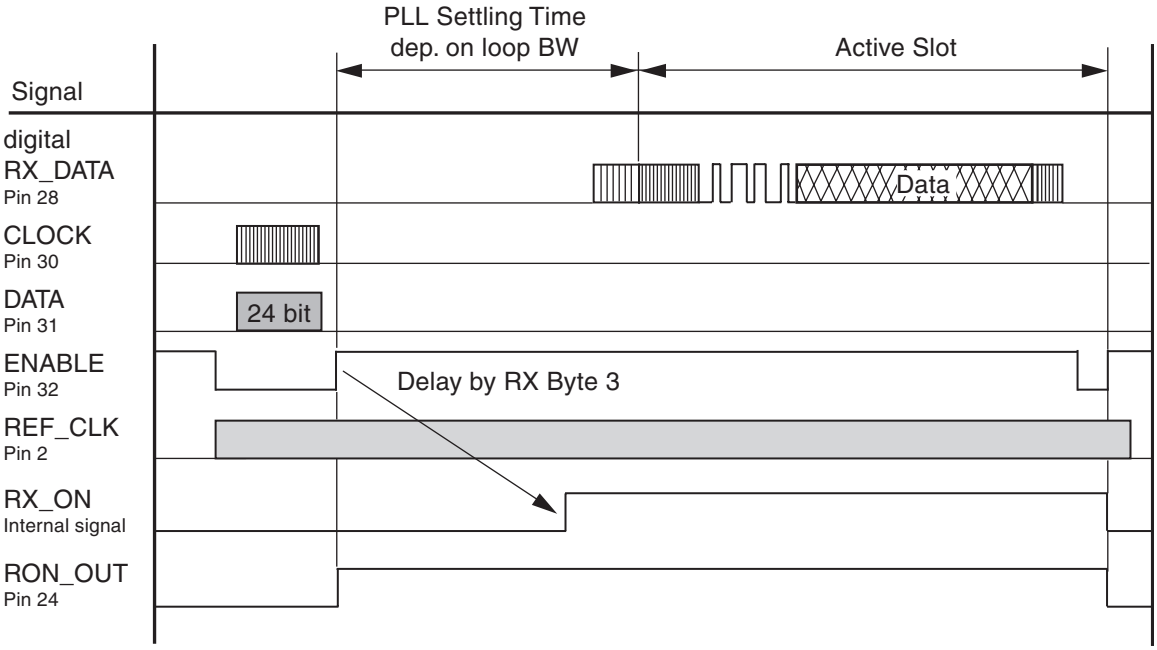

**TX Control Sequence Enhanced Mode:**

- Programming of 3 wire bus (24 bit word)
- First rising edge of CLOCK signal activates power up mode of TRX
- Internal TX_ON high signal (≈ 100 µs before active slot defined by TX Byte 3) activates TX PreAmplifier
- PA_ON high signal (≈ 50 µs before active slot) activates external Power Amplifier (e.g. ATR7040)
- ENABLE low signal activates open loop mode of PLL
- Start of Analog Modulation
- ENABLE high signal deactivates TX PreAmplifier and sets TRX in power down
- PA_ON low signal turns external Power Amplifier off

**Remark:**

- Minimum distance between different signal edges > 4 µs
- REF_CLK must be active before the first CLOCK edge and at least 4 µs after ENABLE high signal

**Figure 9-5.** RX Timing (Enhanced Mode)




**RX Control Sequence Enhanced Mode:**

- Programming of 3 wire bus (24 bit word)
- First rising edge of CLOCK signal activates power up mode of TRX
- RON_OUT output signal can be used to switch external LNA on
- Internal RX_ON high signal (≈ 50 µs before active slot defined by RX Byte 3) activates RX blocks
- RX_DATA (digital) is delivered 25 µs after internal RX_ON high
- Rising edge of ENABLE low pulse signal deactivates RX blocks and sets TRX in power down

**Remark:**

- Minimum distance between different signal edges > 4 µs
- REF_CLK must be active before the first CLOCK edge and at least 4 µs after TX_ON low signal

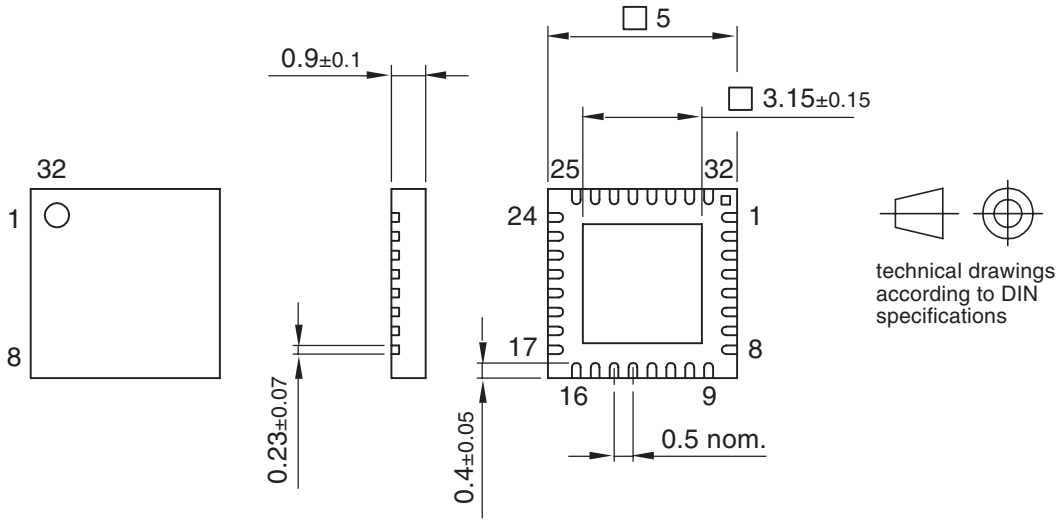
## 10. Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| ATR2820-PNQG | QFN32, 5 mm × 5 mm | Taped and reeled |

## 11. Package Information

Package: QFN 32 - 5 x 5
Exposed pad 3.15 x 3.15
(acc. JEDEC OUTLINE No. MO-220)

Dimensions in mm

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