PRELIMINARY

Integrated Circuit Systems, Inc.

ICS889874

1:2 DIFFERENTIAL-TO-LVPECL BUFFER/DIVIDER

GENERAL DESCRIPTION

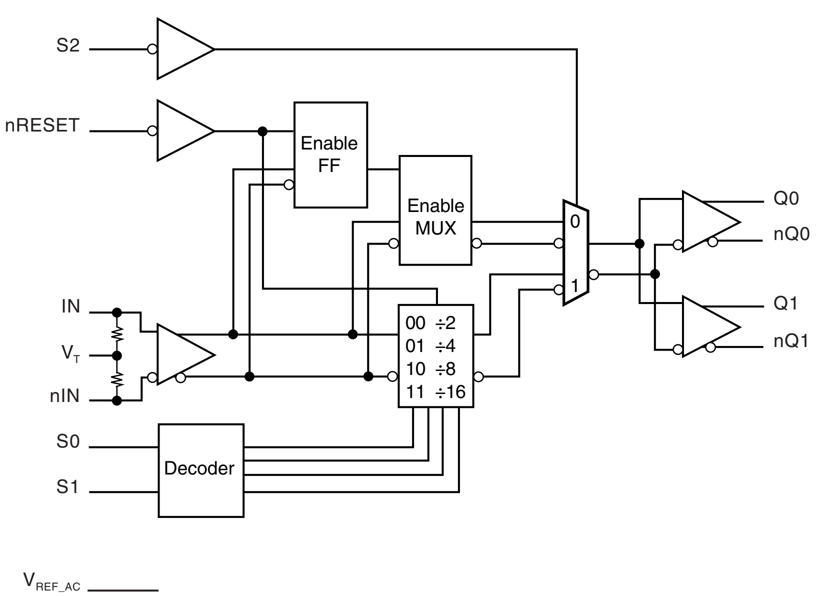
ICS HiPerClockS™

The ICS889874 is a high speed 1:2 Differential-to-LVPECL Buffer/Divider and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. The ICS889874 has a selectable ÷1, ÷2, ÷4, ÷8, ÷16 output divider, which allows the device to be used as either a 1:2 fanout buffer or frequency divider. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

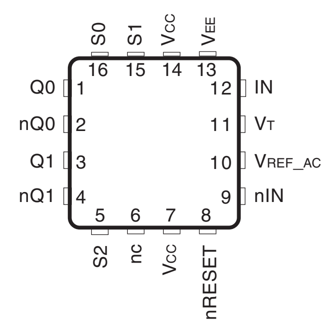
FEATURES

- 2 LVPECL outputs
- Frequency divide select options: ÷ 1, ÷ 2, ÷4, ÷8, ÷16
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: > 2.5GHz
- Output skew: 5ps (typical)
- Part-to-part skew: TBD
- Additive jitter, RMS: <0.03ps (design target)
- Supply voltage range: (LVPECL), 2.375V to 3.465V
  Supply voltage range: (ECL), -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Pin compatible with SY89874U

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS889874
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL / ECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL / ECL interface levels.
5, 15, 16	S2, S1, S0	Input	Pullup	Select pins. LVCMOS/LVTTL interface levels.
6	nc	Unused		No connect.
7, 14	V_{CC}	Power		Positive supply pins.
8	nRESET	Input	Pullup	Synchronizing enable/disable pin. When LOW, resets the divider. When HIGH, unconnected. Input threshold is V_{CC}/2V. Includes a 37kΩ pull-up resistor. LVTTL / LVCMOS interface levels.
9	nIN	Input		Inverting differential LVPECL clock input.
10	V_{REF_AC}	Output		Reference voltage for AC-coupled applications.
11	V_T	Input		Termination input.
12	IN	Input		Non-inverting LVPECL differential clock input.
13	V_{EE}	Power		Negative supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs		Outputs	
nRESET	**Selected Source**	**Q0, Q1**	**nQ0, nQ1**
0	IN, nIN	Disabled; LOW	Disabled; HIGH
1	IN, nIN	Enabled	Enabled

NOTE: After nRESET switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.*

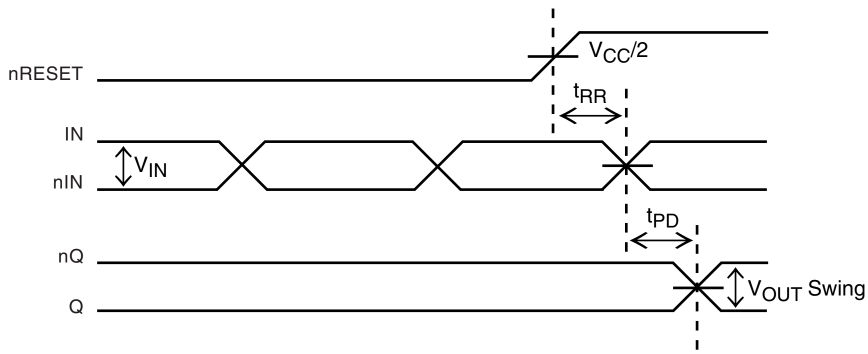


FIGURE 1. nRESET TIMING DIAGRAM (WHEN S2 = 1)

TABLE 3B. TRUTH TABLE

Inputs				Outputs
nRESET	**S2**	**S1**	**S0**	
1	0	X	X	Reference Clock (pass through)
1	1	0	0	Reference Clock ÷2
1	1	0	1	Reference Clock ÷4
1	1	1	0	Reference Clock ÷8
1	1	1	1	Reference Clock ÷16
0	1	X	X	Q = LOW, nQ = HIGH Clock Disable; (NOTE 1)
0	0	X	X	Q = LOW, nQ = HIGH Clock Disable; (NOTE 1)

NOTE 1: Reset/Disable function is asserted on the next clock input (IN/nIN) high-to-low transition.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.5V to +4.0V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Input Current IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
V_{REF_AC} Sink/Source, I_{VREF_AC}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±10% OR 2.5V±5%; TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.63	V
I_{EE}	Power Supply Current			50		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±10% OR 2.5V±5%; TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		0		0.8	V
I_{IH}	Input High Current	$V_{CC} = V_{IN}$ = 3.63V	-125		20	µA
I_{IL}	Input Low Current	V_{CC} = 3.63V, V_{IN} = 0V			-300	µA

TABLE 4C. DC CHARACTERISTICS, V_{CC} = 3.3V±10% OR 2.5V±5%; TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	(IN, nIN)			100		Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{CC} - 0.15	V
V_{IN}	Input Voltage Swing			0.15		2.8	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I_{IN}	Input Current	(IN, nIN)				45	mA
V_{REF_AC}	Bias Voltage				V_{CC} - 1.35		V

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±10% OR 2.5V±5%; TA = -40°C TO 85°C

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1			V_{CC} - 1.005		mV
V_{OL}	Output Low Voltage; NOTE 1			V_{CC} - 1.78		mV
V_{OUT}	Output Voltage Swing			800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing			1.60		V

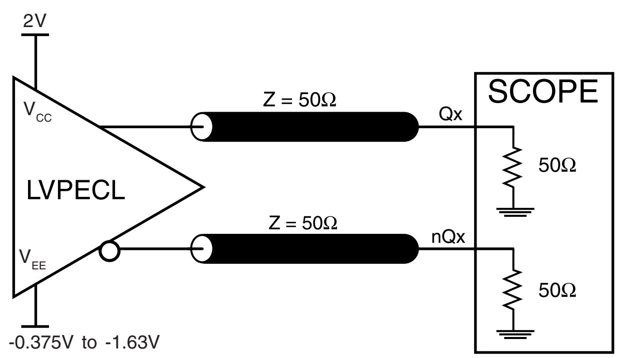
Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±10% OR 2.5V±5%; TA = -40°C TO 85°C

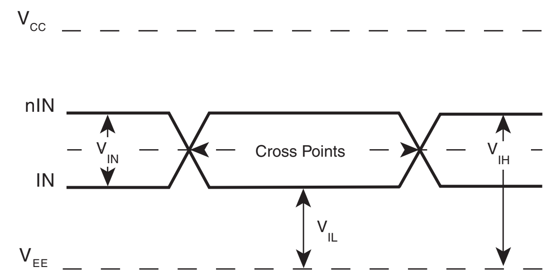
Symbol	Parameter		Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency		Output Swing ≥ 450mV	2			GHz
	Maximum Input Frequency		÷ 2, ÷4, ÷8, ÷16	2			GHz
t_{PD}	Propagation Delay, (Differential); NOTE 1		Input Swing: < 400mV		725		ps
			Input Swing: ≥ 400mV		725		ps
*t*sk(o)	Output Skew; NOTE 2, 4				5		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				TBD		ps
*t*jit	Additive Phase Jitter, RMS; refer to Additive Phase Jitter section				<0.03		ps
t_{RR}	Reset Recovery Time				TBD		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%		180		ps
t_S	Clock Enable Setup Time	EN to IN, nIN			TBD		ps
t_H	Clock Enable Hold Time	EN to IN, nIN			TBD		ps

All parameters characterized at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

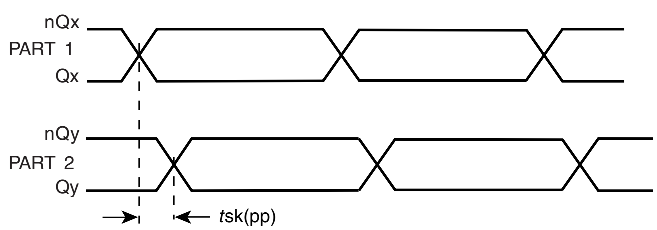
PARAMETER MEASUREMENT INFORMATION



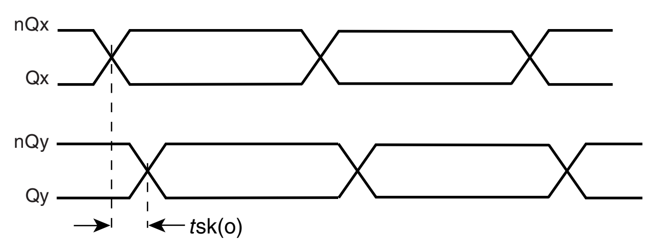
OUTPUT LOAD AC TEST CIRCUIT



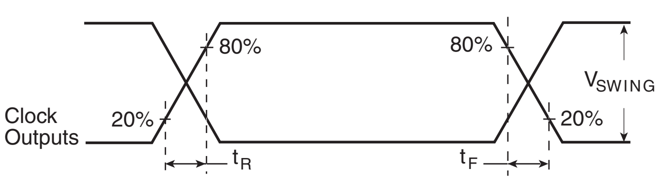
DIFFERENTIAL INPUT LEVEL



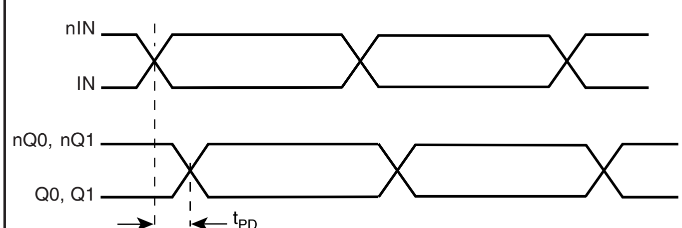
PART-TO-PART SKEW



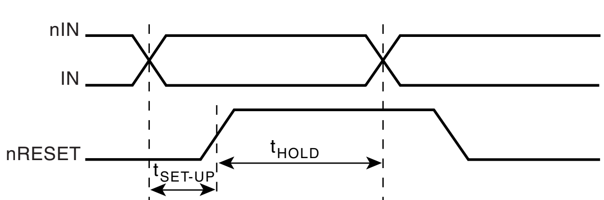
OUTPUT SKEW



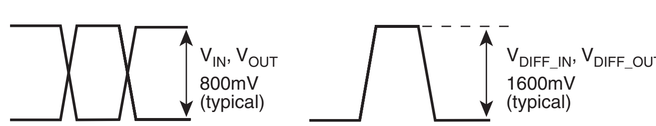
OUTPUT RISE/FALL TIME



PROPAGATION DELAY



SETUP & HOLD TIME



SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING

APPLICATION INFORMATION

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

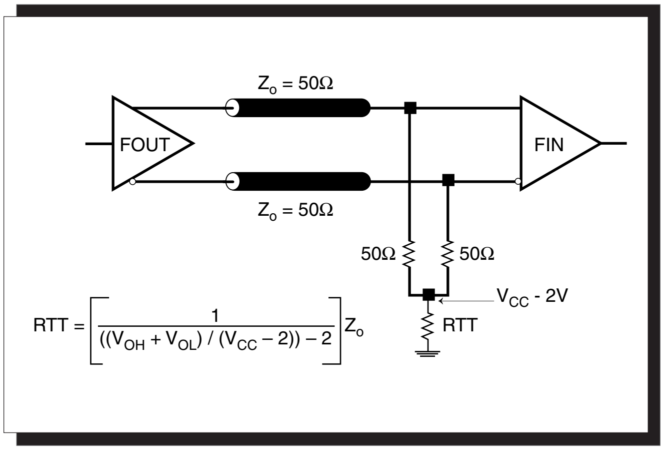


FIGURE 2A. LVPECL OUTPUT TERMINATION

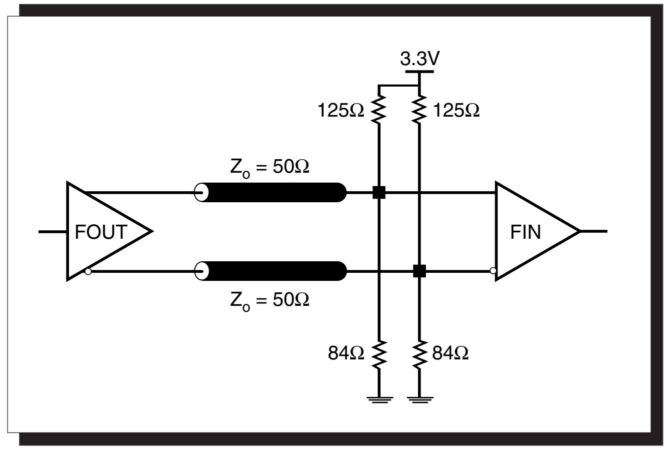


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

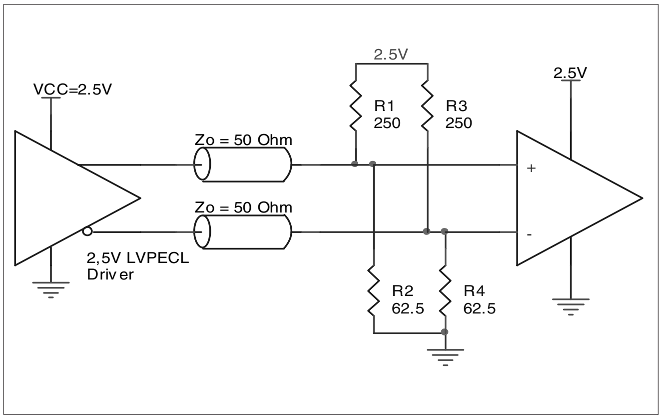


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

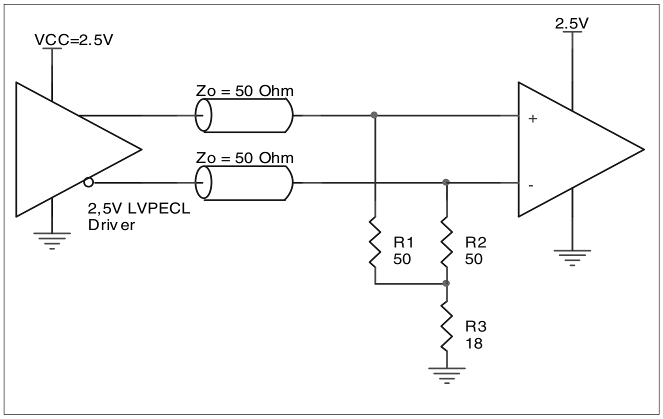


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

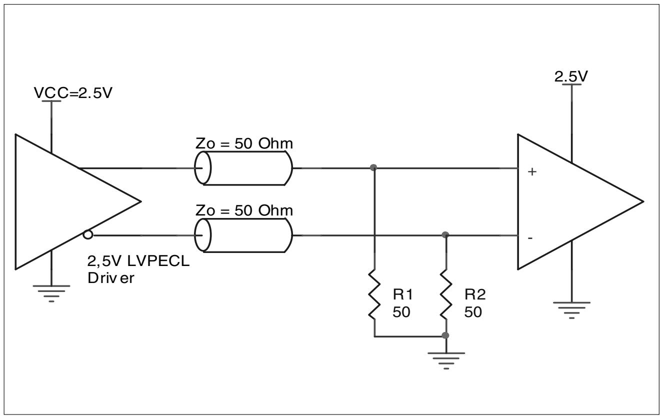


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

2.5V LVPECL INPUT WITH BUILT-IN 50Ω TERMINATIONS INTERFACE

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4D* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

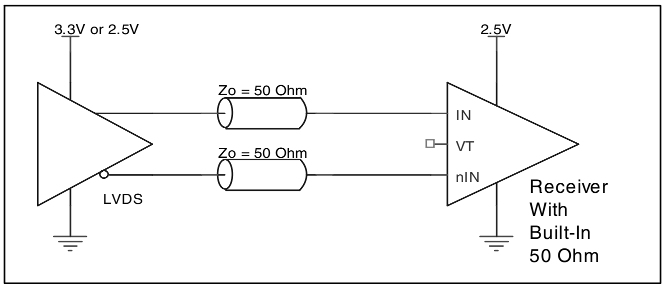


FIGURE 4A. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

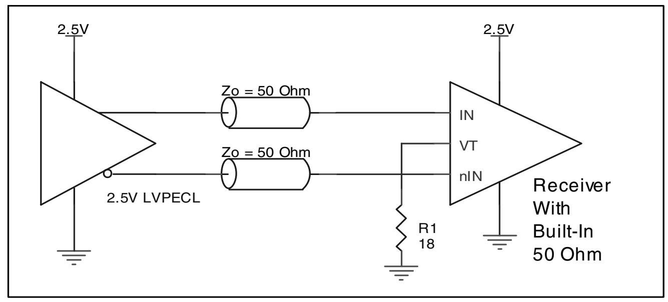


FIGURE 4B. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

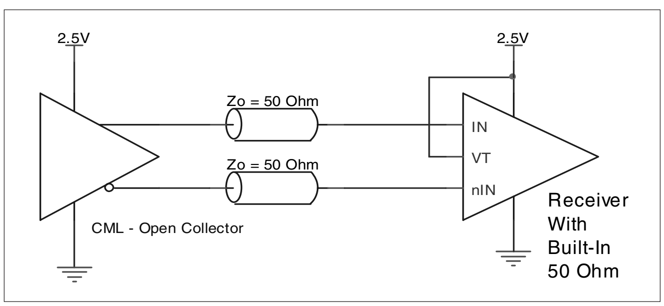


FIGURE 4C. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER

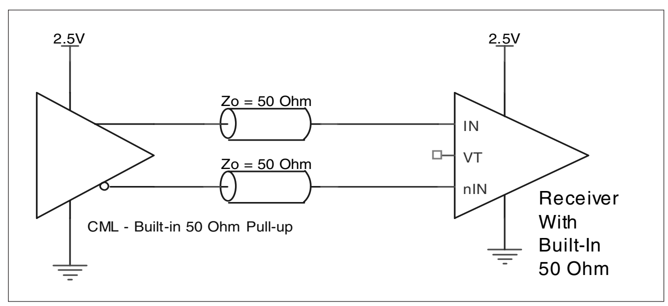


FIGURE 4D. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

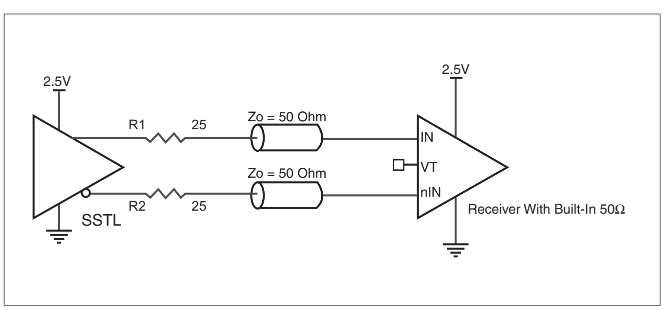


FIGURE 4E. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

3.3V LVPECL INPUT WITH BUILT-IN 50Ω TERMINATIONS INTERFACE

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

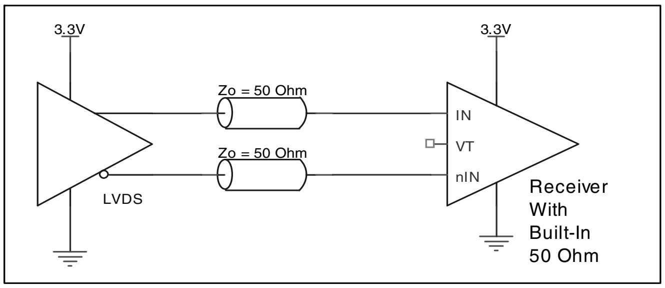


FIGURE 5A. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

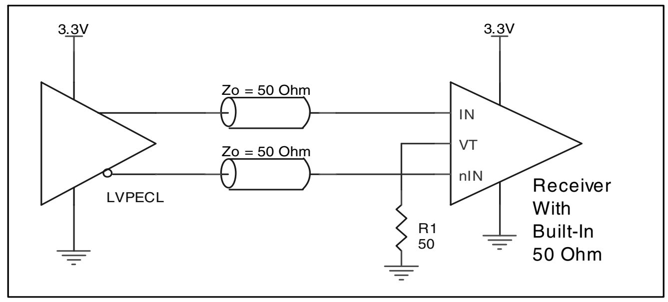


FIGURE 5B. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

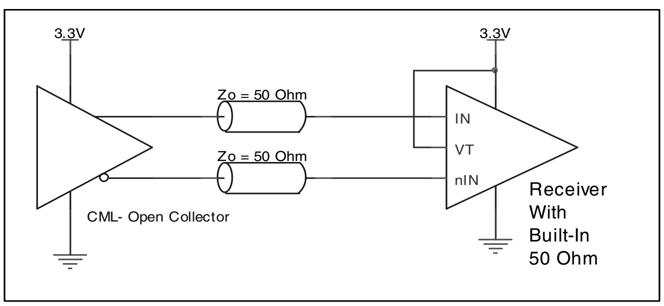


FIGURE 5C. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH OPEN COLLECTOR

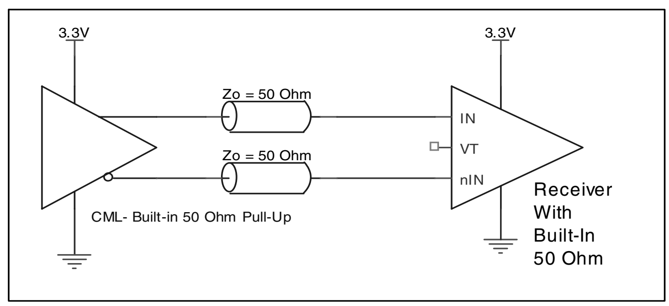


FIGURE 5D. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

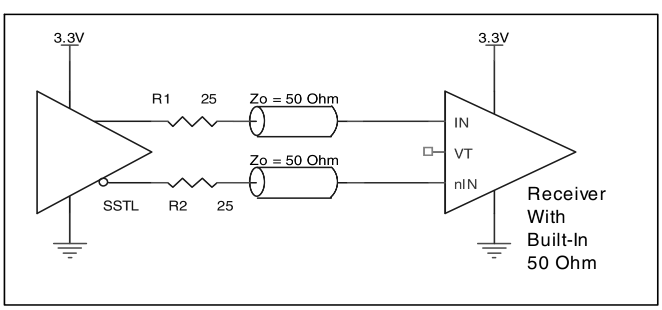


FIGURE 5E. HIPERCLOCKS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

3.3V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 6.*

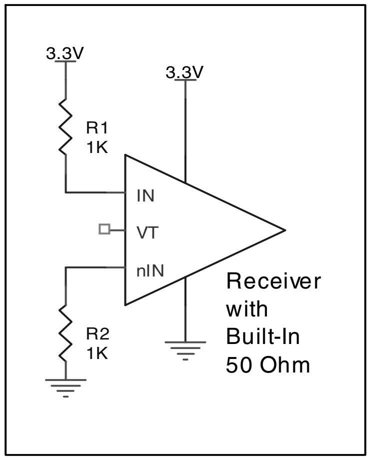


FIGURE 6. UNUSED INPUT HANDLING

2.5V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in *Figure 7.*

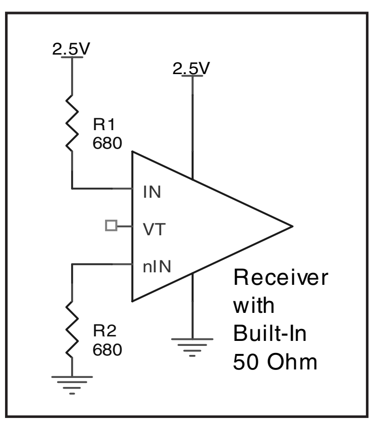


FIGURE 7. UNUSED INPUT HANDLING

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} 0 Air Flow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS889874 is: 326

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

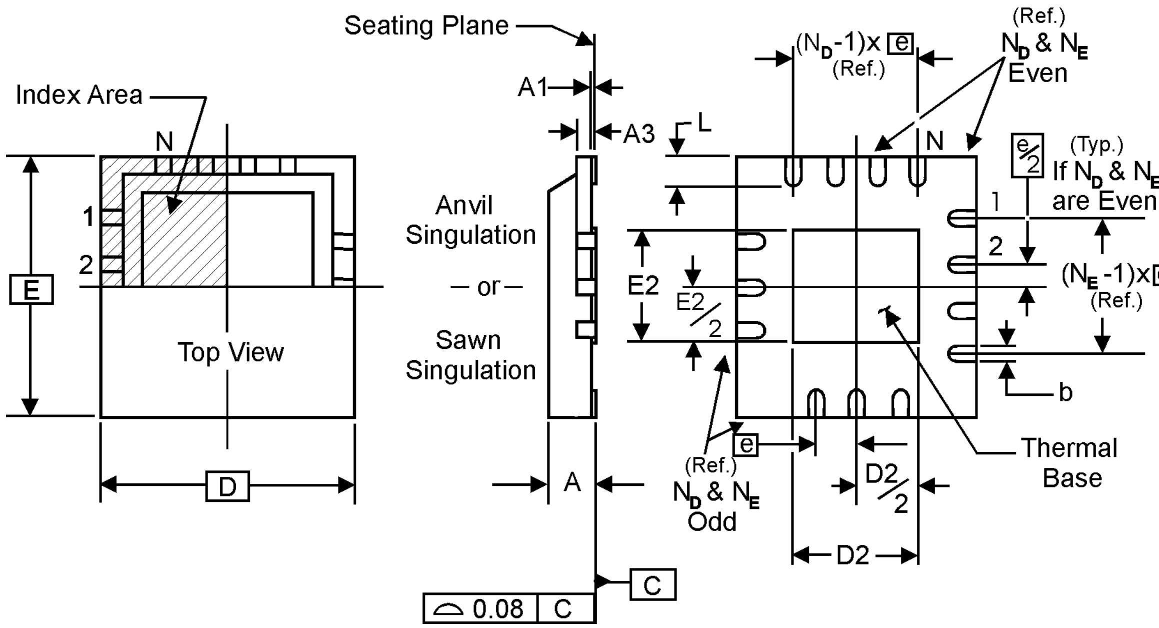


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	MINIMUM	MAXIMUM
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS889874AK	874A	16 Lead VFQFN	120 per tube	-40°C to 85°C
ICS889874AKT	874A	16 Lead VFQFN on Tape and Reel	3500	-40°C to 85°C