1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 1K words of ROM, and 41 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software:

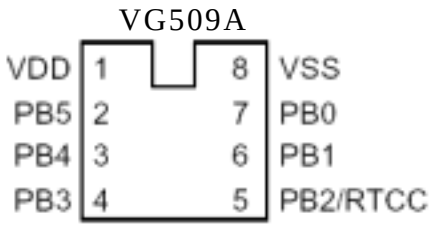
- Fully COMS static design
- 8-bit data bus
- On chip EPROM size : 1 K words
- Internal RAM size : 47 bytes (41 general purpose registers, 6 special registers)
- 36 single word instructions
- 14-bit instructions
- 2-level stacks
- Operating voltage : 2.5 V ~ 6.0 V
- Operating frequency : 0 ~ 20 MHz
- The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset
- Sleep Mode for power saving
  Sleep current @ 5V＜5.0 μA, WDT Enable
- 5 types of oscillator can be selected by programming option:

  INTRC－Internal 4 MHz RC oscillator
  RC－Low cost RC oscillator
  LFXT－Low frequency crystal oscillator
  XTAL－Standard crystal oscillator
  HFXT－High frequency crystal oscillator
- 3 oscillator start-up time can be selected by programming option
- 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- On-chip RC oscillator based Watchdog Timer(WDT)
- Wake-up from sleep on pin change

3. Applications

The application areas of this VG509A range from appliance motor control and high speed automotive to low power remote transmitters/receivers, small instruments, chargers, toy, automobile and PC pe-ripheral ... etc.

4. Pin Assignment



5. Packages available:

PDIP8
SOP8

5. Pin Function Description

Pin Name	I/O	Function Description
PB0, PB1, PB3~PB5	I/O	Port B, TTL input level
RTCC/PB2	I/O	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
Vdd		Power supply
Vss		Ground

6. Memory Map

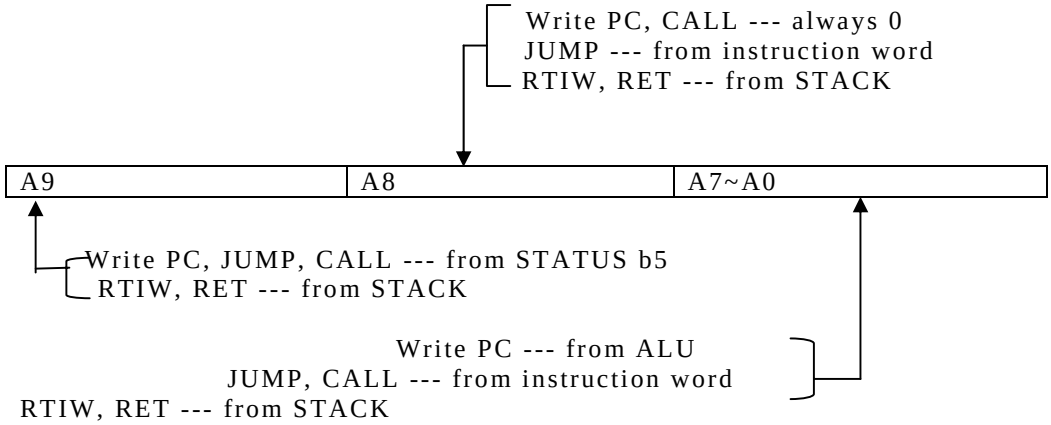
(A) Register Map

Address	Description
BANK0	
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
06	Port B
07~1F	General purpose registers
BANK1	
30~3F	General purpose registers

(1)IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

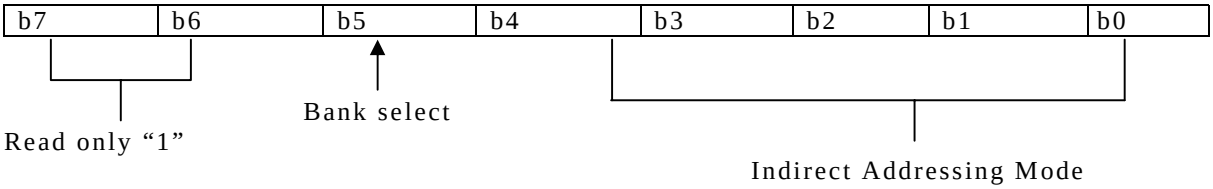
(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power down bit
4	TF	WDT Timer overflow Flag bit
5	PAGE	ROM page select bit :
6	——	Unimplemented
7	PCWUF	Pin change wake up from sleep

(5) MSR (Memory Bank Select Register) : R4



(7) PORT B : R6

PB5~PB0, I/O Register

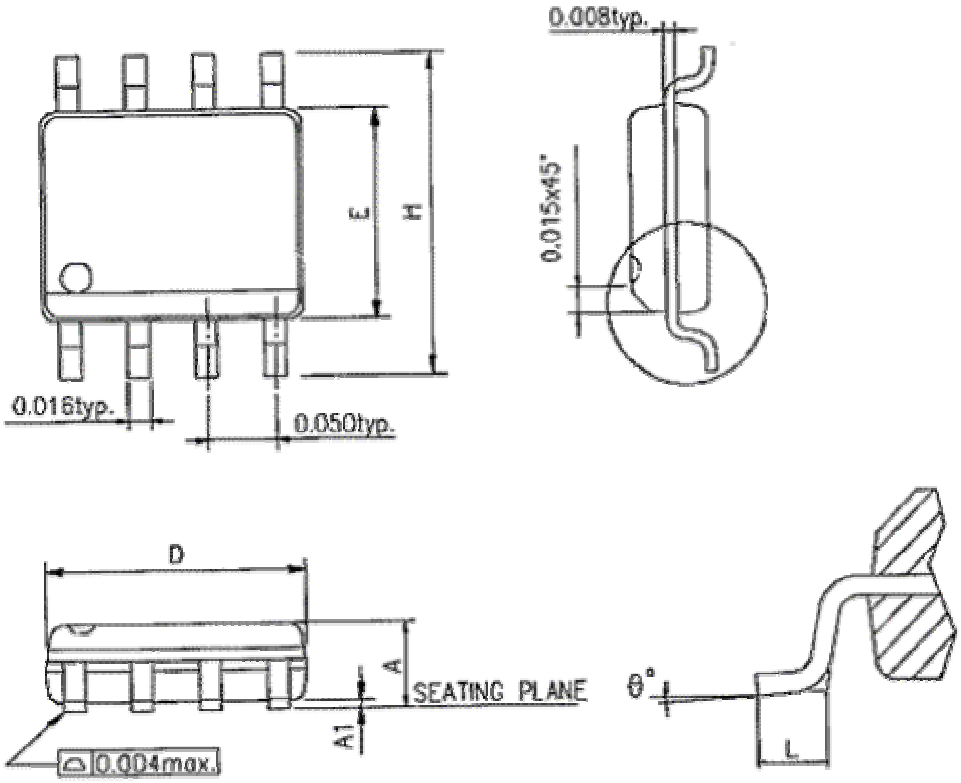
(8) TMR (Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2 — 0	PS2—0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		
6	PBPHB	PortB pull-high : 0 — Enable 1 — Disable		
7	PBWUB	PortB wake-up : 0 — Enable 1 — Disable		

(9) CPIO B (Control Port I/O Mode Register)
The CPIO register is “write-only”
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

Package:

8L SOP (150 mil body)

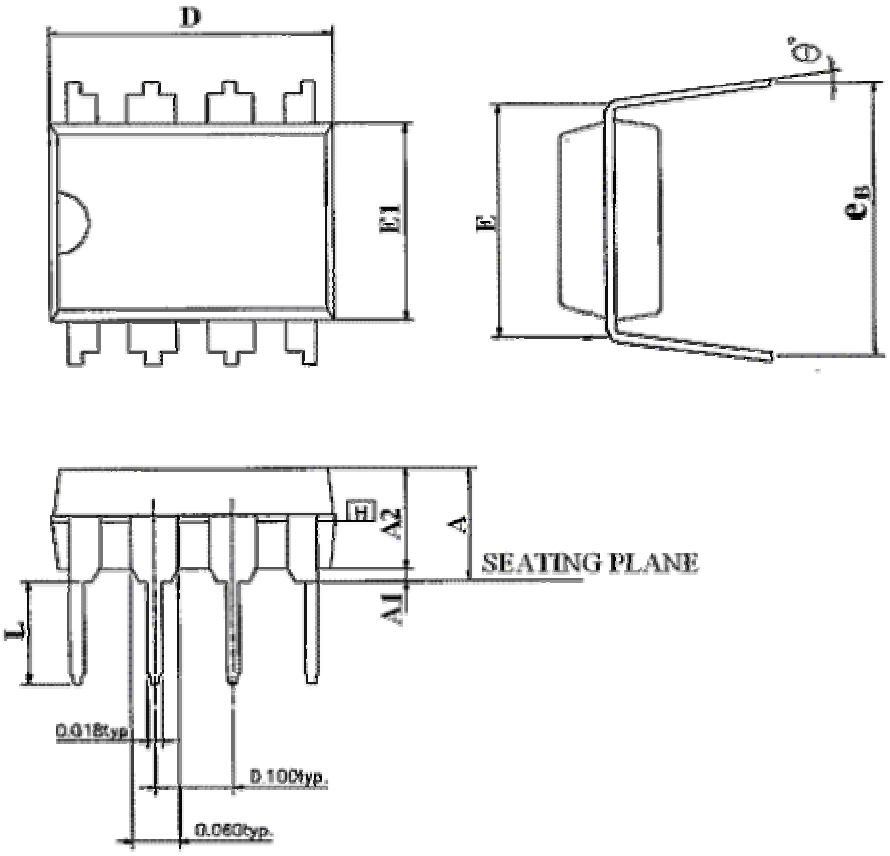


Unit : Inch

Symbols	A	A_1	D	E	H	L	θ °
Min.	0.053	0.004	0.189	0.150	0.228	0.016	0
Max.	0.069	0.010	0.196	0.157	0.244	0.050	8

NOTES :
Jedec outline：MS-012 AA

8PINS P-DIP(300mil body)



Unit : Inch

Symbols	A	A_1	A_2	D	E	E_1	L	e_B	θ °
Min.	—	0.015	0.115	0.355	0.300 BSC	0.240	0.115	—	0
Nor.	—	—	0.130	0.365		0.250	0.130	—	7
Max.	0.210	—	0.195	0.400		0.280	0.150	0.430	15

NOTES :

Jedec outline: MS-001 BA