V320USC Universal System Controller

PCI System Controller for 32-Bit MIPS™ and SuperH™ System Interface

Device Highlights

- Glueless interface between popular MIPS™ and SuperH™ processors and the standard 32-bit PCI bus
- Fully compliant with PCI 2.2 specification
- Configurable for primary master, bus master, or target operation
- SDRAM controller with support for Enhanced SDRAM
- Up to 1 KB burst access to (E)SDRAM from PCI, 32 bytes from local processor (MIPS mode)
- 640 bytes of on-chip FIFO storage with Dynamic Bandwidth Allocation™ architecture
- On-the-fly byte order (endian) conversion
- I2O Ready™ ATU and messaging unit
- Programmable chip select / peripheral device strobe generation
- Hot Swap Ready (PICMG™ Hot Swap Specification 2.1)
- Implementation of PCI Bus Power Management Interface Specification Version 1.0
- 3.3 V operation with 5V tolerant inputs
- 208-pin PQFP package
- Up to 75 MHz local bus clock with separate asynchronous PCI clock up to 50 MHz
- Two 32-bit timers
- Initialization through local processor, PCI or serial EEPROM

Introduction

The V320USC Universal System Controller simplifies the design of systems based on MIPS and SuperH microprocessors by replacing many lower integration support components with a single, high-integration device. This saves design time, board area, and manufacturing cost.

The I2O Ready V320USC from V3 Semiconductor is a high performance PCI bridge with integrated SDRAM controller for MIPS processors operating at up to 75 MHz bus speed. It features address translation capabilities and large on-chip buffers. A separate peripheral bus provides low latency access to SDRAM. The peripheral controller on the V320USC also performs address decoding and chip-select strobes generation for SRAM, PROM and other slow peripherals.

The integrated SDRAM Controller connects the processor as well as the PCI bus through on-chip FIFOs to SDRAM arrays of up to 1 GB in size. The fully programmable SDRAM controller also supports the use of Enhanced SDRAM to achieve even greater performance. Burst accesses of up to 1 KB from PCI and 32 bytes from the MIPS processor are supported.

The two general purpose 32-bit timers can be individually configured as a pulse width modulator, or used in other modes such as retriggerable or one-shot. The bus watch timer (MIPS mode) prevents system hangs during accesses to undecoded regions. Interrupts for a real time OS can be easily generated by the system heartbeat timer. A watchdog timer is also provided for graceful recovery from catastrophic program failures. Interrupt requests for all on-chip peripherals are managed by the Interrupt Control Unit. Additionally, off-chip interrupts can be routed to the Interrupt Control Unit.

The V320USC is packaged in a low-cost 208-pin EIJA Plastic Quad Flat Pack (PQFP), and is available in 75 MHz speed grade (MIPS mode), 66 MHz (SH mode).

This document contains the product codes, pinout, package mechanical information, DC characteristics, and AC characteristics for the V320USC. Detailed functional information is contained in the User's Manual.

Product Code

Table 1 describes the product codes available.

Table 1: Product Code

Product Code	Processors	Package	Frequency
V320USC-75LP REV B1	MIPS (32-bit bus), SH3, SH4 (32-bit bus)	208-pin EIAJ PQFP	75MHz (66 MHz SH)
V320USC-75LPN REV B1	MIPS (32-bit bus), SH3, SH4 (32-bit bus)	PB-Free 208-pin EIAJ PQFP	75MHz (66 MHz SH)

Pin Description

Table 2 lists the pin types found on the V320USC.

Table 2: Pin Types

Pin Type	Description
PCI I	PCI input only pin.
PCI O	PCI output only pin.
PCI I/O	PCI tri-state I/O pin.
PCI I/OD	PCI input with open drain output.
I/O_2, I/O_8, I/O_{12}	TTL I/O pins with 2/8/12 mA drive
I	TTL input only pin.
O_2, O_8, O_{12}	TTL output pins with 2/8/12 mA drive

Signal Description

Table 3 through **Table 8** describe the function of each pin on the V320USC.

Table 3: Signal Description—PCI Bus Interface

Signal	Type	R[a]	Description
AD[31:0]	PCI I/O	Z	Address and data, multiplexed on the same pins.
C/$\overline{\text{BE}}$[3:0]	PCI I/O	Z	Bus Command and Byte Enables, multiplexed on the same pins.
PAR	PCI I/O	Z	Parity represents even parity across AD[31:0] and C/$\overline{\text{BE}}$[3:0].
FRAME	PCI I/O	Z	Cycle Frame indicates the beginning and burst length of an access.
IRDY	PCI I/O	Z	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
TRDY	PCI I/O	Z	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
STOP	PCI I/O	Z	Stop indicates the current target is requesting the master to stop the current transaction (retry or disconnect).
DEVSEL	PCI I/O	Z	Device Select, when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, $\overline{\text{DEVSEL}}$ indicates whether any device on the bus has been selected.
IDSEL	PCI I		Initialization Device Select is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
PERR	PCI I/O	Z	Parity Error is used to report data parity errors during all PCI transactions except a Special Cycle.
SERR	PCI I/OD	Z	System Error is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
REQ	PCI O	Z	Request indicates to the arbiter that this agent requests use of the bus.
GNT	PCI I		Grant indicates to the agent that access to the bus has been granted.
PCLK	PCI I		PCLK provides timing for all transactions on the PCI bus.

a. **R** indicates state during reset.

Table 4: Signal Description—Local Bus Interface, MIPS™ Mode

Signal	Type	R	Description
SYSAD[31:0]	I/O	Z	System Address / Data (multiplexed)
SYSCMD[8:0]	I/O	Z	System Command / data identifier. When MODE0 = '0', SYSCMD[8:5] should be pulled high.
VALIDIN	O_8	Z	Valid command or data from external agent. This signal should have an external pull-up resistor.
VALIDOUT	I		Valid command or data from MIPS™
RELEASE	I		Release the system interface to slave state
WRRDY	O_8	Z	Write Ready: this signal should have an external pull-up resistor.
LCLK	I		Local clock

Table 5: Signal Description—Local Bus Interface, SH3/4 Mode

Signal	Type	R	Description
A[31:26]/$\overline{CS}$[5:0]	I/O_8 I	Z	Upper System Address
A[25:0]	I/O_8	Z	Lower System Address
D[31:0]	I/O_8	Z	Data Bus
RD/$\overline{WR}$	I/O_8	Z	Read/not Write. This is also referred to as $\overline{MWE}$ for SDRAM
BS	I		Bus Cycle Start
$\overline{WAIT}$/$\overline{RDY}$	O_8	Z	Bus Wait
RBE_EN[a]	I		Enable Read Byte Enables: When active (‘0’), PCI byte lane enables are derived from $\overline{RBE}$[3:0] for a local-to-PCI read access.
RBE[3:0][b]	I		Read Byte Enables: provides the byte enable pattern for local-to-PCI read access when $\overline{RBE\_EN}$ is active. Byte enables for writes are derived from the $\overline{DQM}$[3:0] signals.
BREQ	O_8	Z	Bus Request Output: indicates that the V320USC wants to perform a bus cycle on the local bus
BACK	I		Bus Acknowledge: asserted to allow the V320USC to take ownership of the local bus.
BREQ_IN[c]	I		Bus Request Input: assertion of this input will cause the V320USC to give up ownership of the local bus at the end of the current burst/single cycle so that a higher priority master can take ownership. Typically connected to $\overline{IRQ\_OUT}$.
LCLK	I		Local clock. This would be connected to either CKIO on the processor or a clock driver which provides a clock with the same phase relationship as CKIO. See V3 Reference Designs for further details.

a. Not available in revision B0 silicon
b. Not available in revision B0 silicon
c. Not available in revision B0 silicon

Table 6: Signal Description—DRAM and Peripheral Bus Interface

Signal	Type	R	Description
MA[14:0]	O_{12}	Z	SDRAM Memory Address (also, A[16:2] for peripheral access). MA[14:13] are typically used for BA[1:0]
$\overline{DCS}$[3:0]	O_8	Z	SDRAM Chip Select. This should be connected to the $\overline{CS}$ inputs of SDRAM chips or DIMM devices.
DQM[3:0] $\overline{MBE}$[3:0]	I/O_8	Z	SDRAM Data Mask for SDRAM access, Byte enables ($\overline{MBE}$[3:0]) and A[1:0] for peripheral access, and write enables for SH3/4 mode access.
RAS	O_{12}	Z	SDRAM Row Address Strobe
CAS	O_{12}	Z	SDRAM Column Address Strobe
MWE	O_{12}	Z	SDRAM Memory Write Enable
MAD[31:0]	I/O_8	Z	SDRAM and peripheral bus data. MAD[31:0] is known as D[31:0] when in SH3/4 mode.
SDA	I/OD_2	Z	Serial EEPROM Data

Table 6: Signal Description—DRAM and Peripheral Bus Interface *(Continued)*

Signal	Type	R	Description
SCL	O_2	Z	Serial EEPROM Clock
IOC[11:0]	I/O_8	Z	Multi-purpose I/O that can be configured for many functions
$\overline{INT}$[3:0]	PCI I/OD	Z	General purpose interrupt inputs/outputs: may be used for either PCI or local processor interrupts

Table 7: Signal Description—Mode and Reset

Signal	Type	R	Description
RSTIN	I		Reset Input: Active low reset input used to initialize all internal functions of the chip.
RSTOUT	O_8	0	Reset Output: Driven active when the input reset is driven active. Driven inactive when the RSTOUT bit in the system register is set. The $\overline{RSTOUT}$ signal is synchronous to the rising edge of LCLK.
CH	I		PCI Precharge Bias: This signal is driven low to activate the on-chip precharge bias for use in PICMG Hot Swap applications. Non-Hot Swap applications should pull this signal high.
MODE2:1 MODE0	I/O_8 I	Z	MODE Input: selects the CPU mode: 'H' - Tie High with a weak pull up of 4.7–10K Ω 'L' - Tie Low with a weak pull down of 4.7–10K Ω

MODE			Description
2	1	0	
Pin 55	Pin 54	Pin 202	
SYSCMD7	SYSCMD8	'H'	MIPS with 9 bit SYSCMD
'H'	'H'	'L'	MIPS with 5 bit SYSCMD
'H'	'L'	'L'	SH3
'L'	'L'	'L'	SH4
others			reserved

Table 8: Signal Description—Power and Ground Signals

Signal	Type	R	Description
V_{CC}	-		POWER leads for external connection to a 3.3V V_{CC} board plane.
GND	-		GROUND leads for external connection to a GND board plane.
NC	-		No connect.
'H'	-		Tie High with a weak pull up of 4.7K-10K

DC Specifications

The DC specifications for the PCI bus signals match exactly those given in the *PCI Specification*, Rev. 2.2 Section 4.2.1.1. For more information on the PCI DC specifications, see the *PCI Specification*.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to +3.6	V
V_{IN}	DC input voltage	-0.3 to 6.0	V
T_{STG}	Storage temperature range	-55 to +125	°C

Table 10: Guaranteed Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3.0 to 3.6	V
Theta Ja	Thermal resistance	40 to 45	°C/w
T_A	Ambient temperature range	-40 to +85	°C

Table 11: DC Operating Conditions

Symbol	Parameter	Max.	Unit	Condition
I_{CC}(max)	Maximum supply current	110	mA	PCLK=33MHz, LCLK=66MHz, Vcc=3.6V, all buses operating
I_{CC}(typ)	Typical supply current	80	mA	

PCI Bus DC Specifications

Table 12: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IH}	Input high voltage		$0.5V_{CC}$	V_{CC} + 0.5	V
V_{IL}	Input low voltage		-0.5	$0.3V_{CC}$	V
I_{IH}	Input high leakage current[a]		$0.7V_{CC}$		µA
I_{IL}	Input low leakage current	$0 < V_{IN} < V_{CC}$		+10	µA
V_{OH}	Output high voltage	I_{OUT} = -500µA	$0.9V_{CC}$		V
V_{OL}	Output low voltage[b]	I_{OUT} = 1500µA		$0.1V_{CC}$	V
C_{IN}	Input pin capacitance[c]			10	pF
C_{CLK}	PCLK pin capacitance		5	12	pF
C_{IDSEL}	IDSEL pin capacitance[d]			8	pF
L_{PIN}	Pin inductance			20	nH

a. Input leakage currents include high impedance output leakage for all bi-directional buffers with tri-state outputs.
b. Signals without pull-up resistors have greater than 3mA low output current. Signals requiring pull resistors have greater than 6mA output current. The latter include $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, $\overline{\text{STOP}}$, $\overline{\text{SERR}}$, $\overline{\text{PERR}}$.
c. Absolute maximum pin capacitance for a PCI unit is 10pF (except for CLK).
d. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

Local Bus DC Specifications

Table 13: Local Bus/M Bus Signals DC Operating Specifications (V_{CC} = 3.3V± 0.3V)

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IH}	Input high leakage current	$V_{IN} = V_{CC}$	-10	10	µA
I_{IL}	Input low leakage current	V_{IN}=GND	-10	10	µA
V_{OH}	Output high voltage	I_{OUT} = -2, -8, -12mA	2.4		V
V_{OL}	Output low voltage	I_{OUT} = 2, 8, 12mA		0.4	V
I_{OZL}	Low level float input leakage	V_{OL} = GND	-10	10	µA
I_{OZH}	High level float input leakage	$V_{OH} = V_{CC}$	-10	10	µA
C_{IO}	Input and output capacitance			TBA	pF

AC Specifications

The AC specifications for the PCI bus signals match exactly those given in the *PCI Specification*, Rev. 2.1, Section 4.2.1.2. For more information on the PCI AC specifications, including the V/I curves for 5V signalling, see section 4.2.1.2 of the *PCI Specification*, Rev 2.1.

PCI Bus Timings

Table 14: PCI Bus Signals AC Operating Specifications

Symbol	Parameter	Condition	Min.	Max.	Unit
$I_{OH(AC)}$	Switching current high	$0V < V_{OUT} \leq 0.3V_{CC}$	$-12V_{CC}$		mA
		$0.3V_{CC} < V_{OUT} < 0.9V$	$-17.1(V_{CC}-V_{OUT})$		mA
		$0.7V_{CC} < V_{OUT} < V_{CC}$		Equation C	
	(Test point)	$V_{OUT} = 0.7V_{CC}$		$-32V_{CC}$	
$I_{OL(AC)}$	Switching current low	$V_{CC} > V_{OUT} > 0.6V_{CC}$	$16V_{CC}$		mA
		$0.6V_{CC} > V_{OUT} > 0.1V_{CC}$	$26.7V_{CC}$		mA
	(Test point)	$V_{OUT} = 0.18V_{CC}$		$38V_{CC}$	mA
I_{CL}	Low clamp current	$-3V < V_{IN} < -1V$	$-25+(V_{IN}+1)/0.015$		mA
t_R	Unloaded output rise time	$0.2V_{CC}$ to $0.6V_{CC}$	1	4	V/ns
t_F	Unloaded output fall time	0.6V to 0.2V	1	4	V/ns

Local and M Bus Timings

Table 15: Local and M Bus AC Test Conditions

Symbol	Parameter	Limits	Unit
V_{CC}	Supply voltage 3.3 volt operation	3.0 to 3.60	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 16: M Bus AC Test Conditions

Symbol	Parameter	Limits	Unit
V_{CC}	Supply voltage 3.3 volt operation	3.0 to 3.60	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 17: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Supply Voltage	Derating
8 mA	3.3 volt	0.019 ns/pF for loads > 50 pF
12 mA	3.3 volt	0.017 ns/pF for loads > 50 pF

Timing Parameters

Figure 1: Clock and Synchronous Signals

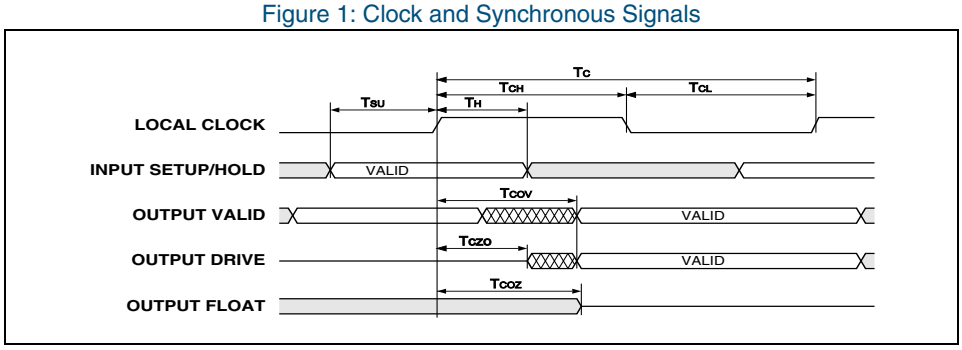

Figure 2: ALE Timing

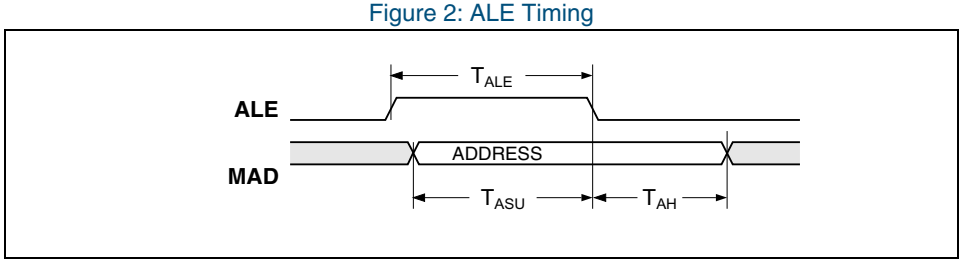

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Table 18: Local Bus/M-Bus Timing Parameters for Vcc =3.3 Volts +/- 5%

Number	Symbol	Description	75 MHz		Unit
			Min.	Max.	
1	T_C	LCLK period	13.33		ns
2	T_{CH}	LCLK high time	4.5		ns
3	T_{CL}	LCLK low time	4.5		ns
4	T_{SU}	Synchronous input setup		2.5	ns
4a	T_{SU}	Synchronous input setup for non-pipelined signals[a]		9	ns
5	T_H	Synchronous input hold		1.5	ns
6	T_{COV}	LCLK to output valid delay		9	ns
7	T_{CZO}	LCLK to output driving delay		9	ns
8	T_{COZ}	LCLK to high impedance delay		12	ns
9	T_{ALE}	ALE pulse width	T_{CH}-1	T_{CH}+2	ns
10	T_{ASU}	Address to ALE setup time	T_{CH}		ns
11	T_{AH}	Address hold time from ALE	T_{CL}-4		ns

a. Non-pipelined signals include $\overline{MRDY}$ when the SYNC_RDY bit in the LB_BUS_CFG register is ‘0’, and $\overline{BGNT}$ when the BREQ_SYNC register is ‘1’.

Table 19: PCI Bus Timing Parameters for Vcc = 3.3 Volts +/- 10%

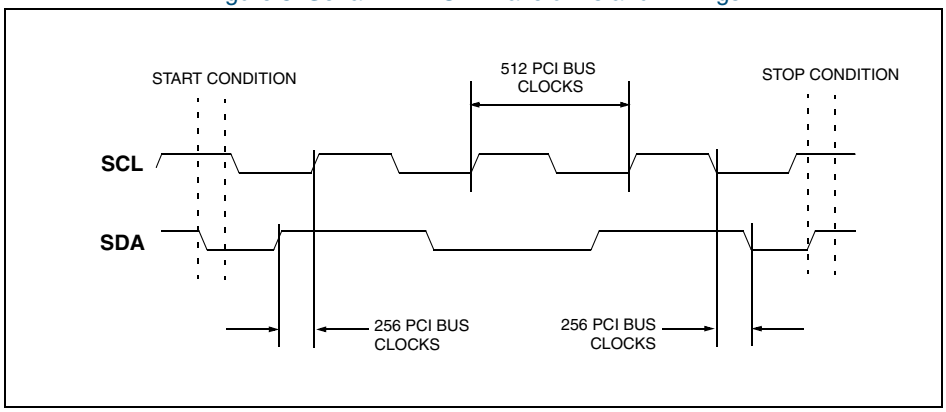
Number	Symbol	Description	Min.	Max.	Unit
1	T_C	PCLK period	20		ns
2	T_{SU}	Synchronous input setup to PCLK[a]	7		ns
2a	T_{SU}	Synchronous input setup to PCLK ($\overline{GNT}$)	10		ns
3	T_H	Synchronous input hold from PCLK	0		ns
4	T_{COV}	PCLK to output valid delay[b]	2	11	ns
4a	T_{COV}	PCLK to output valid delay ($\overline{REQ}$)	2	12	ns
5	T_{CZO}	PCLK to output driving delay	2	11	ns
6	T_{COZ}	PCLK to high impedance delay	3	14	ns
7	T_{RST}	Reset period	$16 \cdot T_C$		

a. All PCI signals except $\overline{GNT}$.
b. All PCI signals except $\overline{REQ}$.

Serial EEPROM Port TImings

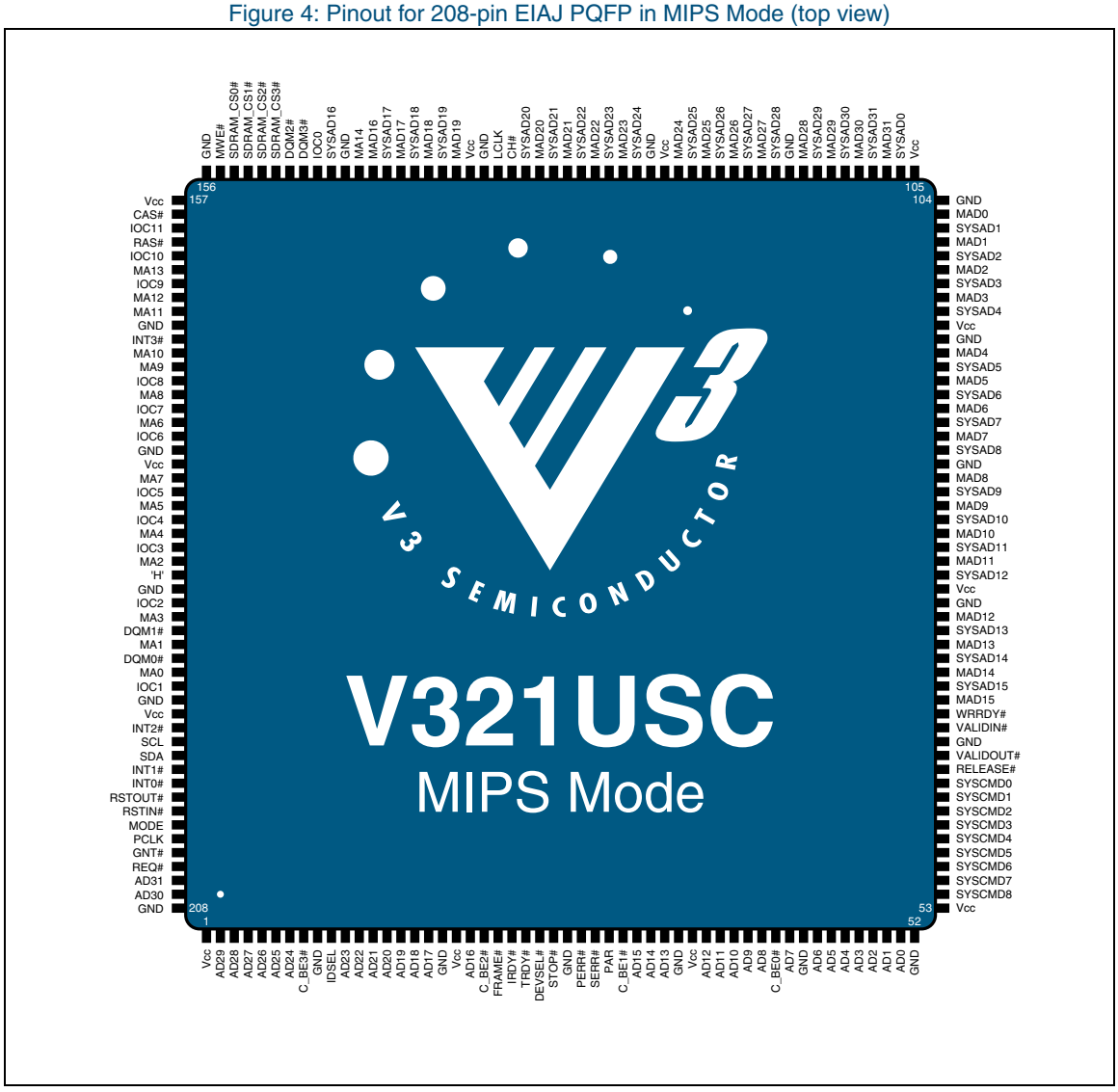
The clock for the serial EEPROM interface is derived by dividing the PCI bus clock. The waveforms generated are shown in **Figure 3**.

Figure 3: Serial EEPROM Waveforms and Timings



208-pin EIAJ PQFP in MIPS Mode Pinout Diagram

Figure 4: Pinout for 208-pin EIAJ PQFP in MIPS Mode (top view)



MIPS™ Mode Pinout Table

Table 20: Pin Assignments for MIPS™ Mode

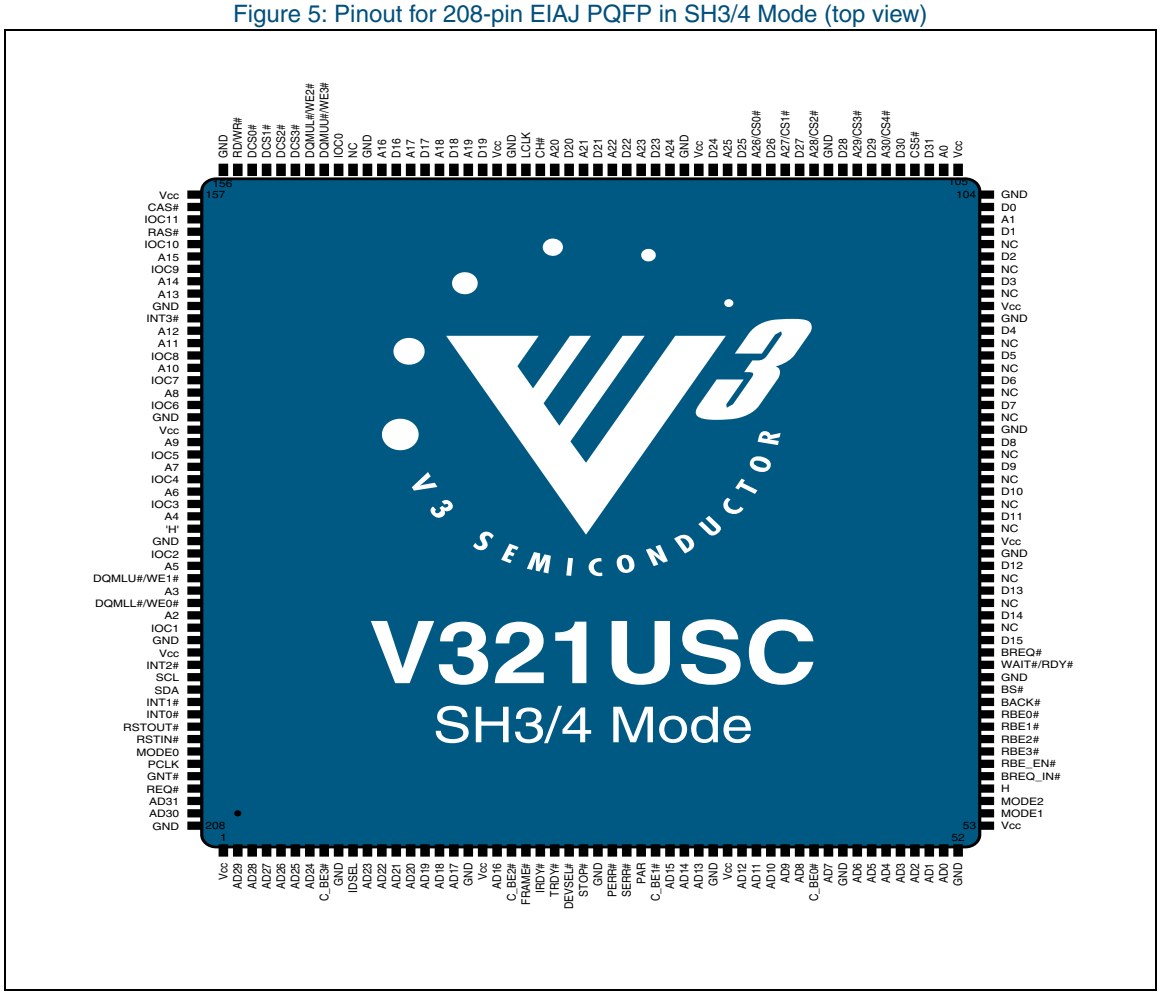
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	V_{CC}	53	Vcc	105	Vcc	157	Vcc
2	AD29	54	SYSCMD8	106	SYSAD0	158	CAS
3	AD28	55	SYSCMD7	107	MAD31	159	IOC11
4	AD27	56	SYSCMD6	108	SYSAD31	160	RAS
5	AD26	57	SYSCMD5	109	MAD30	161	IOC10
6	AD25	58	SYSCMD4	110	SYSAD30	162	MA13
7	AD24	59	SYSCMD3	111	MAD29	163	IOC9
8	C/BE3	60	SYSCMD2	112	SYSAD29	164	MA12
9	GND	61	SYSCMD1	113	MAD28	165	MA11
10	IDSEL	62	SYSCMD0	114	GND	166	GND
11	AD23	63	RELEASE	115	SYSAD28	167	INT3
12	AD22	64	VALIDOUT	116	MAD27	168	MA10
13	AD21	65	GND	117	SYSAD27	169	MA9
14	AD20	66	VALIDIN	118	MAD26	170	IOC8
15	AD19	67	WRRDY	119	SYSAD26	171	MA8
16	AD18	68	MAD15	120	MAD25	172	IOC7
17	AD17	69	SYSAD15	121	SYSAD25	173	MA6
18	GND	70	MAD14	122	MAD24	174	IOC6
19	Vcc	71	SYSAD14	123	Vcc	175	GND
20	AD16	72	MAD13	124	GND	176	Vcc
21	C/$\overline{BE2}$	73	SYSAD13	125	SYSAD24	177	MA7
22	FRAME	74	MAD12	126	MAD23	178	IOC5
23	IRDY	75	GND	127	SYSAD23	179	MA5
24	TRDY	76	Vcc	128	MAD22	180	IOC4
25	DEVSEL	77	SYSAD12	129	SYSAD22	181	MA4
26	STOP	78	MAD11	130	MAD21	182	IOC3
27	GND	79	SYSAD11	131	SYSAD21	183	MA2
28	PERR	80	MAD10	132	MAD20	184	'H'
29	SERR	81	SYSAD10	133	SYSAD20	185	GND
30	PAR	82	MAD9	134	CH	186	IOC2
31	C/$\overline{BE1}$	83	SYSAD9	135	LCLK	187	MA3
32	AD15	84	MAD8	136	GND	188	DQM1
33	AD14	85	GND	137	Vcc	189	MA1
34	AD13	86	SYSAD8	138	MAD19	190	DQM0
35	GND	87	MAD7	139	SYSAD19	191	MA0
36	Vcc	88	SYSAD7	140	MAD18	192	IOC1
37	AD12	89	MAD6	141	SYSAD18	193	GND
38	AD11	90	SYSAD6	142	MAD17	194	Vcc
39	AD10	91	MAD5	143	SYSAD17	195	INT2
40	AD9	92	SYSAD5	144	MAD16	196	SCL
41	AD8	93	MAD4	145	MA14	197	SDA
42	C/$\overline{BE0}$	94	GND	146	GND	198	INT1

Table 20: Pin Assignments for MIPS™ Mode *(Continued)*

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
43	AD7	95	Vcc	147	SYSAD16	199	INT0
44	GND	96	SYSAD4	148	IOC0	200	RSTOUT
45	AD6	97	MAD3	149	DQM3	201	RSTIN
46	AD5	98	SYSAD3	150	DQM2	202	MODE0
47	AD4	99	MAD2	151	DCS3	203	PCLK
48	AD3	100	SYSAD2	152	DCS2	204	GNT
49	AD2	101	MAD1	153	DCS1	205	REQ
50	AD1	102	SYSAD1	154	DCS0	206	AD31
51	AD0	103	MAD0	155	MWE	207	AD30
52	GND	104	GND	156	GND	208	GND

208-pin EIAJ PQFP in SH3/4 Mode Pinout Diagram

Figure 5: Pinout for 208-pin EIAJ PQFP in SH3/4 Mode (top view)



SH3/4 Mode Pinout Table

Table 21: Pin Assignments for SH3/4 Mode

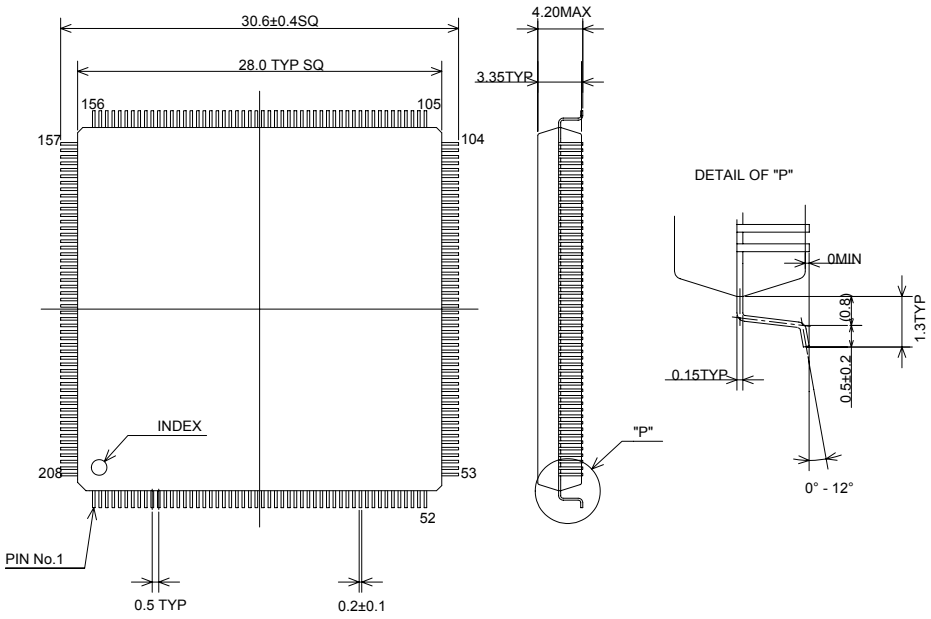
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vcc	53	Vcc	105	Vcc	157	Vcc
2	AD29	54	MODE1	106	A0	158	CAS
3	AD28	55	MODE2	107	D31	159	IOC11
4	AD27	56	'H'	108	A31/$\overline{CS5}$	160	RAS
5	AD26	57	BREQ_IN	109	D30	161	IOC10
6	AD25	58	RBE_EN	110	A30/$\overline{CS4}$	162	A15
7	AD24	59	RBE3	111	D29	163	IOC9
8	C/$\overline{BE3}$	60	RBE2	112	A29/$\overline{CS3}$	164	A14
9	GND	61	RBE1	113	D28	165	A13
10	IDSEL	62	RBE0	114	GND	166	GND
11	AD23	63	BACK	115	A28/$\overline{CS2}$	167	INT3
12	AD22	64	BS	116	D27	168	A12
13	AD21	65	GND	117	A27/$\overline{CS1}$	169	A11
14	AD20	66	$\overline{WAIT}$/$\overline{RDY}$	118	D26	170	IOC8
15	AD19	67	BREQ	119	A26/$\overline{CS0}$	171	A10
16	AD18	68	D15	120	D25	172	IOC7
17	AD17	69	NC	121	A25	173	A8
18	GND	70	D14	122	D24	174	IOC6
19	Vcc	71	NC	123	Vcc	175	GND
20	AD16	72	D13	124	GND	176	Vcc
21	C/$\overline{BE2}$	73	NC	125	A24	177	A9
22	FRAME	74	D12	126	D23	178	IOC5
23	IRDY	75	GND	127	A23	179	A7
24	TRDY	76	Vcc	128	D22	180	IOC4
25	DEVSEL	77	NC	129	A22	181	A6
26	STOP	78	D11	130	D21	182	IOC3
27	GND	79	NC	131	A21	183	A4
28	PERR	80	D10	132	D20	184	'H'
29	SERR	81	NC	133	A20	185	GND
30	PAR	82	D9	134	CH	186	IOC2
31	C/$\overline{BE1}$	83	NC	135	LCLK	187	A5
32	AD15	84	D8	136	GND	188	$\overline{DQMLU}$/$\overline{WE1}$
33	AD14	85	GND	137	Vcc	189	A3
34	AD13	86	NC	138	D19	190	$\overline{DQMLL}$/$\overline{WE0}$
35	GND	87	D7	139	A19	191	A2
36	Vcc	88	NC	140	D18	192	IOC1
37	AD12	89	D6	141	A18	193	GND
38	AD11	90	NC	142	D17	194	Vcc
39	AD10	91	D5	143	A17	195	INT2
40	AD9	92	NC	144	D16	196	SCL
41	AD8	93	D4	145	A16	197	SDA
42	C/$\overline{BE0}$	94	GND	146	GND	198	INT1

Table 21: Pin Assignments for SH3/4 Mode *(Continued)*

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
43	AD7	95	Vcc	147	NC	199	INT0
44	GND	96	NC	148	IOC0	200	RSTOUT
45	AD6	97	D3	149	$\overline{\text{DQMUU}}$/$\overline{\text{WE3}}$	201	RSTIN
46	AD5	98	NC	150	$\overline{\text{DQMUL}}$/$\overline{\text{WE2}}$	202	MODE0
47	AD4	99	D2	151	DCS3	203	PCLK
48	AD3	100	NC	152	DCS2	204	GNT
49	AD2	101	D1	153	DCS1	205	REQ
50	AD1	102	A1	154	DCS0	206	AD31
51	AD0	103	D0	155	RD/$\overline{\text{WR}}$	207	AD30
52	GND	104	GND	156	GND	208	GND

Packaging Drawing

Figure 6: 208-pin EIAJ PQFP Mechanical Details



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Revision History

Revision	Date	Originator and Comments
0.8	Dec 98	First pre-silicon revision of preliminary data sheet.
0.9	Jan 99	First pre-silicon release with Super-H™ processor information.
1.00	Mar 99	Remove “Preliminary” watermark; Update Table 2: Pin Types; Update Table 3: Signal Descriptions; Update Table 9: Local Bus Signals DC Operating Specifications.
1.01	Apr 99	Update diagrams; update tables, register data; add M bus data.
1.02	June 99	Update diagrams, update tables, and update register data for B1 step.
F	July 2004	Bernhard Andretzky and Kathleen Murchek Update to QuickLogic format standards.
G	July 2005	Mehul Kochar and Kathleen Murchek Updated Product Code table to include item V320USC-75LPN REV B1.

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