## Description

The μPB8286 and μPB8287 are octal bus transceivers used for buffering microprocessor bus lines. Being bi-directional, they are ideal for buffering the data bus lines on 8- or 16-bit microprocessors. Each B output is capable of driving 32 mA low or 5 mA high.

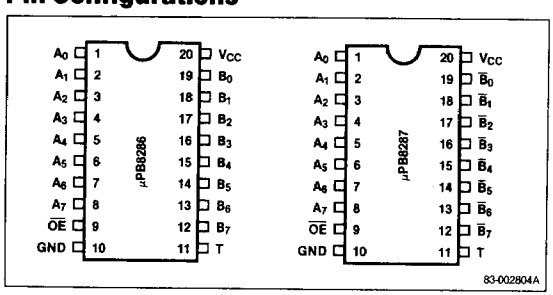
## Features

- ☐ Data bus buffer driver for μCOM-8 (8080, 8085A, 780) and μCOM-16 (8086) families
- ☐ Low input load current – 0.2 mA max
- ☐ High output drive capability for driving system data bus
- ☐ Three-state outputs

## Ordering Information

| Part Number | Package Type | I/O Delay, Max |
|---|---|---|
| μPB8286C | 20-pin plastic DIP | 22 ns |
| μPB8287C | 20-pin plastic DIP | 30 ns |

## Pin Configurations




## Pin Identification

| No. | Symbol | Function |
|---|---|---|
| 1–8 | $A_0$–$A_7$ | Local data bus |
| 9 | $\overline{OE}$ | Output enable |
| 10 | GND | Ground |
| 11 | T | Transmit |
| 12–19 | (μPB8286) $B_7$–$B_0$<br>(μPB8287) $\overline{B}_7$–$\overline{B}_0$ | System data bus |
| 20 | $V_{CC}$ | Power supply |

## Pin Functions

### $\overline{OE}$ (Output Enable)

This active low input control signal enables the output drivers selected by T.

### T (Transmit)

This input controls the direction of data through the transceivers. When high, data is transferred from the $A_0$–$A_7$ inputs to the $B_0$–$B_7$ outputs. When low, data is transferred from the $B_0$–$B_7$ inputs to the $A_0$–$A_7$ outputs.

### $A_0$–$A_7$ (Local Data Bus)

$A_0$–$A_7$ are bidirectional drivers that, depending on the state of the transmit pin, accept data from or transfer data to the processor's local bus.

### $B_0$–$B_7$ (System Data Bus)

$B_0$–$B_7$ are bidirectional drivers that, depending on the state of the transmit pin, accept data from or transfer data to the system bus.

### GND (Ground)

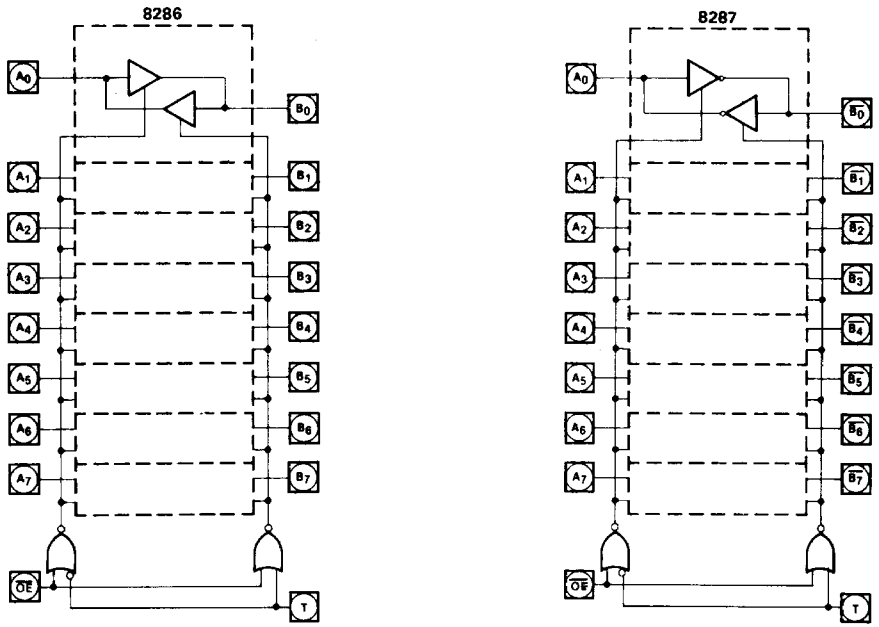
This is the ground.

### $V_{CC}$ (Power Supply)

This is the +5 V power supply.

8

## Block Diagram




| OE | T | RESULT |
|---|---|---|
| 0 | 0 | A←B |
| 0 | 1 | A→B |
| 1 | 0 | A and B are high impendace |
| 1 | 1 | |

## Functional Description

MOS microprocessors like the 8080/8085A/8086 are generally capable of driving a single TTL load. This also applies to MOS memory devices. While sufficient for minimum type small systems on a single PC board, it is usually necessary to buffer the microprocessor and memory signals when a system is expanded or signals go to other PC boards.

These octal bus transceivers are designed to do the necessary buffering.

### Bidirectional Driver

Each buffered line of the octal driver consists of two separate three-state buffers. The B side of the driver is designed to drive 32 mA and interface the system side of the bus to I/O, memory, etc. The A side is connected to the microprocessor.

### Control Gating, $\overline{OE}$, T

The $\overline{OE}$ (output enable) input is an active low signal used to enable the drivers selected by T on to the respective bus.

T is an input control signal used to select the direction of data through the transceivers. When T is high, data is transferred from the $A_0$-$A_7$ inputs to the $B_0$-$B_7$ outputs, and when low, data is transferred from $B_0$-$B_7$ to the $A_0$-$A_7$ outputs.

## Absolute Maximum Ratings

$T_A = 25°C$

| | |
|---|---|
| Power supply voltage, $V_{CC}$ | −0.5 V to +7 V |
| Input voltage, $V_I$ | −1.0 V to +5.5 V |
| Output voltage, $V_O$ | −0.5 V to +7 V |
| Operating temperature, $T_{OPT}$ | 0°C to +70°C |
| Storage temperature, $T_{STG}$ | −65°C to +150°C |

**Comment:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5\,V \pm 10\%$

| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input voltage low — A side | $V_{IL}$ | | | +0.8 | V | $V_{CC} = 5.0$ V, (Note 1) |
| — B side | | | | +0.9 | V | $V_{CC} = 5.0$ V, (Note 1) |
| Input voltage high | $V_{IH}$ | | | 2 | V | $V_{CC}$ +5.0 V, (Note 1), F = 1 MHz |
| Output voltage low — B outputs | $V_{OL}$ | | | +0.45 | V | $I_{OL} = 32$ mA |
| — A outputs | | | | +0.45 | V | $I_{OL} = 16$ mA |
| Output voltage high — B outputs | $V_{OH}$ | 2.4 | | | V | $I_{OH} = -5$ mA |
| — A outputs | | 2.4 | | | V | $I_{OH} = -1$ mA |
| Input clamp voltage | $V_C$ | | | −1 | V | $I_C = -5$ mA |
| Input forward current | $I_F$ | | | −0.2 | μA | $V_F = 0.45$ V |
| Input reverse current | $I_R$ | | | 50 | μA | $V_R = 5.25$ V |
| Power supply current | $I_{CC}$ | | | | | |
| μPB8287 | | | | 130 | mA | |
| μPB8286 | | | | 160 | mA | |
| Output off current | $I_{OFF}$ | | | $I_F$ | | $V_{OFF} = 0.45$ V |
| Output off current | $I_{OFF}$ | | | $I_R$ | | $V_{OFF} = 5.25$ V |

**Note:**

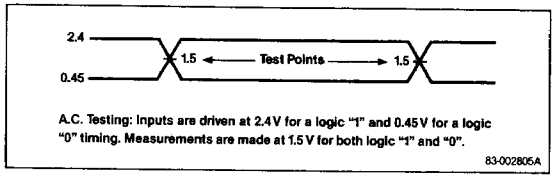
(1) B outputs — $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF
A outputs — $I_{OL} = 16$ mA, $I_{OH} = -1$ mA, $C_L = 100$ pF

## AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\,V \pm 10\%$

| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input to output delay | $t_{IVOV}$ | | | | | |
| Inverting | | 5 | | 22 | ns | |
| Non-inverting | | 5 | | 30 | ns | |
| Transmit / receive hold time | $t_{EHTV}$ | $t_{EHOZ}$ | | | ns | |
| Transmit / receive setup | $t_{TVEL}$ | 10 | | | ns | |
| Output disable time | $t_{EHOZ}$ | 5 | | 22 | ns | |
| Output enable time | $t_{ELOV}$ | 10 | | 30 | ns | |
| I / O rise time | $t_{ILIH}$ $t_{OLOH}$ | | | 20 | ns | |
| I / O fall time | $t_{IHIL}$ $t_{OHOL}$ | | | 12 | ns | |

### AC Test Conditions




A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0" timing. Measurements are made at 1.5 V for both logic "1" and "0".

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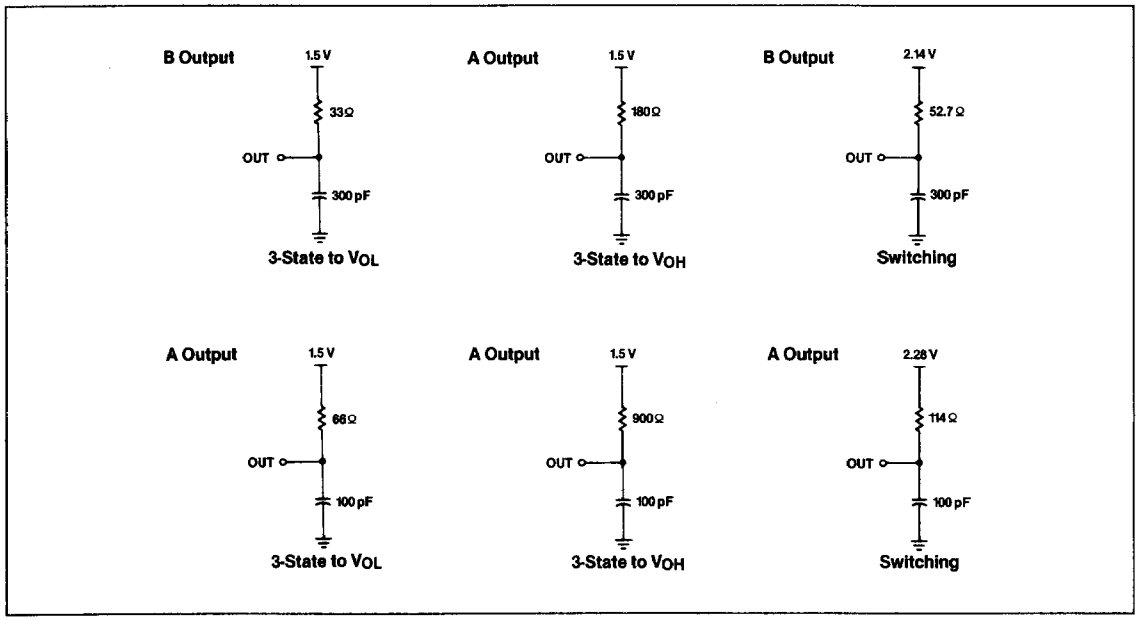
8

### *Test Load Circuits*




## Timing Waveform