

1 TMS320C6455 Fixed-Point Digital Signal Processor

1.1 Features

- **High-Performance Fixed-Point DSP (C6455)**
 - 1.39-, 1.17-, 1-ns Instruction Cycle Time
 - 720-, 850-MHz and 1-GHz Clock Rate
 - Eight 32-Bit Instructions/Cycle
 - 5760, 6800, 8000 MIPS
 - 5760, 6800, 8000 MMACS (16 Bits)
 - Commercial Temperature [0°C to 90°C]
- **TMS320C64x+™ DSP Core**
 - Dedicated SPLOOP Instruction
 - Compact Instructions (32-/16-Bit)
 - Instruction Set Enhancements
 - Exception Handling
- **TMS320C64x+ Megamodule**
- **L1/L2 Memory Architecture:**
 - 256K-Bit (32K-Byte) L1P Program Cache [Direct Mapped]
 - 256K-Bit (32K-Byte) L1D Data Cache [2-Way Set-Associative]
 - 16M-Bit (2048K-Byte) L2 Unified Mapped RAM/Cache [Flexible Allocation]
- **Enhanced Viterbi Decoder Coprocessor (VCP2)**
 - Supports Over 694 7.95-Kbps AMR
 - Programmable Code Parameters
- **Enhanced Turbo Decoder Coprocessor (TCP2)**
 - Supports up to Eight 2-Mbps 3GPP (6 Iterations)
 - Programmable Turbo Code and Decoding Parameters
- **Endianess: Little Endian, Big Endian**
- **64-Bit/133-MHz EMIFA**
 - Glueless Interface to Asynchronous Memories (SRAM, Flash, and EPROM)
 - Glueless Interface to Synchronous Memories (SBSRAM and ZBT SRAM)
 - Supports Interface to Standard Sync Devices
 - Sync or Async Interface to Custom Logic (FPGA, CPLD, ASICs, etc.)
 - 32M-Byte Total Addressable External Memory Space (8MB per CE space)
- **32-Bit DDR2 EMIF (DDR2-500 SDRAM)**
- **EDMA Controller (64 Independent Channels)**
- **Four 1x Serial RapidIO® Links (or One 4x), v1.2 Compliant**
 - 1.25-, 2.5-, 3.125-Gbps Link Rates
 - Message Passing, DirectIO Support, Error Management Extensions, and Congestion Control
 - IEEE 1149.6 Compliant I/Os
- **32-/16-Bit Host-Port Interface (HPI)**
- **32-Bit/66-MHz, 3.3-V Peripheral Component Interconnect (PCI) Master/Slave Interface**
 - Conforms to PCI Specification 2.3
- **One Inter-Integrated Circuit (I²C) Bus**
- **Two Multichannel Buffered Serial Ports (McBSPs)**
- **10/100/1000 Mb/s Ethernet MAC (EMAC)**
 - IEEE 802.3 Compliant
 - Supports Multiple Media Independent Interfaces (MII, GMII, RMII, and RGMII)
 - 8 Independent Transmit (TX) and 8 Independent Received (RX) Channels
- **Two 64-Bit General-Purpose Timers, Configurable as Four 32-Bit Timers**
- **Universal Test and Operations PHY Interface for ATM (UTOPIA)**
 - UTOPIA Level 2 Slave ATM Controller
 - 8-Bit Transmit and Receive Operations up to 50 MHz per Direction
 - User-Defined Cell Format up to 64 Bytes
- **16 General-Purpose I/O (GPIO) Pins**
- **PLL1 and PLL1 Controller**
- **PLL2 Dedicated for DDR2 EMIF and EMAC**
- **IEEE-1149.1 (JTAG) Boundary-Scan-Compatible**
- **697-Pin Ball Grid Array (BGA) Package (ZTZ Suffix), 0.8-mm Ball Pitch**
- **0.09-µm/7-Level Cu Metal Process (CMOS)**
- **3.3-, 1.8-, 1.5-, 1.2-V I/Os, 1.2-V Internal**



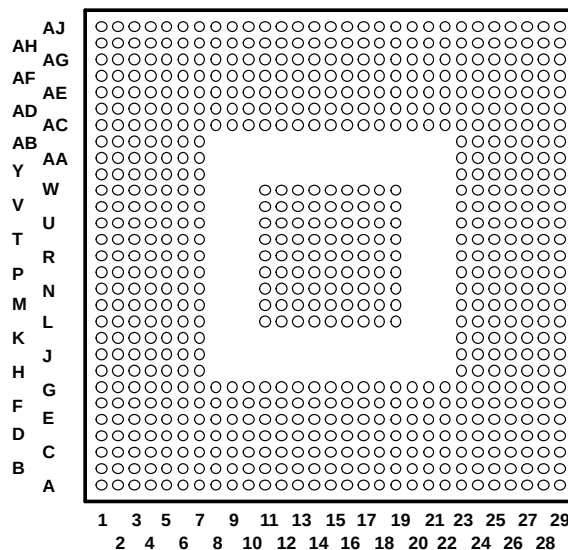
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1.1.1 ZTZ BGA Package (Bottom View)

The TMS320C6455 devices are designed for a package temperature range of 0°C to +90°C (commercial temperature range).

**ZTZ 697-PIN BALL GRID ARRAY (BGA) PACKAGE
(BOTTOM VIEW)**



NOTE: The ZTZ mechanical package designator represents the version of the GTZ package with lead-free balls. For more detailed information, see the *Mechanical Data* section of this document.

Figure 1-1. ZTZ BGA Package (Bottom View)

1.2 Description

The TMS320C64x+™ DSPs (including the TMS320C6455 device) are the highest-performance fixed-point DSP generation in the TMS320C6000™ DSP platform. The C6455 device is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for applications including video and telecom infrastructures, imaging/medical, and wireless infrastructure (WI). The C64x+™ devices are upward code-compatible from previous devices that are part of the C6000™ DSP platform.

Based on 90-nm process technology and with performance of up to 8000 million instructions per second (MIPS) [or 8000 16-bit MMACs per cycle] at a clock rate of 1 GHz, the C6455 device offers cost-effective solutions to high-performance DSP programming challenges. The C6455 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors.

The C64x+ DSP core employs eight functional units, two register files, and two data paths. Like the earlier C6000 devices, two of these eight functional units are multipliers or .M units. Each C64x+ .M unit doubles the multiply throughput versus the C64x core by performing four 16-bit x 16-bit multiply-accumulates (MACs) every clock cycle. Thus, eight 16-bit x 16-bit MACs can be executed every cycle on the C64x+ core. At a 1-GHz clock rate, this means 8000 16-bit MMACs can occur every second. Moreover, each multiplier on the C64x+ core can compute one 32-bit x 32-bit MAC or four 8-bit x 8-bit MACs every clock cycle.

The C6455 device has two high-performance embedded coprocessors [enhanced Viterbi Decoder Coprocessor (VCP2) and enhanced Turbo Decoder Coprocessor (TCP2)] that significantly speed up channel-decoding operations on-chip. The VCP2 operating at CPU clock divided-by-3 can decode over 694 7.95-Kbps adaptive multi-rate (AMR) [$K = 9$, $R = 1/3$] voice channels. The VCP2 supports constraint lengths $K = 5, 6, 7, 8$, and 9 , rates $R = 3/4, 1/2, 1/3, 1/4$, and $1/5$ and flexible polynomials, while generating hard decisions or soft decisions. The TCP2 operating at CPU clock divided-by-3 can decode up to fifty 384-Kbps or eight 2-Mbps turbo encoded channels (assuming 6 iterations). The TCP2 implements the max*log-map algorithm and is designed to support all polynomials and rates required by Third-Generation Partnership Projects (3GPP and 3GPP2), with fully programmable frame length and turbo interleaver. Decoding parameters such as the number of iterations and stopping criteria are also programmable. Communications between the VCP2/TCP2 and the CPU are carried out through the EDMA controller.

The C6455 DSP integrates a large amount of on-chip memory organized as a two-level memory system. The level-1 (L1) program and data memories on the C6455 device are 32KB each. This memory can be configured as mapped RAM, cache, or some combination of the two. When configured as cache, L1 program (L1P) is a direct mapped cache where as L1 data (L1D) is a two-way set associative cache. The level 2 (L2) memory is shared between program and data space and is 2MB in size. L2 memory can also be configured as mapped RAM, cache, or some combination of the two. The C64x+ Megamodule also has a 32-bit peripheral configuration (CFG) port, an internal DMA (IDMA) controller, a system component with reset/boot control, interrupt/exception control, a power-down control, and a free-running 32-bit timer for time stamp.

The C6455 device includes Serial RapidIO®. This high bandwidth peripheral dramatically improves system performance and reduces system cost for applications that include multiple DSPs on a board, such as video and telecom infrastructures and medical/imaging.

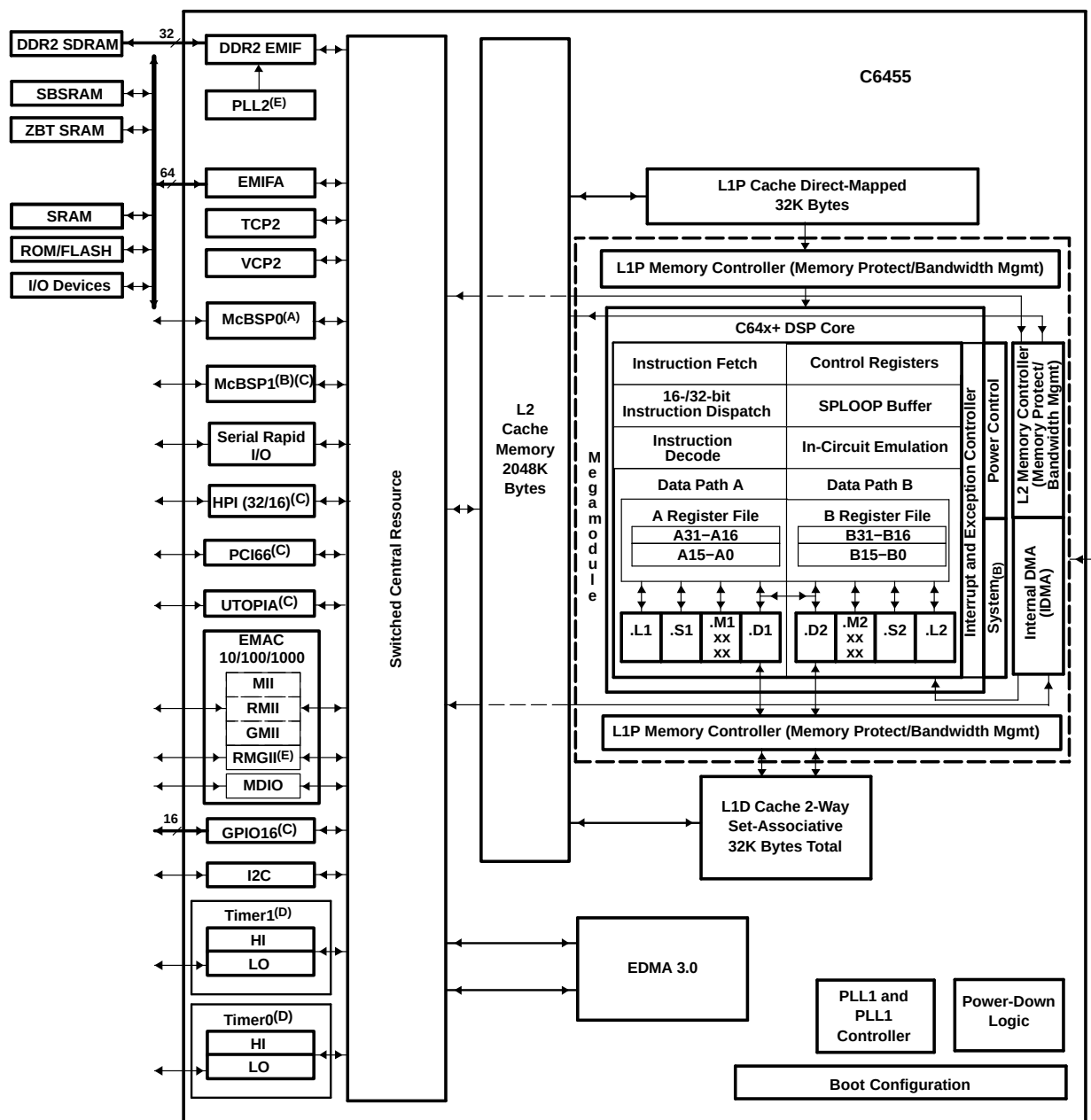
The peripheral set also includes: an inter-integrated circuit bus module (I2C); two multichannel buffered serial ports (McBSPs); an 8-bit Universal Test and Operations PHY Interface for Asynchronous Transfer Mode (ATM) Slave [UTOPIA Slave] port; two 64-bit general-purpose timers (also configurable as four 32-bit timers); a user-configurable 16-bit or 32-bit host-port interface (HPI16/HPI32); a peripheral component interconnect (PCI); a 16-pin general-purpose input/output port (GPIO) with programmable interrupt/event generation modes; an 10/100/1000 Ethernet media access controller (EMAC), which provides an efficient interface between the C6455 DSP core processor and the network; a management data input/output (MDIO) module (also part of the EMAC) that continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system; a glueless external memory interface (64-bit EMIFA), which is capable of interfacing to synchronous and asynchronous peripherals; and a 32-bit DDR2 SDRAM interface.

The I2C ports on the C6455 allow the DSP to easily control peripheral devices and communicate with a host processor. In addition, the standard multichannel buffered serial port (McBSP) may be used to communicate with serial peripheral interface (SPI) mode peripheral devices.

The C6455 has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows® debugger interface for visibility into source code execution.

1.3 Functional Block Diagram

Figure 1-2 shows the functional block diagram of the C6455 device.



- A. McBSPs: Framing Chips – H.100, MVIP, SCSA, T1, E1; AC97 Devices; SPI Devices; Codecs
 B. System consists of Test, Emulation, Power Down, and Interrupt Controller.
 C. The PCI peripheral pins are MUXED with some of the HPI, UTOPIA, McBSP1, and GPIO peripheral pins.
 D. Each of the TIMER peripherals (TIMER1 and TIMER0) is configurable as either two 64-bit general-purpose timer **or** two 32-bit general-purpose timers **or** a watchdog timer.
 E. The PLL2 peripheral is also used for the RGMII mode of the EMAC.

Figure 1-2. Functional Block Diagram

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2 Device Overview

2.1 Device Characteristics

[Table 2-1](#), provides an overview of the C6455 DSP. The tables show significant features of the C6455 device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count.

Table 2-1. Characteristics of the C6455 Processor

	HARDWARE FEATURES	C6455
Peripherals Not all peripherals pins are available at the same time (For more detail, see the Device Configuration section).	EMIFA (64-bit bus width) [133 MHz] (clock source = AECLKIN or SYSCLK3)	1
	DDR2 EMIF (32-bit bus width) [1.8 V I/O] (clock source = CLKIN2)	1
	EDMA (64 independent channels) [CPU/3 clock rate]	1
	High-speed 1x/4x Serial Rapid IO Port (RIOCLK and RIOCLK)	1
	I2C	1
	HPI (32- or 16-bit user selectable)	1 (HPI16 or HPI32)
	PCI (32-bit), [66-MHz or 33-MHz]	1 (PCI66 or PCI33)
	McBSPs (internal CPU/12 or external clock source up to 100 Mbps)	2
	UTOPIA (8-bit mode, 50-MHz, Slave-only)	1
	10/100/1000 Ethernet MAC (EMAC)	1
	Management Data Input/Output (MDIO)	1
	64-Bit Timers (Configurable) (internal clock source = CPU/6 clock frequency)	2 64-bit or 4 32-bit
	General-Purpose Input/Output Port (GPIO)	16
Decoder Coprocessors	VCP2 (clock source = CPU/3 clock frequency)	1
	TCP2 (clock source = CPU/3 clock frequency)	1
On-Chip Memory	Size (Bytes)	2112K
	Organization	32K-Byte (32KB) L1 Program Memory Controller [SRAM/Cache] 32KB Data Memory Controller [SRAM/Cache] 2048KB L2 Unified Memory/Cache
CPU MegaModule Revision ID	Revision ID Register (MM_REVID.[15:0]) 0x0181 2000	0x0
JTAG BSDL_ID	JTAGID register (address location: 0x02A80008)	0x0008 A02F
Frequency	MHz	720, 850, and 1000 (1-GHz)
Cycle Time	ns	1.39 ns (C6455-720), 1.17 ns (C6455-850), 1 ns (C6455-1000) [1 GHz CPU]
Voltage	Core (V)	1.2 V (-720, -850, -1000)
	I/O (V)	1.2 [RapidIO], 1.5/1.8 [EMAC RGMII], and 1.8 and 3.3 V [I/O Supply Voltage]
PLL1 and PLL1 Controller Options	CLKIN frequency multiplier	Bypass (x1), x20, x25, x30, x32
PLL2	CLKIN frequency multiplier [DDR2 EMIF and EMAC support only]	x10
BGA Package	24 x 24 mm	697-Pin Flip-Chip Plastic BGA (ZTZ)
Process Technology	μm	0.09 μm
Product Status ⁽¹⁾	Product Preview (PP), Advance Information (AI), or Production Data (PD)	PP
Device Part Numbers	(For more details on the C64x+™ DSP part numbering, see Figure 2-9)	TMX320C6455ZTZ720, TMX320C6455ZTZ850, TMX320C6455ZTZ1

(1) PRODUCT PREVIEW information concerns experimental products (designated as TMX) that are in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

2.2 CPU (DSP Core) Description

The C64x+ Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in [Figure 2-1](#). The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C64x+ CPU extends the performance of the C64x core through enhancements and new features.

Each C64x+ .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes for 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for audio and other high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C64x+ core enhances the .S unit in several ways. In the C64x core, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C64x+ core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

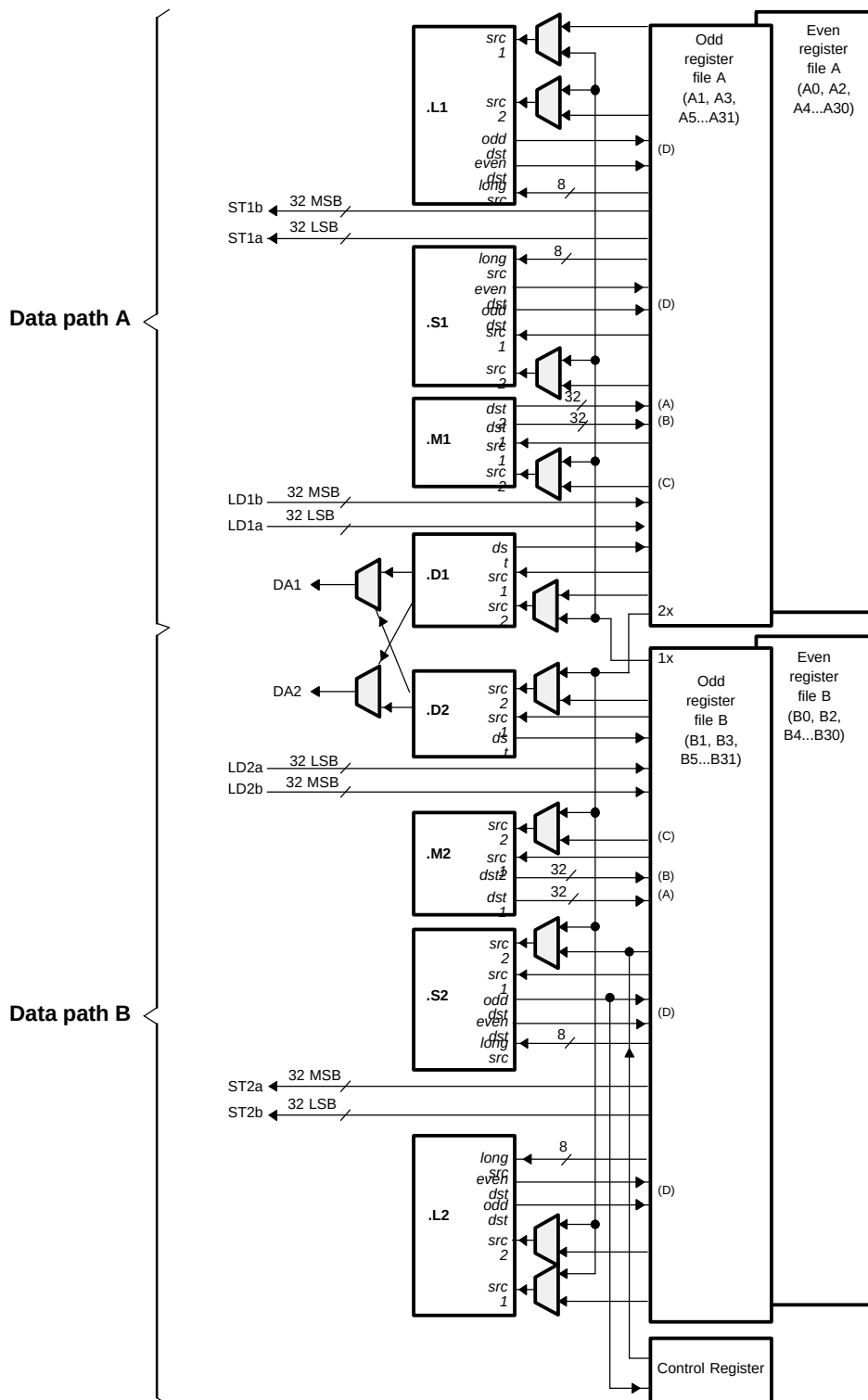
Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 obits if the C64x+ compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C64x+ CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.

- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is **not** sensitive to system stalls.

For more details on the C64x+ CPU and its enhancements over the C64x architecture, see the following documents:

- *C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRUTBD)
- *C64x+ DSP Cache User's Guide* (literature number SPRUTBD)
- *C64x+ Megamodule Peripherals Reference Guide* (literature number SPRUTBD)
- *C64x+ DSP Technical Overview* (literature number [SPRU965](#))
- *C64x to C64x+ CPU Migration Guide* (literature number SPRAATBD)



- A. On .M unit, *dst2* is 32 MSB.
- B. On .M unit, *dst1* is 32 LSB.
- C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
- D. On .L and .S units, *odd dst* connects to odd register files and *even dst* connects to even register files.

Figure 2-1. TMS320C64x+™ CPU (DSP Core) Data Paths

PRODUCT PREVIEW

2.3 Memory Map Summary

Table 2-2 shows the memory map address ranges of the C6455 device. The external memory configuration register address ranges in the C6455 device begin at the hex address location 0x7000 0000 for EMIFA and hex address location 0x7800 0000 for DDR2 EMIF.

Table 2-2. C6455 Memory Map Summary

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
Reserved	1024K	0000 0000 - 000F FFFF
Reserved	32K	0010 0000 - 0010 7FFF
Reserved	7M - 32K	0010 8000 - 007F FFFF
Internal RAM (L2) [L2 SRAM]	2M	0080 0000 - 009F FFFF
Reserved	4M	00A0 0000 - 00DF FFFF
L1P SRAM	32K	00E0 0000 - 00E0 7FFF
Reserved	1M - 32K	00E0 8000 - 00EF FFFF
L1D SRAM	32K	00F0 0000 - 00F0 7FFF
Reserved	1M - 32K	00F0 8000 - 00FF FFFF
Reserved	8M	0100 0000 - 017F FFFF
CPU MegaModule Interrupt Controller	64K	0180 0000 - 0180 FFFF
CPU MegaModule Powerdown Status	64K	0181 0000 - 0181 FFFF
CPU MegaModule IDMA Registers	64K	0182 0000 - 0182 01FF
CPU MegaModule BandWidth Management Control Registers	768	0182 0200 - 0182 02FF
CPU MegaModule Configuration Registers	130K	0182 0300 - 0183 FFFF
CPU MegaModule Cache Configuration Registers	3.5K	0184 0000 - 0184 0DFF
CPU MegaModule BandWidth Management L1D and L2 Registers	12.8K	0184 0E00 - 0184 3FFF
CPU MegaModule Cache Status and Control Registers	8K	0184 4000 - 0184 5FFF
Reserved	8K	0184 6000 - 0184 7FFF
CPU MegaModule Cache MAR Registers	8K	0184 8000 - 0184 9FFF
CPU MegaModule Memory Protection Registers	8K	0184 A000 - 0184 BFFF
CPU MegaModule L1/L2 Control Registers	128K	0184 0000 - 0185 FFFF
Reserved	128K - 16	0186 0000 - 0187 FFF0
Reserved	3.4M	0187 FFFC - 01BB FFFF
Emulation	256K	01BC 0000 - 01BF FFFF
Reserved	12.5M	01C0 0000 - 0287 FFFF
HPI Control Registers	256K	0288 0000 - 028B FFFF
McBSP 0 Registers	256K	028C 0000 - 028F FFFF
McBSP 1 Registers	256K	0290 0000 - 0293 FFFF
Timer 0 Registers	256K	0294 0000 - 0297 FFFF
Timer 1 Registers	128K	0298 0000 - 0299 FFFF
PLL1 Controller	512	029A 0000 - 029A 01FF
Reserved	512K - 512	029C 0200 - 029C 02FF
EDMA3.0 - CC Registers	32K	02A0 0000 - 02A0 7FFF
Reserved	96K	02A0 8000 - 02A1 FFFF
Reserved	32K	02A2 0000 - 02A2 7FFF
Reserved	32K	02A2 8000 - 02A2 FFFF
Reserved	32K	02A3 0000 - 02A3 7FFF
Reserved	32K	02A3 8000 - 02A3 FFFF

Table 2-2. C6455 Memory Map Summary (continued)

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
Reserved	256K	02A4 0000 - 02A7 FFFF
Chip-Level Registers	256K	02A8 0000 - 02AB FFFF
Powersaver Registers	256K	02AC 0000 - 02AF FFFF
GPIO Registers	16K	02B0 0000 - 02B0 3FFF
I2C Data and Control Registers	256K	02B0 4000 - 02B3 FFFF
UTOPiA Control Registers	512	02B4 0000 - 02B4 01FF
Reserved	256K - 512	02B4 0200 - 02B7 FFFF
VCP2 Control Registers	128K	02B8 0000 - 02B9 FFFF
TCP2 Control Registers	128K	02BA 0000 - 02BB FFFF
Reserved	256K	02BC 0000 - 02BF FFFF
PCI Control Registers	256K	02C0 0000 - 02C3 FFFF
Reserved	256K	02C4 0000 - 02C7 FFFF
EMAC Control	4K	02C8 0000 - 02C8 0FFF
EMAC Wrapper Control	2K	02C8 1000 - 02C8 17FF
MDIO Control Registers	2K	02C8 1800 - 02C8 1FFF
EMAC CPPI RAM	8K	02C8 2000 - 02C8 3FFF
Reserved	496K	02C8 4000 - 02CF FFFF
RapidIO Control Registers	256K	02D0 0000 - 02D3 FFFF
Reserved	768K	02D4 0000 - 02DF FFFF
RapidIO CPPI RAM	16K	02E0 0000 - 02E0 3FFF
Reserved	2M - 16K	02E0 4000 - 02FF FFFF
Reserved	16M	0300 0000 - 03FF FFFF
Reserved	192M	0400 0000 - 0FFF FFFF
Reserved	256M	1000 0000 - 1FFF FFFF
Reserved	256M	2000 0000 - 2FFF FFFF
McBSP 0 Data	256	3000 0000 - 3000 00FF
Reserved	64M - 256	3000 0100 - 33FF FFFF
McBSP 1 Data	256	3400 0000 - 3400 00FF
Reserved	64M - 256	3400 0100 - 37FF FFFF
Reserved	64M	3800 0000 - 3BFF FFFF
UTOPiA Rx Data Registers	1K	3C00 0000 - 3C00 03FF
UTOPiA Tx Data Registers	1K	3C00 0400 - 3C00 07FF
Reserved	16M - 2K	3C00 0800 - 3CFF FFFF
Reserved	48M	3D00 0000 - 3FFF FFFF
Reserved	256M	4000 0000 - 4FFF FFFF
TCP2 Data Registers	128M	5000 0000 - 57FF FFFF
VCP2 Data Registers	128M	5800 0000 - 5FFF FFFF
Reserved	256M	6000 0000 - 6FFF FFFF
EMIFA (EMIF64) Configuration Registers	128M	7000 0000 - 77FF FFFF
DDR2 EMIF Configuration Registers	128M	7800 0000 - 7FFF FFFF
Reserved	256M	8000 0000 - 8FFF FFFF
Reserved	256M	9000 0000 - 9FFF FFFF
EMIFA CE2 - SBSRAM/Async ⁽¹⁾	256M	A000 0000 - AFFF FFFF
EMIFA CE3 - SBSRAM/Async ⁽¹⁾	256M	B000 0000 - BFFF FFFF
EMIFA CE4 - SBSRAM/Async ⁽¹⁾	256M	C000 0000 - CFFF FFFF
EMIFA CE5 - SBSRAM/Async ⁽¹⁾	256M	D000 0000 - DFFF FFFF

(1) The EMIFA $\overline{\text{CE0}}$ and $\overline{\text{CE1}}$ are **not** functionally supported on the C6455 device, and therefore, are **not** pinned out.

Table 2-2. C6455 Memory Map Summary (continued)

MEMORY BLOCK DESCRIPTION	BLOCK SIZE (BYTES)	HEX ADDRESS RANGE
DDR2 EMIF CE0 - DDR2 SDRAM	256M	E000 0000 - EFFF FFFF
Reserved	256M	F000 0000 - FFFF FFFF

2.4 Bootmode

The C6455 device resets using the active-low signal $\overline{\text{RESET}}$. While $\overline{\text{RESET}}$ is low, the device is held in reset and is initialized to the prescribed reset state. Refer to reset timing for reset timing characteristics and states of device pins during reset. The release of $\overline{\text{RESET}}$ starts the processor running with the prescribed device configuration and boot mode.

The C6455 has three types of boot modes:

- Host boot

If host boot is selected, upon release of $\overline{\text{RESET}}$, the CPU is internally "stalled" while the remainder of the device is released. During this period, an external host can initialize the CPU's memory space as necessary through the host interface, including internal configuration registers, such as those that control the EMIF or other peripherals. For the C6455 device, the HPI peripheral is used for host boot providing the $\overline{\text{PCI_EN}}$ pin is low, enabling the HPI peripheral [default]. Once the host is finished with all necessary initialization, it must set the DSPINT bit in the HPIC register to complete the boot process. This transition causes the boot configuration logic to bring the CPU out of the "stalled" state. The CPU then begins execution from address 0. The DSPINT condition is not latched by the CPU, because it occurs while the CPU is still internally "stalled". Also, DSPINT brings the CPU out of the "stalled" state only if the host boot process is selected. All memory may be written to and read by the host. This allows for the host to verify what it sends to the DSP if required. After the CPU is out of the "stalled" state, the CPU needs to clear the DSPINT, otherwise, no more DSPINTs can be received.

- EMIF boot (using default ROM timings)

Upon the release of $\overline{\text{RESET}}$, the device will begin executing software out of an Asynchronous 8-bit ROM located in EMIFA CE3 space.

- No boot

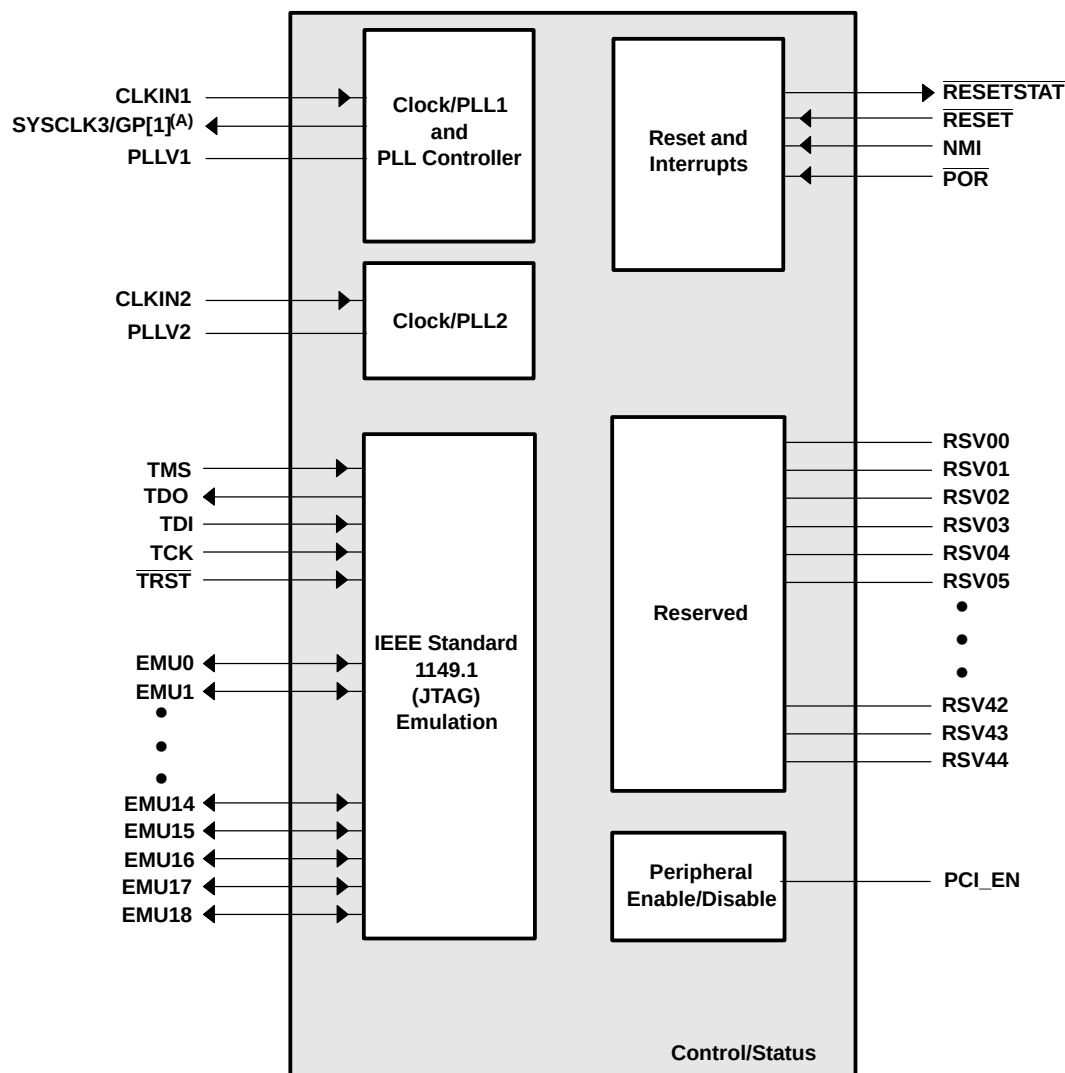
With no boot, the CPU begins direct execution from the memory located at address 0. Note: operation is undefined if invalid code is located at address 0.

2.5 Pin Assignments

2.5.1 Pin Map

TBD through TBD show the C6455 pin assignments in four quadrants (A, B, C, and D).

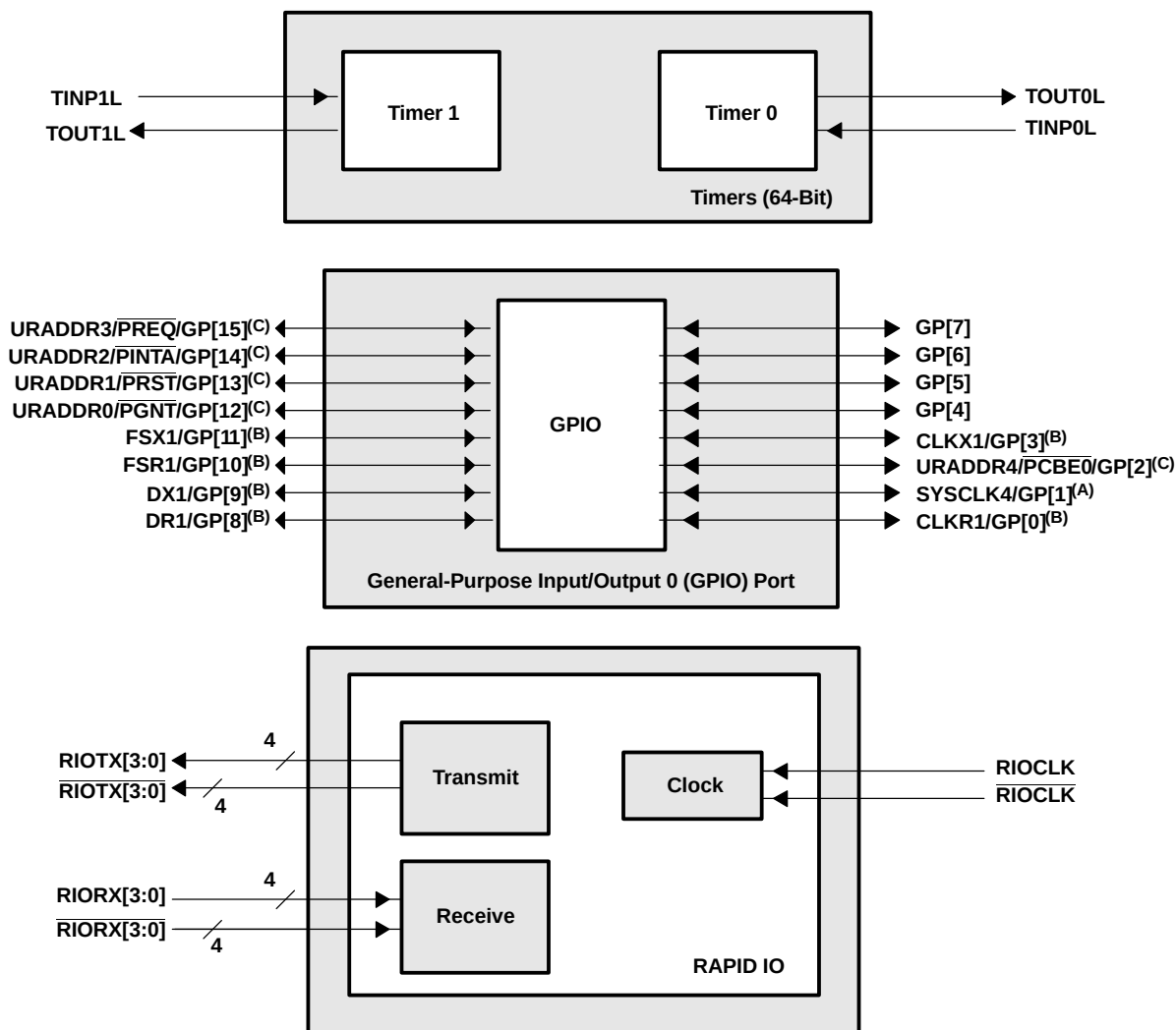
2.6 Signal Groups Description



A. This pin is muxed with the GP[1] pin and by default these signals function as GP[1]. For more details, see the Device Configurations section of this data sheet.

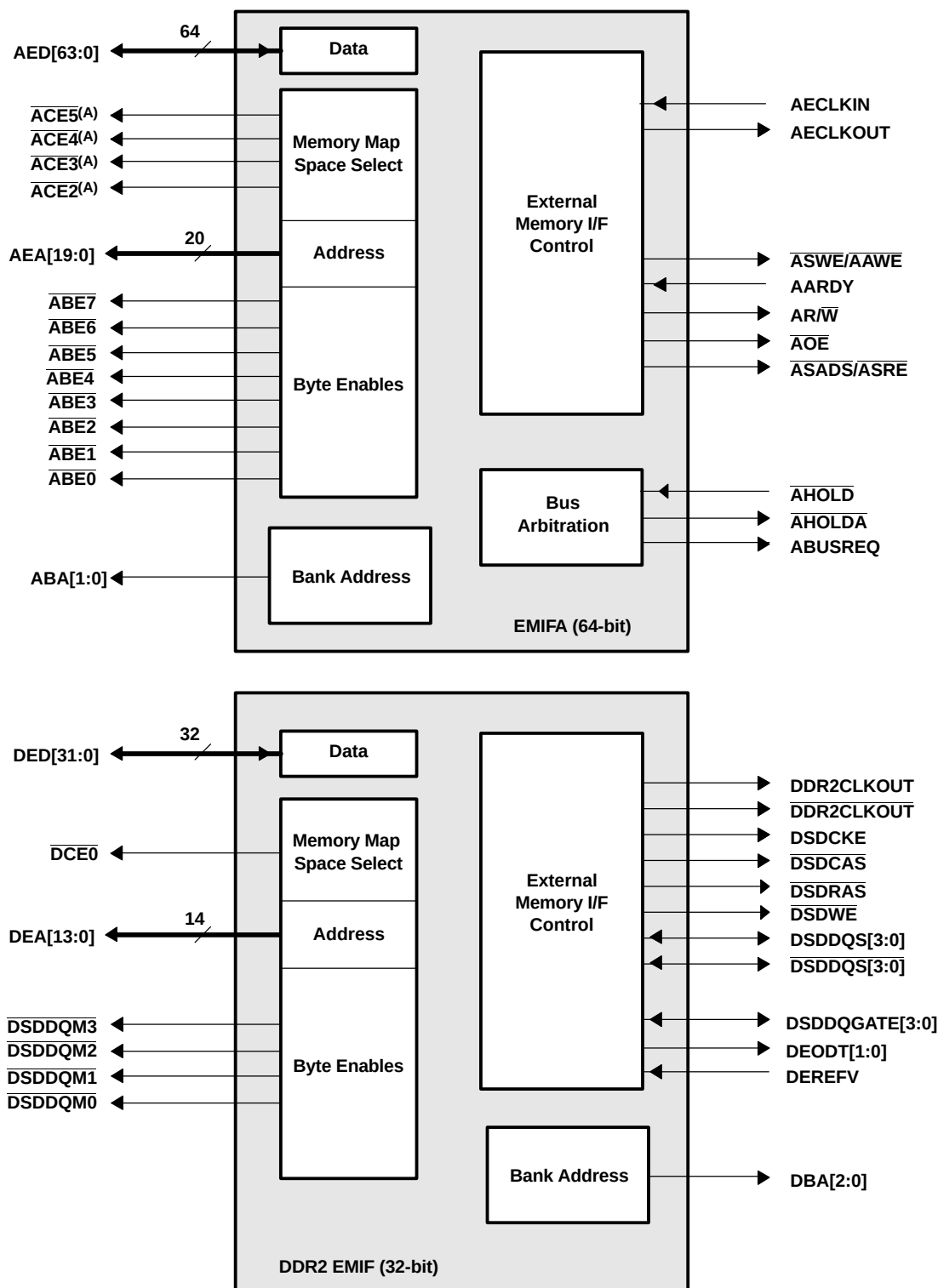
Figure 2-2. CPU and Peripheral Signals

PRODUCT PREVIEW



- A. This pin is muxed with the GP[1] pin and by default this signal functions as GP[1]. For more details, see the Device Configurations section of this data sheet.
- B. These McBSP1 peripheral pins are muxed with the GPIO peripheral pins and by default these signals function as GPIO peripheral pins. For more details, see the Device Configurations section of this data sheet.
- C. These UTOPIA and PCI peripheral pins are muxed with the GPIO peripheral pins and by default these signals function as GPIO peripheral pins. For more details, see the Device Configurations section of this data sheet.

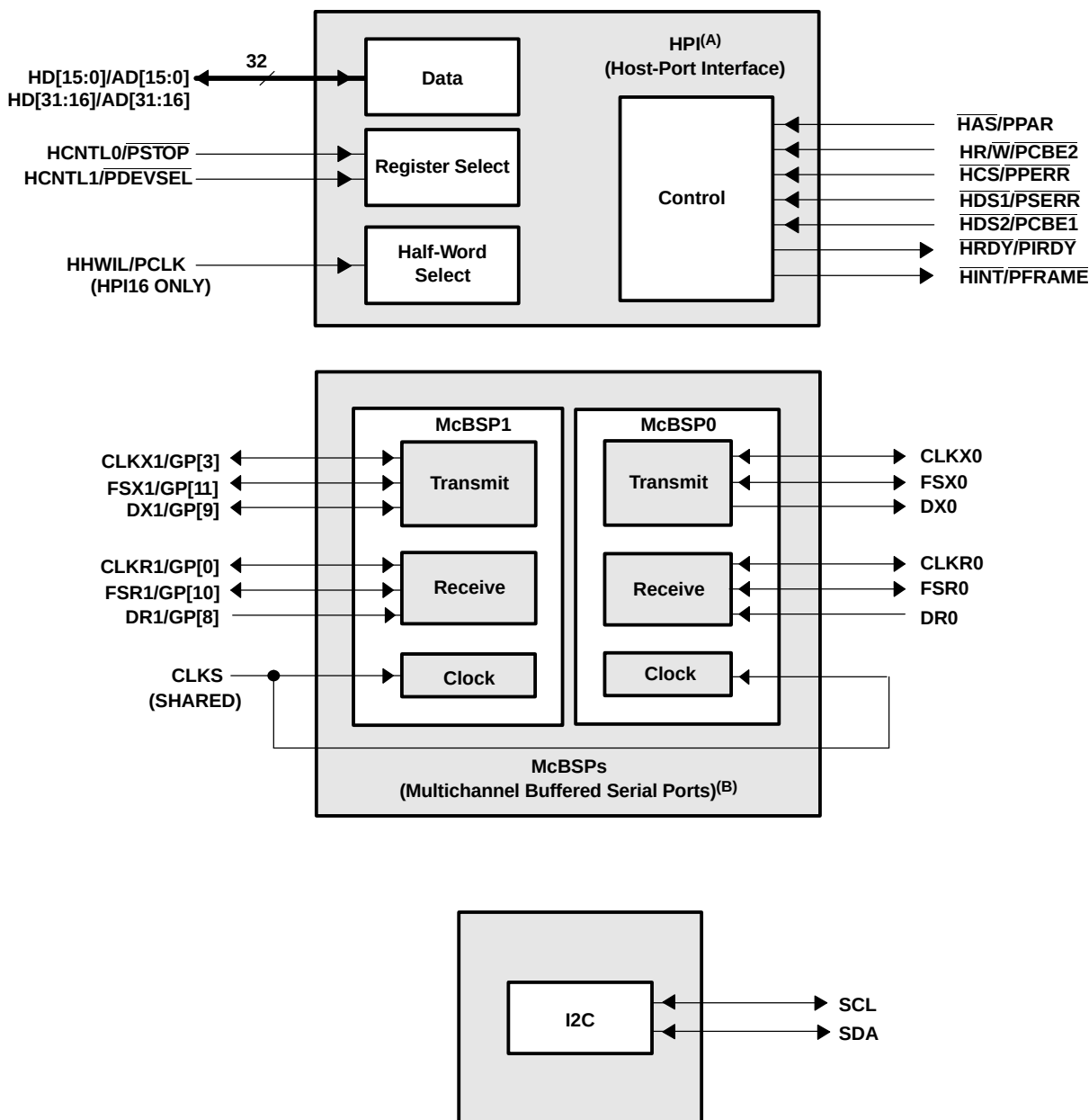
Figure 2-3. Timers/GPIO/RapidIO Peripheral Signals



A. The EMIFA $\overline{ACE0}$ and $\overline{ACE1}$ are **not** functionally supported on the C6455 device.

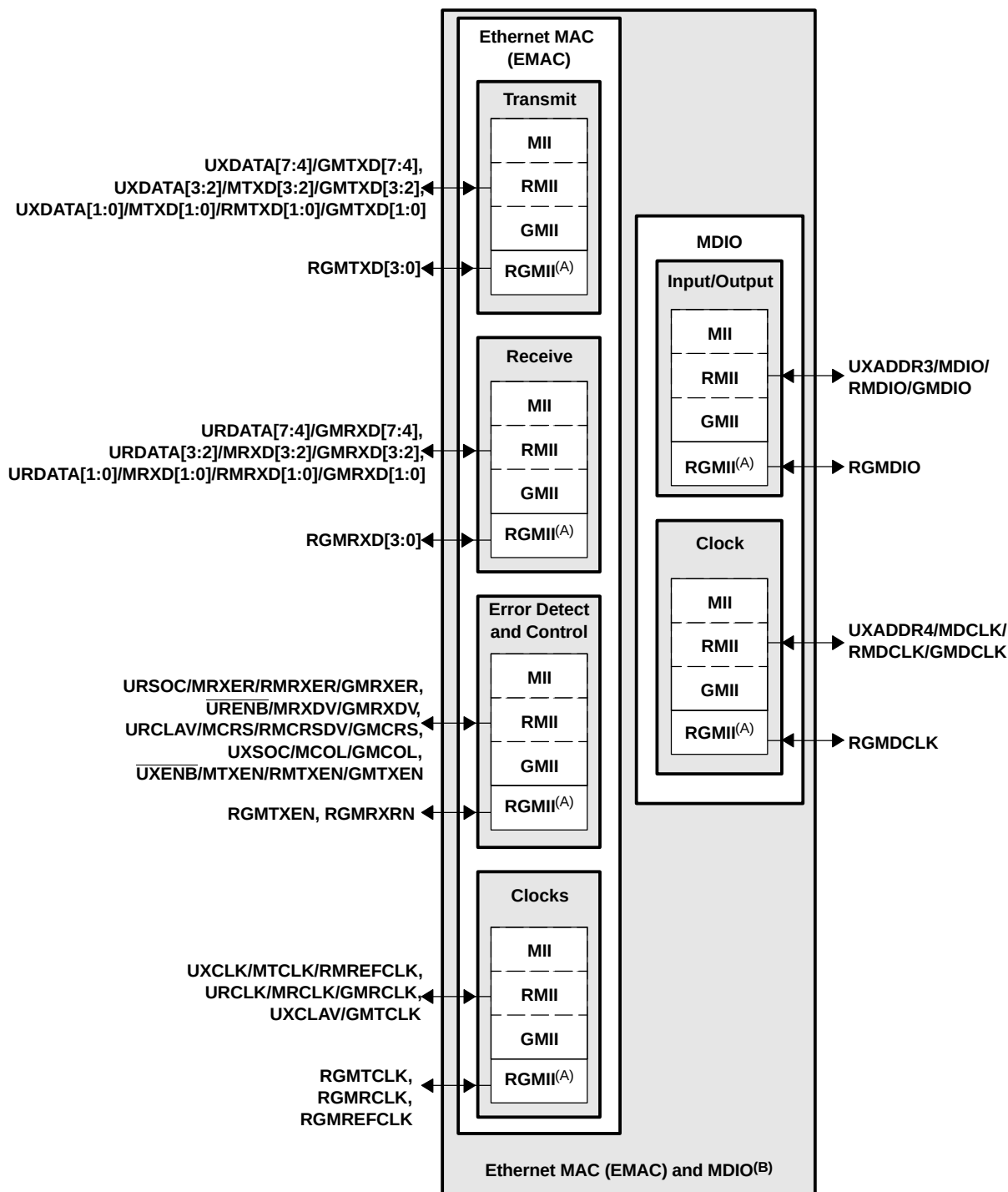
Figure 2-4. EMIFA/DDR2 EMIF Peripheral Signals

PRODUCT PREVIEW



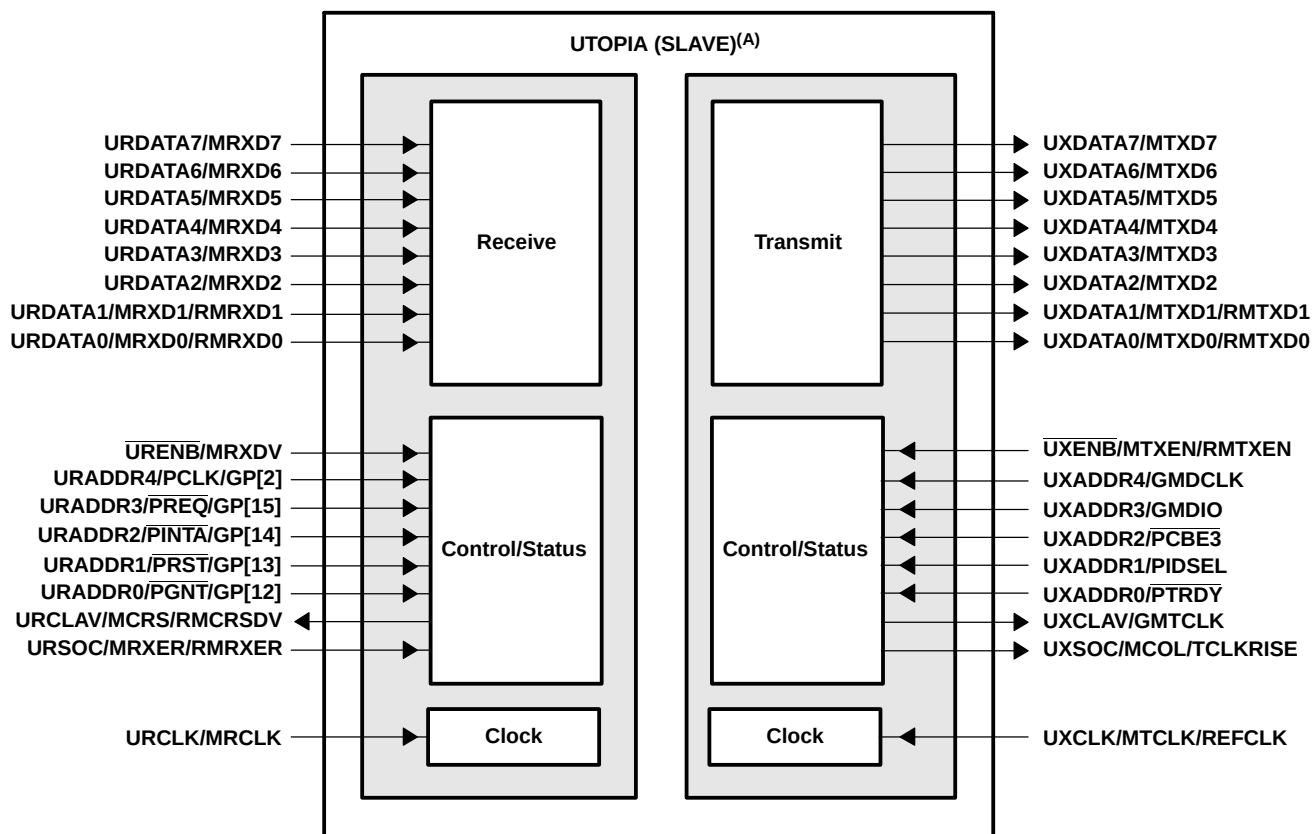
- A. These HPI pins are muxed with the PCI peripheral. By default, these pins function as HPI and no function, respectively. For more details on these muxed pins, see the Device Configurations section of this data sheet.
- B. These McBSP1 peripheral pins are muxed with the GPIO peripheral pins and by default these signals function as GPIO peripheral pins. For more details, see the Device Configurations section of this data sheet.

Figure 2-5. HPI/McBSP/I1C Peripheral Signals



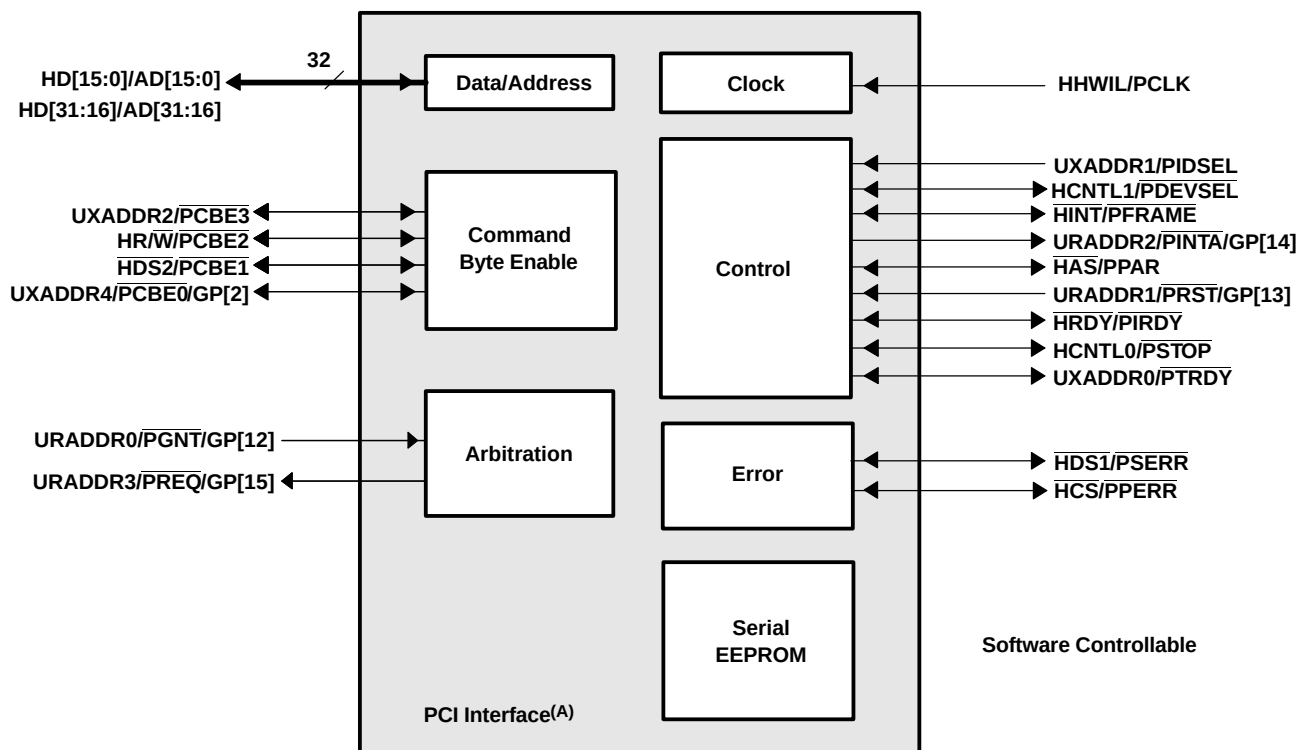
- A. RGMII signals are mutually exclusive to all other EMAC signals.
- B. These EMAC pins are muxed with the UTOPIA peripheral. By default, these signals function as EMAC. For more details on these muxed pins, see the Device Configurations section of this data sheet.

Figure 2-6. EMAC/MDIO [MII/RMII/GMII/RGMII Peripheral Signals



A. These UTOPIA pins are muxed with the PCI or EMAC or GPIO peripherals. By default, these signals function as GPIO or EMAC peripheral pins or no function, respectively. For more details on these muxed pins, see the Device Configurations section of this data sheet.

Figure 2-7. UTOPIA Peripheral Signals



A. These PCI pins are muxed with the HPI or UTOPIA or GPIO peripherals. By default, these signals function as HPI or GPIO or EMAC, respectively. For more details on these muxed pins, see the Device Configurations section of this data sheet.

Figure 2-8. PCI Peripheral Signals

PRODUCT PREVIEW

2.1 Terminal Functions

The terminal functions table ([Table 2-3](#)) identifies the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type (I, O/Z, or I/O/Z), whether the pin has any internal pullup/pulldown resistors and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and debugging considerations, see the Device Configurations section of this data sheet.

Table 2-3. Terminal Functions TBD

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
Clock/PLL Configurations				
CLKIN1		I	IPD	Clock Input for PLL1.
CLKIN2		I	IPD	Clock Input for PLL2.
PLL1V1		A		1.8-V I/O supply voltage for PLL1
PLL2V2		A		1.8-V I/O supply voltage for PLL2
SYSCLK3/GP[1] ⁽³⁾		I/O/Z	IPD	SYSCLK3 is the clock output at 1/8 of the device speed (O/Z) or this pin can be programmed as the GP1 pin (I/O/Z) [default].
JTAG EMULATION				
TMS		I	IPU	JTAG test-port mode select
TDO		O/Z	IPU	JTAG test-port data out
TDI		I	IPU	JTAG test-port data in
TCK		I	IPU	JTAG test-port clock
TRST		I	IPD	JTAG test-port reset. For IEEE 1149.1 JTAG compatibility, see the IEEE 1149.1 JTAG compatibility statement portion of this data sheet.
EMU0		I/O/Z	IPU	Emulation pin 0
EMU1		I/O/Z	IPU	Emulation pin 1
EMU2		I/O/Z	IPU	Emulation pin 2
EMU3		I/O/Z	IPU	Emulation pin 3
EMU4		I/O/Z	IPU	Emulation pin 4
EMU5		I/O/Z	IPU	Emulation pin 5
EMU6		I/O/Z	IPU	Emulation pin 6
EMU7		I/O/Z	IPU	Emulation pin 7
EMU8		I/O/Z	IPU	Emulation pin 8
EMU9		I/O/Z	IPU	Emulation pin 9
EMU10		I/O/Z	IPU	Emulation pin 10
EMU11		I/O/Z	IPU	Emulation pin 11
EMU12		I/O/Z	IPU	Emulation pin 12
EMU13		I/O/Z	IPU	Emulation pin 13
EMU14		I/O/Z	IPU	Emulation pin 14
EMU15		I/O/Z	IPU	Emulation pin 15
EMU16		I/O/Z	IPU	Emulation pin 16
EMU17		I/O/Z	IPU	Emulation pin 17
EMU18		I/O/Z	IPU	Emulation pin 18
RESETS, INTERRUPTS, AND GENERAL-PURPOSE INPUT/OUTPUTS				
RESET		I		Device reset
NMI		I	IPD	Nonmaskable interrupt, edge-driven (rising edge)

(1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal

(2) IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-k Ω IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-k Ω resistor should be used.)

(3) These pins are multiplexed pins. For more details, see the Device Configurations section of this data sheet.

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
RESETSTAT		O		Reset Status pin. The RESETSTAT pin indicates when the device is in reset
POR		I		Power on reset.
GP[7]		I/O/Z	IPD	General-purpose input/output (GPIO) pins (I/O/Z).
GP[6]		I/O/Z	IPD	
GP[5]		I/O/Z	IPD	
GP[4]		I/O/Z	IPD	
URADDR3/ PREQ / GP[15]		I/O/Z		UTOPIA received address pins or PCI peripheral pins or General-purpose input/output (GPIO) [15:12, 2] pins (I/O/Z) [default] PCI bus request (O/Z) or GP[15] (I/O/Z) [default] PCI interrupt A (O/Z) or GP[14] (I/O/Z) [default] PCI reset (I) or GP[13] (I/O/Z) [default] PCI bus grant (I) or GP[12] (I/O/Z) [default] PCI command/byte enable 3 (I/O/Z) or GP[2] (I/O/Z) [default] McBSP1 pins or GP[11:8] pins (I/O/Z) [default] McBSP1 transmit clock (I/O/Z) or GP[3] (I/O/Z) [default] McBSP1 receive clock (I/O/Z) or GP[0] (I/O/Z) [default] GP[1] pin (I/O/Z). SYSCLK3 is the clock output at 1/8 of the device speed (O/Z) or this pin can be programmed as a GP[1] pin (I/O/Z) [default].
URADDR2/ PINTA / GP[14]		I/O/Z		
URADDR1/ PRST / GP[13]		I/O/Z		
URADDR0/ PGNT / GP[12]		I/O/Z		
FSX1/GP[11]		I/O/Z	IPD	
FSR1/GP[10]		I/O/Z	IPD	
DX1/GP[9]		I/O/Z	IPD	
DR1/GP[8]		I/O/Z	IPD	
CLKX1/GP[3]		I/O/Z	IPD	
URADDR4/ PCBE0 / GP[2]		I/O/Z		
SYSCLK3/GP[1] ⁽³⁾		O/Z	IPD	
CLKR1/GP[0]		I/O/Z	IPD	
HOST-PORT INTERFACE (HPI) or PERIPHERAL COMPONENT INTERCONNECT (PCI)				
PCI_EN		I	IPD	PCI enable pin. This pin controls the selection (enable/disable) of the HPI and GP[15:8], or PCI peripherals. This pin works in conjunction with the MCBSP1_EN (AEA5 pin) to enable/disable other peripherals (for more details, see the Device Configurations section of this data sheet).
HINT/ PFRAME		I/O/Z		Host interrupt from DSP to host (O/Z) or PCI frame (I/O/Z)
HCNTL1/ PDEVSEL		I/O/Z		Host control - selects between control, address, or data registers (I) [default] or PCI device select (I/O/Z)
HCNTL0/ PSTOP		I/O/Z		Host control - selects between control, address, or data registers (I) [default] or PCI stop (I/O/Z)
HHWIL/ PCLK		I/O/Z		Host half-word select - first or second half-word (not necessarily high or low order) [For HPI16 bus width selection only] (I) [default] or PCI clock (I)
HR/ W / PCBE2		I/O/Z		Host read or write select (I) [default] or PCI command/byte enable 2 (I/O/Z)
HAS / PPAR		I/O/Z		Host address strobe (I) [default] or PCI parity (I/O/Z)
HCS / PPER		I/O/Z		Host chip select (I) [default] or PCI parity error (I/O/Z)
HDS1 / PSERR		I/O/Z		Host data strobe 1 (I) [default] or PCI system error (I/O/Z)
HDS2 / PCBE1		I/O/Z		Host data strobe 2 (I) [default] or PCI command/byte enable 1 (I/O/Z)
HRDY / PIRDY		I/O/Z		Host ready from DSP to host (O/Z) [default] or PCI initiator ready (I/O/Z)
URADDR3/ PREQ / GP[15]		I/O/Z		UTOPIA received address pin 3 (URADDR3) or PCI bus request (O/Z) or GP[15] (I/O/Z) [default]
URADDR2/ PINTA / GP[14]		I/O/Z		UTOPIA received address pin 2 or PCI interrupt A (O/Z) or GP[14] (I/O/Z) [default]
URADDR1/ PRST / GP[13]		I/O/Z		UTOPIA received address pin 1 (URADDR1) or PCI reset (I) or GP[13] (I/O/Z) [default]
URADDR0/ PGNT / GP[12]		I/O/Z		UTOPIA received address pin 0 (URADDR0) or PCI bus grant (I) or GP[12] (I/O/Z) [default]

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
URADDR4/ <u>PCBE0</u> / GP[2]		I/O/Z		UTOPIA received address pin 4 (URADDR4) or PCI bus grant (I) or GP[12] (I/O/Z) [default]
UXADDR2/ <u>PCBE3</u>		I/O/Z		UTOPIA transmit address pin 2 (UXADDR2) (I) or PCI command/byte enable 3 (I/O/Z)
UXADDR1/ <u>PIDSEL</u>		I		UTOPIA transmit address pin 1 (UXADDR1) (I) or PCI initialization device select (I)
UXADDR0/ <u>PIRDY</u>		I/O/Z		UTOPIA transmit address pin 0 (UXADDR0) (I) or PCI initiator ready (I/O/Z)
HD31/AD31		I/O/Z		Host-port data [31:16] pin (I/O/Z) [default] or PCI data-address bus [31:16] (I/O/Z)
HD30/AD30				
HD29/AD29				
HD28/AD28				
HD27/AD27				
HD26/AD26				
HD25/AD25				
HD24/AD24				
HD23/AD23				
HD22/AD22				
HD21/AD21				
HD20/AD20				
HD19/AD19				
HD18/AD18				
HD17/AD17				
HD16/AD16				
HD15/AD15		I/O/Z		Host-port data [15:0] pin (I/O/Z) [default] or PCI data-address bus [15:0] (I/O/Z)
HD14/AD14				
HD13/AD13				
HD12/AD12				
HD11/AD11				
HD10/AD10				
HD9/AD9				
HD8/AD8				
HD7/AD7				
HD6/AD6				
HD5/AD5				
HD4/AD4				
HD3/AD3				
HD2/AD2				
HD1/AD1				
HD0/AD0				

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
EMIFA (64-BIT) - CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY				
ABA1/EMIFA_EN		O/Z	IPD	EMIFA bank address control (ABA[1:0]) Active-low bank selects for the 64-bit EMIFA. When interfacing to 16-bit Asynchronous devices, ABA1 carries bit 1 of the byte address. For an 8-bit Asynchronous interface, ABA[1:0] are used to carry bits 1 and 0 of the byte address
ABA0/DDR2_EN		O/Z	IPD	DDR2 EMIF enable (DDR2_EN) [ABA0] 0 - DDR2 EMIF peripheral pins are disabled (default) 1 - DDR2 EMIF peripheral pins are enabled EMIFA enable (EMIFA_EN) [ABA1] 0 - EMIFA peripheral pins are disabled (default) 1 - EMIFA peripheral pins are enabled
$\overline{ACE5}$		O/Z	IPU	EMIFA memory space enables - Enabled by bits 28 through 31 of the word address - Only one pin is asserted during any external data access Note: The C6455 device does <i>not</i> have $\overline{ACE0}$ and $\overline{ACE1}$ pins
$\overline{ACE4}$		O/Z	IPU	
$\overline{ACE3}$		O/Z	IPU	
$\overline{ACE2}$		O/Z	IPU	
$\overline{ABE7}$		O/Z	IPU	
$\overline{ABE6}$		O/Z	IPU	
$\overline{ABE5}$		O/Z	IPU	
$\overline{ABE4}$		O/Z	IPU	
$\overline{ABE3}$		O/Z	IPU	
$\overline{ABE2}$		O/Z	IPU	
$\overline{ABE1}$		O/Z	IPU	
$\overline{ABE0}$		O/Z	IPU	
EMIFA (64-BIT) - BUS ARBITRATION				
AHOLDA		O	IPU	EMIFA hold-request-acknowledge to the host
AHOLD		I	IPU	EMIFA hold request from the host
ABUSREQ		O	IPU	EMIFA bus request output
EMIFA (64-BIT) - ASYNCHRONOUS/SYNCHRONOUS MEMORY CONTROL				
AECLKIN		I	IPD	EMIFA external input clock. The EMIFA input clock (AECLKIN or SYSCLK3 clock) is selected at reset via the pullup/pulldown resistor on the AEA[15] pin. Note: AECLKIN is the default for the EMIFA input clock.
AECLKOUT		O/Z	IPD	EMIFA output clock [at EMIFA input clock (AECLKIN or SYSCLK3) frequency]
$\overline{AAWE}/\overline{ASWE}$		O/Z	IPU	Asynchronous memory write-enable/Programmable synchronous interface write-enable
AARDY		I	IPU	Asynchronous memory ready input
$\overline{AR}/\overline{W}$		O/Z	IPU	Asynchronous/Programmable synchronous memory read/write
$\overline{AAOE}/\overline{ASOE}$		O/Z	IPU	Asynchronous/Programmable synchronous memory output-enable
$\overline{ASADS}/\overline{ASRE}$		O/Z	IPU	Programmable synchronous address strobe or read-enable - For programmable synchronous interface, the TBD field in the TBD Register selects between $\overline{ASADS}$ and $\overline{ASRE}$: - If TBD = 0, then the $\overline{ASADS}/\overline{ASRE}$ signal functions as the $\overline{ASADS}$ signal. - If TBD = 1, then the $\overline{ASADS}/\overline{ASRE}$ signal functions as the $\overline{ASRE}$ signal.

Table 2-3. Terminal Functions TBD (continued)

SIGNAL		TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
NAME	NO.			
EMIFA (64-BIT) - ADDRESS				
AEA19/BOOTMODE3		O/Z	IPD	EMIFA external address (word address) (O/Z) Controls initialization of the DSP modes at reset (I) via pullup/pulldown resistors [For more detailed information, see the <i>Device Configurations</i> section of this datasheet.] - Bootmode - device bootmode configurations (BOOTMODE[3:0]) AEA[19:16]: 0000 - No boot (default mode) 0001 - HPI/PCI boot 0010 -Reserved 0011 - Reserved 0100 - EMIFA 8-bit ROM boot 0101 - Reserved 0110 - Reserved 0111 - Reserved 1000 -Reserved 1001 - Reserved 1010 -Reserved Others - Reserved [1011 thru 1111] - EMIFA input clock source select Clock mode select for EMIFA (AECLKIN_SEL) AEA15: 0 - AECLKIN (default mode) 1 - SYSCLK3 (CPU/x) Clock Rate. The SYSCLK3 clock rate is software selectable via the Software PLL1 Controller. By default, SYSCLK3 is selected as CPU/8 clock rate. - HPI peripheral bus width (HPI_WIDTH) select [Applies only when HPI is enabled; PCI_EN pin = 0] AEA14: 0 - HPI operates as an HPI16 (default). (HPI bus is 16 bits wide. HD[15:0] pins are used and the remaining HD[31:16] pins are reserved pins in the Hi-Z state.) 1 - HPI operates as an HPI32. - Device Endian mode (LENDIAN) AEA13: 0 - System operates in Big Endian mode 1 - System operates in Little Endian mode(default) - UTOPIA Enable bit (UTOPIA_EN) AEA12: UTOPIA peripheral enable(functional) 0 - UTOPIA disabled; Ethernet MAC (EMAC) and MDIO enable(default). This means all multiplexed EMAC/UTOPIA and MDIO/UTOPIA pins function as EMAC and MDIO. Which EMAC/MDIO configuration (interface) [MII, RMII, GMII or the standalone RGMII] is controlled by the MACSEL[1:0] bits. 1 - UTOPIA enabled; EMAC and MDIO disabled [except when the MACSEL[1:0] bits = 11 then, the EMAC/MDIO RGMII interface is <i>still</i> functional]. This means all multiplexed EMAC/UTOPIA and MDIO/UTOPIA pins now function as UTOPIA. And if MACSEL[1:0] = 11, the RGMII standalone pin functions can be used. - EMAC/MDIO interface select bits (MACSEL[1:0]) If the EMAC and MDIO peripherals are enabled, AEA12 pin (UTOPIA_EN = 0) , there are two additional configuration pins — MACSEL[1:0] — to select the EMAC/MDIO interface. AEA[10:9]: MACSEL[1:0] with AEA12 =0. 00 - 10/100 EMAC/MDIO MII Mode Interface (default) 01 - 10/100 EMAC/MDIO RMII Mode Interface 10 - 10/100/1000 EMAC/MDIO GMII Mode Interface 11 - 0/100/1000 with RGMII Mode Interface [RGMII interface requires a 1.5 V I/O supply] When UTOPIA is enabled (AEA12 = 1), if the MACSEL[1:0] bits = 11 then, the EMAC/MDIO RGMII interface is <i>still</i> functional. For more detailed information, see the Device Configuraiton section of this data sheet.
AEA18/BOOTMODE2				
AEA17/BOOTMODE1				
AEA16/BOOTMODE0				
AEA15/AECLKIN_SEL				
AEA14/HPI_WIDTH		O/Z	IPU	
AEA13/LENDIAN				
AEA12/UTOPIA_EN				
AEA11				
AEA10/MACSEL1				
AEA9/MACSEL0		O/Z	IPD	

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
AEA8/PCI_EEAI		O/Z	IPD	- PCI EEPROM Auto-Initialization (PCI_EEAI) AEA8: PCI auto-initialization via external EEPROM If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must not be pulled up. 0 - PCI auto-initialization through EEPROM is disabled (default). 1 - PCI auto-initialization through EEPROM is enabled. - PCI Frequency Selection (PCI66) [The PCI peripheral <i>needs</i> be enabled (PCI_EN = 1) to use this function] Selects the PCI operating frequency of 66 MHz or 33 MHz PCI operating frequency is selected at reset via the pullup/pulldown resistor on the PCI66 pin: AEA6: 0 - PCI operates at 33 MHz (default). 1 - PCI operates at 66 MHz. Note: If the PCI peripheral is disabled (PCI_EN = 0), this pin must not be pulled up. - McBSP1 Enable bit (MCBSP1_EN) Selects which function is enabled on the McBSP1/GPIO muxed pins AEA5: 0 - GPIO pin functions enabled (default). 1 - McBSP1 pin functions enabled. - SYCLKOUT Enable bit (SYCLKOUT_EN) Selects which function is enabled on the SYCLK3/GP[1] muxed pin AEA4: 0 - GP[1] pin function of the SYCLK3/GP[1] pin enabled (default). 1 - SYCLK3 pin function of the SYCLK3/GP[1] pin enabled. - Configuration GPI (CFGGP[2:0]) (AEA[2:0]) These pins are latched during reset and their values are shown in the DEVSTAT register. These values can be used by S/W routines for boot operations. Note: For proper C6455 device operation, the AEA11 and AEA3 pins must be externally pulled up with a 1-kΩ resistor during Power-On Reset, Warm Reset, and Max Reset. Also for proper C6455 device operation, do not oppose the IPD on the AEA7 pin during Power-On Reset, Warm Reset, and Max Reset.
AEA7				
AEA6/PCI66				
AEA5/MCBSP1_EN				
AEA4/SYCLKOUT_EN				
AEA3				
AEA2/CFGGP2				
AEA1/CFGGP1				
AEA0/CFGGP0				

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
EMIFA (64-BIT) - DATA				
AED63				
AED62				
AED61				
AED60				
AED59				
AED58				
AED57				
AED56				
AED55				
AED54				
AED53				
AED52				
AED51				
AED50				
AED49				
AED48				
AED47				
AED46				
AED45				
AED44				
AED43				
AED42				
AED41				
AED40				
AED39				
AED38				
AED37				
AED36				
AED35				
AED34				
AED33				
AED32				
AED31				
AED30				
AED29				
AED28				
AED27				
AED26				
AED25				
AED24				
AED23				
AED22				

I/O/Z

IPU

EMIFA external data

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
AED21		I/O/Z	IPU	EMIFA external data
AED20				
AED19				
AED18				
AED17				
AED16				
AED15				
AED14				
AED13				
AED12				
AED11				
AED10				
AED9				
AED8				
AED7				
AED6				
AED5				
AED4				
AED3				
AED2				
AED1				
AED0				
DDR2 EMIF (32-BIT) - CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY				
DEV _{DDR0}		A		DDR2 supply (1.8-V I/O supply)
DEV _{DDR1}		A		DDR2 supply (1.8-V I/O supply)
$\overline{DCE0}$		O/Z		DDR2 EMIF memory space enables - Enabled by bits 28 through 31 of the word address - Only one pin is asserted during any external data access
DBA2		O/Z		DDR2 EMIF bank address control
DBA1		O/Z		
DBA0		O/Z		
DDR2CLKOUT		O/Z		DDR2 EMIF output clock (CPU/4 frequency)
$\overline{DDR2CLKOUT}$		O/Z		Negative DDR2 EMIF output clock (CPU/4 frequency)
$\overline{DSDCAS}$		O/Z		DDR2 EMIF SDRAM column-address strobe
$\overline{DSDRAS}$		O/Z		DDR2 EMIF SDRAM row-address strobe
$\overline{DSDWE}$		O/Z		DDR2 EMIF SDRAM write-enable
DSDCKE		O/Z		DDR2 EMIF SDRAM clock-enable (used for self-refresh mode). If SDRAM is not in system, SDCKE can be used as a general-purpose output.
DRSV		O/Z		Reserved
DRSV		O/Z		Reserved
DSDDQGATE3		I/O/Z		DDR2 EMIF data strobe gate [3:0]
DSDDQGATE2		I/O/Z		
DSDDQGATE1		I/O/Z		
DSDDQGATE0		I/O/Z		

Table 2-3. Terminal Functions TBD (continued)

SIGNAL		TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
NAME	NO.			
DSDDQM3		O/Z		DDR2 EMIF byte-enable controls - Decoded from the low-order address bits. The number of address bits or byte enables used depends on the width of external memory. - Byte-write enables for most types of memory. - Can be directly connected to SDRAM read and write mask signal (SDQM).
DSDDQM2		O/Z		
DSDDQM1		O/Z		
DSDDQM0		O/Z		
DSDDQS3		I/O/Z		DDR2 EMIF data strobe [3:0] positive
DSDDQS2		I/O/Z		
DSDDQS1		I/O/Z		
DSDDQS0		I/O/Z		
<u>DSDDQS3</u>		I/O/Z		DDR2 EMIF data strobe [3:0] negative
<u>DSDDQS2</u>		I/O/Z		
<u>DSDDQS1</u>		I/O/Z		
<u>DSDDQS0</u>		I/O/Z		
DDR2 EMIF (32-BIT) - ADDRESS				
DEA13	O/Z			DDR2 EMIF external address (word address)
DEA12				
DEA11				
DEA10				
DEA9				
DEA8				
DEA7				
DEA6				
DEA5				
DEA4				
DEA3				
DEA2				
DEA1				
DEA0				

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
DDR2 EMIF (32-BIT) - DATA				
DED31	I/O/Z			DDR2 EMIF external data
DED30				
DED29				
DED28				
DED27				
DED26				
DED25				
DED24				
DED23				
DED22				
DED21				
DED20				
DED19				
DED18				
DED17				
DED16				
DED15				
DED14				
DED13				
DED12				
DED11				
DED10				
DED9				
DED8				
DED7				
DED6				
DED5				
DED4				
DED3				
DED2				
DED1				
DED0				
Timer 1				
TOUT1L	O/Z	IPD	Timer 0 or general-purpose output 1 low	
TINP1L	I	IPD	Timer 0 or general-purpose input 1 low	
Timer 0				
TOUT0L	O/Z	IPD	Timer 0 or general-purpose output 0 low	
TINP0L	I	IPD	Timer 0 or general-purpose input 0 low	
Inter-integrated circuit (I2C)				
SCL	I/O/Z	—	I2C clock. When the I2C module is used, use an external pullup resistor.	
SDA	I/O/Z	—	I2C data. When I2C is used, ensure there is an external pullup resistor.	
MULTICHANNEL BUFFERED SERIAL PORT 1 AND MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP1 and McBSP0)				
CLKS	I/O/Z	IPD	McBSP external clock source (as opposed to internal) (I/O/Z) [shared by McBSP1 and McBSP0]	

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1)				
CLKR1/GP[0]		I/O/Z	IPD	McBSP1 receive clock (I/O/Z) or GP[1] (I/O/Z) [default]
FSR1/GP[10]		I/O/Z	IPD	McBSP1 receive frame sync (I/O/Z) or GP[10] (I/O/Z) [default]
DR1/GP[8]		I	IPD	McBSP1 receive data (I) or GP[8] (I/O/Z) [default]
DX1/GP[9]		O/Z	IPD	McBSP1 transmit data (O/Z) or GP[9] (I/O/Z) [default]
FSX1/GP[11]		I/O/Z	IPD	McBSP1 transmit frame sync (I/O/Z) or GP[11] (I/O/Z) [default]
CLKX1/GP[3]		I/O/Z	IPD	McBSP1 transmit clock (I/O/Z) or GP[3] (I/O/Z) [default]
MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0)				
CLKR0		I/O/Z	IPU	McBSP0 receive clock (I/O/Z)
FSR0		I/O/Z	IPD	McBSP0 receive frame sync (I/O/Z)
DR0		I	IPD	McBSP0 receive data (I)
DX0		O/Z	IPD	McBSP0 transmit data (O/Z)
FSX0		I/O/Z	IPD	McBSP0 transmit frame sync (I/O/Z)
CLKX0		I/O/Z	IPU	McBSP0 transmit clock (I/O/Z)
UNIVERSAL TEST AND OPERATIONS PHY INTERFACE for ASYNCHRONOUS TRANSFER MODE (ATM) [UTOPIA SLAVE]				
UTOPIA SLAVE (ATM CONTROLLER) - TRANSMIT INTERFACE				
UXCLK/MTCLK/ RMREFCLK		I/O/Z		Source clock for UTOPIA transmit driven by Master ATM Controller. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is either EMAC MII transmit clock (MTCLK) or the EMAC RMII reference clock. The EMAC function is controlled by the MACSEL[1:0] (AEA[10:9] pins). For more detailed information, see the Device Configuration section of this datasheet.
UXCLAV/GMTCLK		I/O/Z		Transmit cell available status output signal from UTOPIA Slave. 0 indicates a complete cell is NOT available for transmit 1 indicates a complete cell is available for transmit When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC GMII transmit clock. MACSEL[1:0] dependent.
UXENB/MTXEN/ RMTXEN/GMTXEN		I/O/Z		UTOPIA transmit interface enable input signal. Asserted by the Master ATM Controller to indicate that the UTOPIA Slave should put out on the Transmit Data Bus the first byte of valid data and the UXSOC signal in the next clock cycle. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is either the EMAC MII transmit enable [default] or EMAC RMII transmit enable or EMAC GMII transmit enable. MACSEL[1:0] dependent.
UXSOC/MCOL/ GMCOL		I/O/Z		Transmit Start-of-Cell signal. This signal is output by the UTOPIA Slave on the rising edge of the UXCLK, indicating that the first valid byte of the cell is available on the 8-bit Transmit Data Bus (UXDATA[7:0]). When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is either the EMAC MII collision sense or EMAC GMII collision sense. MACSEL[1:0] dependent.
UXADDR4/MDCLK/ RMDCLK/GMDCLK		I		UTOPIA transmit address pins (UXADDR[4:0]) (I) As UTOPIA transmit address pins, UTOPIA_EN (AEA12 pin) = 1: 5-bit Slave transmit address input pins driven by the Master ATM Controller to identify and select one of the Slave devices (up to 31 possible) in the ATM System. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0) and if the PCI_EN pin (TBD) = 1, these pins are PCI peripheral pins - PCI command/byte enable 3(PCBE3) [I/O/Z], PCI initialization device select (PIDSEL) [I], and PCI initiator ready (PIRDY) [I/O/Z]. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), these pins are MDIO MII or GMII serial data input/output (MDIO or GMDIO). MACSEL[1:0] dependent.
UXADDR3/MDIO/ GMDIO		I		
UXADDR2/PCBE3		I		
UXADDR1/PIDSEL		I		
UXADDR0/PIRDY		I		

Table 2-3. Terminal Functions TBD (continued)

SIGNAL		TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
NAME	NO.			
UXDATA7/GMTXD7		I/O/Z		UTOPIA 8-bit transmit data bus (I/O/Z) or EMAC MII 4-bit transmit data bus (I/O/Z) [default] or EMAC GMII 8-bit transmit data bus or EMAC RMII 2-bit transmit data bus (I/O/Z) Using the Transmit Data Bus, the UTOPIA Slave (on the rising edge of the UXCLK) transmits the 8-bit ATM cells to the Master ATM Controller. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), these pins function as EMAC pins and are controlled by the MACSEL[1:0] (AEA[10:9] pins) to select the MII, RMII, GMII, or RGMII EMAC interface. (For more details, see the Device Configurations section of this datasheet).
UXDATA6/GMTXD6				
UXDATA5/GMTXD5				
UXDATA4/GMTXD4				
UXDATA3/MTXD3/GMTXD3				
UXDATA2/MTXD2/GMTXD2				
UXDATA1/MTXD1/RMTXD1/GMTXD1				
UXDATA0/MTXD0/RMTXD0/GMTXD0				
UTOPIA SLAVE (ATM CONTROLLER) - RECEIVE INTERFACE				
URCLK/MRCLK/GMRCLK		I/O/Z		Source clock for UTOPIA receive driven by Master ATM Controller. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC MII [default] or GMII receive clock. MACSEL[1:0] dependent.
URCLAV/MCRS/RMCSDV/GMCRS		I/O/Z		Receive cell available status output signal from UTOPIA Slave. 0 indicates NO space is available to receive a cell from Master ATM Controller 1 indicates space is available to receive a cell from Master ATM Controller When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC MII carrier sense [default] or RMII carrier sense/data valid or GMII carrier sense. MACSEL[1:0] dependent. MACSEL[1:0] dependent.
URENB/MRXDV/GMRXDV		I/O/Z		UTOPIA receive interface enable input signal. Asserted by the Master ATM Controller to indicate to the UTOPIA Slave to sample the Receive Data Bus (URDATA[7:0]) and URSOC signal in the next clock cycle or thereafter. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC MII [default] or GMII receive data valid. MACSEL[1:0] dependent.
URSOC/MRXER/RMRXER/GMRXER		I/O/Z		Receive Start-of-Cell signal. This signal is output by the Master ATM Controller to indicate to the UTOPIA Slave that the first valid byte of the cell is available to sample on the 8-bit Receive Data Bus (URDATA[7:0]). When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC MII [default] or RMII or GMII receive error. MACSEL[1:0] dependent.
URADDR4/ $\overline{\text{PCBE0}}$ /GP[2]		I		UTOPIA receive address pins [URADDR[4:0] (I)]: As UTOPIA receive address pins, UTOPIA_EN (AEA12 pin) = 1: 5-bit Slave receive address input pins driven by the Master ATM Controller to identify and select one of the Slave devices (up to 31 possible) in the ATM System. - When the UTOPIA peripheral is disabled [UTOPIA_EN (AEA12 pin) = 0], these pins are PCI (if PCI_EN = 1) or GPIO (if PCI_EN = 0) pins (GP[15:12, 2]).
URADDR3/ $\overline{\text{PREQ}}$ /GP[15]		I		
URADDR2/ $\overline{\text{PINTA}}$ /GP[14]		I		
URADDR1/ $\overline{\text{PRST}}$ /GP[13]		I		
URADDR0/ $\overline{\text{PGNT}}$ /GP[12]		I		
				As PCI peripheral pins - PCI command/byte enable 0 ($\overline{\text{PCBE0}}$) [I/O/Z] PCI bus request ($\overline{\text{PREQ}}$) [O/Z], PCI interrupt A ($\overline{\text{PINTA}}$) [O/Z], PCI reset ($\overline{\text{PRST}}$) [I] and PCI bus grant ($\overline{\text{PGNT}}$) [I/O/Z].

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
URDATA7/GMRXD7		I/O/Z		UTOPIA 8-bit Receive Data Bus (I/O/Z) or EMAC receive data bus [MII] (I/O/Z) [default] or [GMII] (I/O/Z) or [RMII] (I/O/Z) Using the Receive Data Bus, the UTOPIA Slave (on the rising edge of the URCLK) can receive the 8-bit ATM cell data from the Master ATM Controller. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), these pins function as EMAC pins and are controlled by the MACSEL[1:0] (AEA[10:9] pins) to select the MII, RMII, GMII, or RGMII EMAC interface. (For more details, see the Device Configurations section of this data sheet).
URDATA6/GMRXD6				
URDATA5/GMRXD5				
URDATA4/GMRXD4				
URDATA3/MRXD3/ GMRXD3				
URDATA2/MRXD2/ GMRXD2				
URDATA1/MRXD1/ RMRXD1/GMRXD1				
URDATA0/MRXD0/ RMRXD0/GMRXD0				
RAPID I/O SERIAL PORT				
RIOCLK		I		Rapid I/O serial port source (reference) clock
$\overline{\text{RIOCLK}}$		I		Negative Rapid I/O serial port source (reference) clock
RIOTX3		O		Rapid IO transmit data bus bits [3:0] For proper C6455 device operation, the AEA3 pin must be externally pulled up with a 1-k Ω resistor at device reset.
RIOTX2				
RIOTX1				
RIOTX0				
$\overline{\text{RIOTX3}}$		O/Z		Rapid IO negative transmit data bus bits [3:0] (differential) For proper C6455 device operation, the AEA3 pin must be externally pulled up with a 1-k Ω resistor at device reset.
$\overline{\text{RIOTX2}}$				
$\overline{\text{RIOTX1}}$				
$\overline{\text{RIOTX0}}$				
RIORX3		I		Rapid IO receive data bus bits [3:0] For proper C6455 device operation, the AEA3 pin must be externally pulled up with a 1-k Ω resistor at device reset.
RIORX2				
RIORX1				
RIORX0				
$\overline{\text{RIORX3}}$		I		Rapid IO negative receive data bus bits [3:0] (differential) For proper C6455 device operation, the AEA3 pin must be externally pulled up with a 1-k Ω resistor at device reset.
$\overline{\text{RIORX2}}$				
$\overline{\text{RIORX1}}$				
$\overline{\text{RIORX0}}$				
MANAGEMENT DATA INPUT/OUTPUT (MDIO) FOR MII/RMII/GMII				
MDCLK		I/O/Z	IPD	MDIO serial clock input/output
MDIO		I/O/Z	IPU	MDIO serial data input/output
MANAGEMENT DATA INPUT/OUTPUT (MDIO) FOR RGMII				
RGMDCLK		O/Z		MDIO serial clock input/output (RGMII mode)
RGMDIO		I/O/Z		MDIO serial data input/output (RGMII mode)
ETHERNET MAC (EMAC) [MII/RMII/GMII]				
If the Ethernet MAC (EMAC) and MDIO peripherals are enabled (AEA12 pin driven low [UTOPIA_EN = 0]), there are two additional configuration pins — the MAC_SEL[1:0] (AEA[10:9] pins) — that select one of the four interface modes (MII, RMII, GMII, or RGMII) for the EMAC/MDIO interface. For more detailed information on the EMAC select pins, see the <i>Device Configuration</i> section of this document.				
URCLK/MRCLK/ GMCLK		I/O/Z		UTOPIA receive clock (URCLK) driven by Master ATM Controller(TBD) or when the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC MII [default] or GMII receive clock. MACSEL[1:0] dependent.
URCLAV/MCRS/ RMCSDV/GMCRS		I/O/Z		UTOPIA receive cell available status output signal from UTOPIA Slave(TBD) or when the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC MII carrier sense [default] or RMII carrier sense/data valid or GMII carrier sense. MACSEL[1:0] dependent.

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
URSOC/MRXER/ RMRXER/GMRXER		I/O/Z		UTOPIA receive Start-of-Cell signal (TBD) or when the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC MII [default] or RMII or GMII receive error. MACSEL[1:0] dependent.
URENB/MRXDV/ GMRXDV		I/O/Z		UTOPIA receive interface enable input signal. Asserted by the Master ATM Controller to indicate to the UTOPIA Slave to sample the Receive Data Bus (URDATA[7:0]) and URSOC signal in the next clock cycle or thereafter. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC MII [default] or GMII receive data valid. MACSEL[1:0] dependent.
URDATA7/GMRXD7		I/O/Z		UTOPIA 8-bit Receive Data Bus (I/O/Z) [default] or EMAC receive data bus [MII] (I/O/Z) [default] or [GMII] (I/O/Z) or [RMII] (I/O/Z) Using the Receive Data Bus, the UTOPIA Slave (on the rising edge of the URCLK) can receive the 8-bit ATM cell data from the Master ATM Controller. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), these pins function as EMAC pins and are controlled by the MACSEL[1:0] (AEA[10:9] pins) to select the MII, RMII, GMII or RGMII EMAC interface. (For more details, see the Device Configurations section of this datasheet).
URDATA6/GMRXD6		I/O/Z		
URDATA5/GMRXD5		I/O/Z		
URDATA4/GMRXD4		I/O/Z		
URDATA3/MRXD3/ GMRXD3		I/O/Z		
URDATA2/MRXD2/ GMRXD2		I/O/Z		
URDATA1/MRXD1/ RMTXD1/GMRXD1		I/O/Z		
URDATA0/MRXD0/ RMTXD0/GMRXD0		I/O/Z		
UXCLAV/GMTCLK		I/O/Z		Transmit cell available status output signal from UTOPIA Slave. 0 indicates a complete cell is NOT available for transmit 1 indicates a complete cell is available for transmit When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is EMAC GMII transmit clock. MACSEL[1:0] dependent.
UXCLK/MTCLK/ RMREFCLK		I/O/Z		UTOPIA transmit source clock (UXCLK) driven by Master ATM Controller (TBD) or when the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is either EMAC MII transmit clock (MTCLK) [default] or the EMAC RMII reference clock. The EMAC function is controlled by the MACSEL[1:0] (AEA[10:9] pins). For more detailed information, see the Device Configuration section of this datasheet.
UXSOC/MCOL/ GMCOL		O/Z		UTOPIA transmit Start-of-Cell signal. This signal is output by the UTOPIA Slave on the rising edge of the UXCLK, indicating that the first valid byte of the cell is available on the 8-bit Transmit Data Bus (UXDATA[7:0]). When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is either the EMAC MII collision sense [default] or EMAC GMII collision sense. MACSEL[1:0] dependent.
UXENB/MTXEN/ RMTXEN/GMTXEN		I/O/Z		UTOPIA transmit interface enable input signal (TBD) or when the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), this pin is either the EMAC MII transmit enable [default] or EMAC RMII transmit enable or EMAC GMII transmit enable. MACSEL[1:0] dependent.
UXDATA7/GMTXD7		I/O/Z		UTOPIA 8-bit transmit data bus (I/O/Z) or EMAC MII 4-bit transmit data bus (I/O/Z) [default] or EMAC GMII 8-bit transmit data bus or EMAC RMII 2-bit transmit data bus (I/O/Z) Using the Transmit Data Bus, the UTOPIA Slave (on the rising edge of the UXCLK) transmits the 8-bit ATM cells to the Master ATM Controller. When the UTOPIA peripheral is disabled (UTOPIA_EN [AEA12 pin] = 0), these pins function as EMAC pins and are controlled by the MACSEL[1:0] (AEA[10:9] pins) to select the MII, RMII, GMII or RGMII EMAC interface. (For more details, see the Device Configurations section of this datasheet).
UXDATA6/GMTXD6		I/O/Z		
UXDATA5/GMTXD5		I/O/Z		
UXDATA4/GMTXD4		I/O/Z		
UXDATA3/MTXD3/ GMTXD3		I/O/Z		
UXDATA2/MTXD2/ GMTXD2		I/O/Z		
UXDATA1/MTXD1/ RMTXD1		I/O/Z		
UXDATA0/MTXD0/ RMTXD0		I/O/Z		

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
ETHERNET MAC (EMAC) [RGMI]				
If the Ethernet MAC (EMAC) and MDIO peripherals are enabled (AEA12 pin driven low [UTOPIA_EN = 0]), there are two additional configuration pins — the MAC_SEL[1:0] (AEA[10:9] pins) — that select one of the four interface modes (MII, RMII, GMII, or RGMII) for the EMAC/MDIO interface. For more detailed information on the EMAC select pins, see the <i>Device Configuration</i> section of this document.				
RGMREFCLK		O/Z		RGMII reference clock. MACSEL[1:0] =11
RGREFV		A		RGMII reference voltage TBD-V TBD
RGMTCLK		O/Z		RGMII transmit clock. MACSEL[1:0] =11
RGMTD3		O/Z		RGMII transmit data [3:0]. MACSEL[1:0] =11
RGMTD2				
RGMTD1				
RGMTD0				
RGMTXEN		O/Z		RGMII transmit enable. MACSEL[1:0] =11
RGMRCLK		I		RGMII receive clock. MACSEL[1:0] =11
RGMRXD3		I		RGMII receive data [3:0] TBD. MACSEL[1:0] =11
RGMRXD2		I		
RGMRXD1		I		
RGMRXD0		I		
RGMRXCTL		I		RGMII receive control [for error detection and data valid]. MACSEL[1:0] =11
RESERVED FOR TEST				
RSV01				Reserved. These pins must be connected directly to Core Supply (CV _{DD}) for proper device operation
RSV02				
RSV03				
RSV04				
RSV05				
RSV06				Reserved. This pin must be connected directly to 3.3-V I/O Supply (DV _{DD33}) for proper device operation.
RSV07		I		Reserved. This pin must be connected directly to 1.5-V I/O Supply (DV _{DD15}) for proper device operation.
RSV08		I		
RSV09		I		Reserved. This pin must be connected directly to 1.8-V I/O Supply (DV _{DD18}) for proper device operation.
RSV10				
RSV11				Reserved. This pin must be connected via a 200-Ω resistor directly to ground (V _{SS}) for proper device operation.
RSV12				Reserved. This pin must be connected via a 200-Ω resistor directly to 1.8-V I/O Supply (DV _{DD18}) for proper device operation.
RSV13				Reserved. This pin must be connected via a 200-Ω resistor directly to ground (V _{SS}) for proper device operation.
RSV14				Reserved. This pin must be connected via a 200-Ω resistor directly to 1.5/1.8-V I/O Supply (DV _{DD15}) for proper device operation.
RSV15				Reserved. This pin must be connected via a 40-Ω resistor directly to ground (V _{SS}) for proper device operation.
RSV16				Reserved. This pin must be connected via a 40-Ω resistor directly to 3.3-V I/O Supply (DV _{DD33}) for proper device operation.

Table 2-3. Terminal Functions TBD (continued)

SIGNAL		TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
NAME	NO.			
RSV17		A		Reserved (leave unconnected, do not connect to power or ground)
RSV18		A		
RSV19		A		
RSV20		A		
RSV21		A		
RSV22		O		
RSV23		O		
RSV24		O		
RSV25		O		
RSV26		A		
RSV27		A		
RSV36		I/O/Z	IPU	
RSV37		I/O/Z	IPU	
RSV38		I/O/Z	IPU	
RSV39		I/O/Z	IPU	
RSV40		I/O/Z	IPU	
RSV41		O/Z	IPU	
RSV42		O/Z	IPU	
RSV43		O/Z	IPU	
RSV44		O/Z	IPU	
RSV28		A		Reserved. This pin must be connected directly to V _{SS} for proper device operation.
RSV29		A		
RSV30		A		
RSV31		A		
RSV32		I	IPD	
RSV33		I	IPD	
RSV34		I	IPD	Reserved. This pin must be connected directly to V _{SS} for proper device operation.
RSV35		I	IPD	
SUPPLY VOLTAGE PINS				
NOTE: The number of blank rows in each respective supply voltage and ground (GND) sections to follow indicates the actual number of supply voltage pins or GND pins required on the C6455 device.				
V _{REFSSTL}		A		1.8-V reference for SSTL buffer [DDR2 EMIF peripheral]. NOTE: If the DDR2 peripheral is not used, connect this pin to V _{SS} .
V _{REFHSTL}		A		1.8-V reference for HSTL buffer [DDR2 EMIF peripheral]. NOTE: If the DDR2 peripheral is not used, connect this pin to V _{SS} . TBD
DV _{DDR}		S		1.8-V I/O supply voltage (RapidIO I/O Voltage for Rapid I/O regulator supply). NOTE: If Rapid I/O is not used, these pins must be connected directly to V _{SS} for proper device operation.
ADV _{DD12}		A		V _{DDA} 1.2-V I/O supply voltage (RapidIO I/O Voltage for Rapid I/O analog supply) Do not use the core supply.
				NOTE: If Rapid I/O is not used, these pins must be connected directly to V _{SS} for proper device operation.

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
DV _{DD12}		S		1.2-V I/O supply voltage (RapidIO I/O Voltage for Rapid I/O termination supply), (RapidIO I/O Voltage for Rapid I/O digital supply) (RapidIO I/O MAC/PHY supply) Do not use the core supply. NOTE: If Rapid I/O is not used, these pins must be connected directly to V _{SS} for proper device operation.
DV _{DD15}		S		1.5-V or 1.8-V I/O supply voltage (EMAC RGMII I/O Voltage)
DV _{DD18}		S		1.8-V I/O supply voltage (DDR2 EMIF I/O Voltage)
DV _{DD33}		S		3.3-V I/O supply voltage
DV _{DD33}		S		3.3-V I/O supply voltage
DV _{DD33}		S		3.3-V I/O supply voltage
CV _{DD}		S		1.2-V core supply voltage

Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME		NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
CV _{DD}		S		1.2-V core supply voltage	
GROUND PINS					
V _{SS}		GND		Ground pins	
V _{SS}		GND		Ground pins	
V _{SS}		GND		Ground pins	
V _{SS}		GND		Ground pins	

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Table 2-3. Terminal Functions TBD (continued)

SIGNAL NAME	NO.	TYPE ⁽¹⁾	IPD/IPU ⁽²⁾	DESCRIPTION
V _{SS}		GND		Ground pins
V _{SS}		GND		Ground pins

2.1.1 Development

2.1.1.1 Development Support

In case the customer would like to develop their own features and software on the C6455 device, TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of C6000™ DSP-based applications:

Software Development Tools: Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools: Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug) EVM (Evaluation Module)

2.1.1.2 Device Support

2.1.1.2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMX320C6455ZTZ1**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX	Experimental device that is not necessarily representative of the final device's electrical specifications
TMP	Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
TMS	Fully qualified production device

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing.
TMDS	Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped with against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

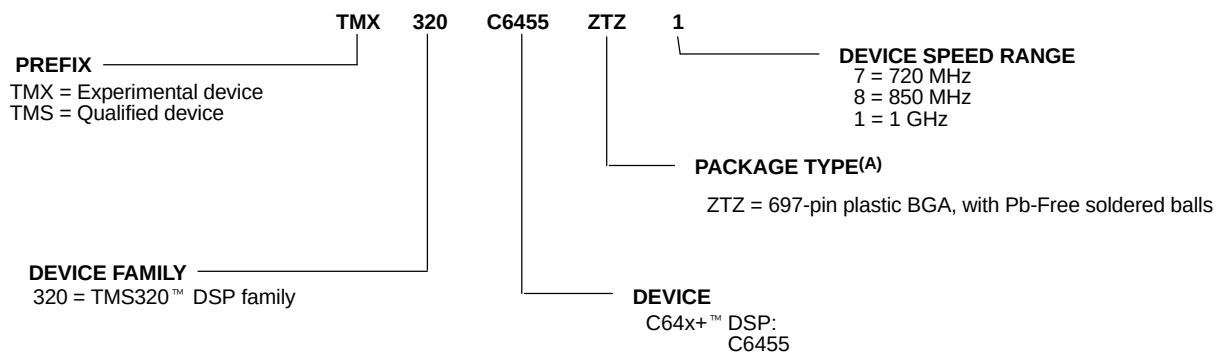
Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZTZ), the temperature range (for example, blank is the default commercial temperature range), and the device speed range in megahertz (for example, 1 is 1 GHz). [Figure 2-9](#) provides a legend for reading the complete device name for any TMS320C64x+™ DSP generation member.

For device part numbers and further ordering information for TMS320C6455 in the ZTZ package type, see the TI website (<http://www.ti.com>) or contact your TI sales representative.

TMS320C6455 Fixed-Point Digital Signal Processor

SPRS276–MAY 2005



A. BGA = Ball Grid Array

Figure 2-9. TMS320C64x+™ DSP Device Nomenclature (including the TMS320C6455 DSP)

2.1.1.2.2 Documentation Support - TBD

2.1.2 Device Silicon Revision

The data manual supports the initial release of the C6455 device; therefore, no device-specific silicon errata document is currently available.

3 Device Configurations

On the C6455 device, bootmode and certain device configurations/peripheral selections are determined at device reset, while peripheral usage (on/off) is determined by the Power Saver registers after device reset. **By default, the peripherals on the C6455 device are "off" and need to be "turned on".** For more details, see the Power Saver section of this document.

RESERVED (AEA[3] pin), for proper device operation this pin *must* be **externally PULLED UP**

RESERVED (AEA[11] pin), for proper device operation this pin *must* be **externally PULLED UP**

The C6455 has **no** hardware CLKMODE selection, the PLL1 multiply factor is set in software during boot.

3.1 Device Configuration at Device Reset

[Table 3-1](#) describes the C6455 device configuration pins. The logic level of the AEA[19:0] pins is latched at reset to determine the device configuration. The logic level on the device configuration pins can be set by using external pullup/pulldown resistors or by using some control device (e.g., FPGA/CPLD) to intelligently drive these pins. When using a control device, care should be taken to ensure there is no contention on the lines when the device is out of reset. The device configuration pins are sampled during reset and are driven after the reset is removed. At this time, the control device should ensure it has stopped driving the device configuration pins of the DSP to again avoid contention.

Table 3-1. C6455 Device Configuration Pins (AEA[19:0] and ABA[1:0])

CONFIGURATION PIN	NO.	IPD/ IPU ⁽¹⁾	FUNCTIONAL DESCRIPTION
AEA[19:16]	[TBD, TBD, TBD, TBD]	IPD	Bootmode Selections (Bootmode [3:0]): 0000 - No boot (default mode) 0001 - HPI/PCI boot (based on PCI_EN [pin]) 0010 - Reserved 0011 - Reserved 0100 - EMIFA 8-bit ROM boot 0101 - Reserved 0110 - Reserved 0111 - Reserved 1000 - Reserved 1001 - Reserved 1010 - Reserved Others - Reserved [1011 thru 1111]
AEA15	TBD	IPD	EMIFA input clock source select Clock mode select for EMIFA (AECLKIN_SEL) 0 - AECLKIN (default mode) 1 - SYSCLK3 (CPU/x) Clock Rate. The SYSCLK3 clock rate is software selectable via the Software PLL1 Controller. By default, SYSCLK3 is selected as CPU/8 clock rate.
AEA14	TBD	IPD	HPI peripheral bus width (HPI_WIDTH) select [Applies only when HPI is enabled; PCI_EN pin = 0] 0 - HPI operates as an HPI16 (default). (HPI bus is 16 bits wide. HD[15:0] pins are used and the remaining HD[31:16] pins are reserved pins in the Hi-Z state.) 1 - HPI operates as an HPI32.

(1) IPD = Internal pulldown, IPU = Internal pullup. (These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor. To pull up a signal to the opposite supply rail, a 1-kΩ resistor should be used.)

Table 3-1. C6455 Device Configuration Pins (AEA[19:0] and ABA[1:0]) (continued)

CONFIGURATION PIN	NO.	IPD/ IPU ⁽¹⁾	FUNCTIONAL DESCRIPTION
AEA13	TBD	IPU	Device Endian mode (LENDIAN) 0 - System operates in Big Endian mode 1 - System operates in Little Endian mode (default)
AEA12	TBD	IPD	UTOPIA enable bit (UTOPIA_EN) 0 - UTOPIA disabled; Ethernet MAC (EMAC) and MDIO enabled (default) This means all multiplexed EMAC/UTOPIA and MDIO/UTOPIA pins function as EMAC and MDIO. Which EMAC/MDIO configuration (interface) [MII, RMII, GMII or the standalone RGMII] is controlled by the MACSEL[1:0] bits (AEA[10:9] pins). 1 - UTOPIA enabled; EMAC and MDIO disabled [except when the MACSEL[1:0] bits = 11 then, the EMAC/MDIO RGMII interface is <i>still</i> functional] This means all multiplexed EMAC/UTOPIA and MDIO/UTOPIA pins now function as UTOPIA. And if MACSEL[1:0] = 11, the RGMII standalone pin functions can be used.
AEA11	TBD	IPD	Reserved. For proper C6455 device operation, this pin must be externally pulled up with a 1-kΩ resistor at device reset.
AEA[10:9]	[TBD, TBD]	IPD	If the EMAC/MDIO peripherals are enabled, [AEA12 pin driven low (UTOPIA_EN = 0)], there are two additional configuration pins — the MACSEL[1:0] (AEA[10:9] pins) — that select one of the four interface modes (MII, RMII, GMII, or RGMII) for the EMAC. EMAC Interface Selects (MACSEL[1:0]) [EMAC/DMIO enabled; UTOPIA disabled (UTOPIA_EN (AEA12 pin) = 0)] 00 - 10/100 EMAC/MDIO with MII Interface [default] 01 - 10/100 EMAC/MDIO with RMII Interface 10 - 10/100/1000 EMAC/MDIO with GMII Interface 11 - 10/100/1000 EMAC/MDIO with RGMII Interface [RGMII interface requires a 1.5 V I/O supply] If the UTOPIA peripheral is enabled, [UTOPIA_EN (AEA12 pin) = 1] the UTOPIA interface is dependent on the PCI_EN pin [TBD] and the EMAC/MDIO interface is dependent on MAC_SEL[1:0] (AEA10:9): 0 !11 - UTOPIA Slave with Full Functionality 0 11 - UTOPIA Slave with Full Functionality plus 10/100/1000 EMAC/MDIO with RGMII Interface 1 !11 - UTOPIA Slave with Single PHY Mode only Plus PCI 1 11 - UTOPIA Slave with Single PHY Mode only Plus 10/100/1000 EMAC/MDIO with RGMII Interface Plus PCI For more detailed information on the UTOPIA_EN, PCI_EN, and the MAC_SEL[1:0] control pin selections, see Table 3-3
AEA8	TBD	IPD	PCI EEPROM Auto-Initialization (PCI_EEA) PCI auto-initialization via external EEPROM 0 - PCI auto-initialization through external EEPROM is disabled; the PCI peripheral uses the specified PCI default values (default). 1 - PCI auto-initialization through external EEPROM is enabled; the PCI peripheral is configured through external I2C EEPROM provided the PCI peripheral is enabled (PCI_EN = 1). Note: If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must not be pulled up.
AEA7	TBD	IPD	For proper C6455 device operation, do not oppose the IPD on this pin.
AEA6	TBD	IPD	PCI Frequency Selection (PCI66) [PCI peripheral <i>needs</i> be enabled (PCI_EN pin = 1) to use this function] Selects the PCI operating frequency of 66 MHz or 33 MHz PCI operating frequency is selected at reset via the pullup/pulldown resistor on the PCI66 pin: 0 - PCI operates at 33 MHz (default). 1 - PCI operates at 66 MHz. Note: If the PCI peripheral is disabled (PCI_EN pin = 0), this pin must not be pulled up.
AEA5	TBD	IPD	McBSP1 Enable bit (MCBSP1_EN) Selects which function is enabled on the McBSP1/GPIO muxed pins 0 - GPIO pin functions enabled (default). 1 - McBSP1 pin functions enabled.
AEA4	TBD	IPD	SYSCLKOUT Enable bit (SYSCLKOUT_EN) Selects which function is enabled on the SYSCLK3/GP[1] muxed pin 0 - GP[1] pin function of the SYSCLK3/GP[1] pin enabled (default). 1 - SYSCLK3 pin function of the SYSCLK3/GP[1] pin enabled.
AEA3	TBD	IPD	Reserved. For proper C6455 device operation, this pin must be externally pulled up with a 1-kΩ resistor at device reset.

Table 3-1. C6455 Device Configuration Pins (AEA[19:0] and ABA[1:0]) (continued)

CONFIGURATION PIN	NO.	IPD/ IPU ⁽¹⁾	FUNCTIONAL DESCRIPTION
AEA[2:0]	[TBD, TBD, TBD]	IPD	Configuration GPI (General-Purpose Inputs for Configuration purposes (CFGGP[2:0]) These pins are used in S/W routines located in internal ROM for boot operations.
PCI_EN	TBD	IPD	PCI Enable bit (PCI_EN) Controls whether the HPI peripheral or PCI peripheral is enabled/disabled. 0 - HPI peripheral pins are enabled; PCI peripheral pins are disabled (default) 1 - PCI peripheral pins are enabled; HPI peripheral pins are disabled
ABA0	TBD	IPD	DDR2 EMIF enable (DDR2_EN) 0 - DDR2 EMIF peripheral pins are disabled (default) 1 - DDR2 EMIF peripheral pins are enabled
ABA1	TBD	IPD	EMIFA enable (EMIFA_EN) 0 - EMIFA peripheral pins are disabled (default) 1 - EMIFA peripheral pins are enabled

3.2 Peripheral Configuration at Device Reset

Some C6455 peripherals share the same pins (internally muxed) and are mutually exclusive.

On the C6455 device, the PCI peripheral is muxed with the HPI peripheral and partially muxed with UTOPIA.

Table 3-2. PCI_EN, PCI66, PCI_EEAI, and HPI_WIDTH Peripheral Selection (HPI16/32, PCI, and PCI EEPROM)

PERIPHERAL SELECTION ⁽¹⁾				PERIPHERALS SELECTED			
PCI_EN pin [TBD]	PCI66 AEA6 Pin [TBD]	PCI_EEAI AEA8 Pin [TBD] ⁽¹⁾	HPI_WIDTH AEA14 Pin [TBD]	HPI Data Lower	HPI Data Upper	32-Bit PCI (66-/33-MHz)	PCI Auto-Init
0	0	0	0	Enabled	Hi-Z	Disabled	N/A
0	0	0	1	Enabled	Enabled	Disabled	N/A
1	1	1	X	Disabled		Enabled (66 MHz)	Enabled (via External EEPROM)
1	1	0	X	Disabled			Disabled
1	0	0	X	Disabled		Enabled (33 MHz)	Disabled (default values)
1	0	1	X	Disabled			Enabled (via External EEPROM)

(1) PCI_EEAI is latched at reset as a configuration input. If PCI_EEAI is set as one, then default values are loaded from an external I2C EEPROM.

The UTOPIA_EN function (AEA12 pin) controls whether or not the peripheral module is used and the MAC_SEL[1:0] functions (AEA[10:9]) control which interface and features are used.

Table 3-3. UTOPIA_EN, and MAC_SEL[1:0] Peripheral Selection (UTOPIA and EMAC)

PERIPHERAL SELECTION			HOST FUNCTION SELECTED
UTOPIA_EN AEA12 Pin [TBD]	PCI_EN Pin [TBD]	MAC_SEL[1:0] AEA[10:9] Pins [TBD, TBD]	
0	x	00b	10/100 EMAC/MDIO with MII Interface [default]
0	x	01b	10/100 EMAC/MDIO with RMII Interface
0	x	10b	10/100/1000 EMAC/MDIO with GMII Interface
0	x	11b	10/100/1000 EMAC/MDIO with RGMII Interface ⁽¹⁾
1	0	!11b	UTOPIA Slave with Full Functionality
1	0	11b	UTOPIA Slave with Full Functionality plus 10/100/1000 EMAC/MDIO with RGMII Interface ⁽¹⁾
1	1	!11b	UTOPIA Slave with Single PHY Mode Only Plus PCI
1	1	11b	UTOPIA Slave with Single PHY Mode only Plus 10/100/1000 EMAC/MDIO with RGMII Interface Plus PCI ⁽¹⁾

(1) RGMII interface requires a 1.5-V I/O supply.

3.3 Peripheral Selection After Device Reset

The C6455 device has a powersaver module that manages the power down of specific peripheral modules. For more detailed information on the powersaver module and its associated registers, see the Powersaver section of this document.

3.4 Device Status Register Description

The device status register depicts the status of the device peripheral selection. Once set, these bits will remain set until a device reset; therefore, these bits should be masked when reading the DEVSTAT register since their values can change. For the actual register bit names and their associated bit field descriptions, see [Figure 3-1](#) and [Table 3-4](#).

31	30	29					24
Reserved		Reserved					
R/W-0		R-00 0000					
23	22	21	20	19	18	17	16
Reserved	EMIFA_EN	DDR2_EN	PCI_EN	CFGGP2	CFGGP1	CFGGP0	Reserved
R-0	R-x	R-x	R-x	R-x	R-x	R-x	R-1
15	14	13	12	11	10	9	8
SYSCLKOUT_EN	MCBSP1_EN	PCI66	RESERVED	PCI_EEAI	MAC_SEL1	MAC_SEL0	Reserved
R-x	R-x	R-x	R-0	R-x	R-x	R-x	R-1
7	6	5	4	3	2	1	0
UTOPIA_EN	LENDIAN	HPI_WIDTH	AECLKINSEL	BOOTMODE3	BOOTMODE2	BOOTMODE1	BOOTMODE0
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x

LEGEND: R/W = Read/Write; R = Read only; -x = value after reset

Figure 3-1. Device Status Register (DEVSTAT) - 0x02A8 0000

Table 3-4. Device Status Register (DEVSTAT) Field Descriptions

Bit	Field	Value	Description
31:30	Reserved		Reserved. For proper device operation, write only zeroes to these bits.
29:23	Reserved		Reserved. Read-only, writes have no effect.
22	EMIFA_EN	0 1	EMIFA Enable (EMIFA_EN) status bit Shows the status of whether the EMIFA peripheral is enabled/disabled. EMIFA peripheral pins are disabled (default) EMIFA peripheral pins are enabled
21	DDR2_EN	0 1	DDR2 EMIF Enable (DDR2_EN) status bit Shows the status of whether the DDR2 EMIF peripheral is enabled/disabled. DDR2 EMIF peripheral pins are disabled (default) DDR2 EMIF peripheral pins are enabled
20	PCI_EN	0 1	PCI Enable (PCI_EN) status bit Shows the status of whether the HPI peripheral or PCI peripheral is enabled/disabled. HPI peripheral pins are enabled; PCI peripheral pins are disabled (default) PCI peripheral pins are enabled; HPI peripheral pins are disabled
19:17	CFGGP[2:0]		Used as General-Purpose inputs for configuration purposes. These pins are latched at reset. These values can be used by S/W routines for boot operations.
16	Reserved		Reserved. Read-only, writes have no effect.
15	SYCLKOUT_EN	0 1	SYCLKOUT Enable (SYCLKOUT_EN) status bit Shows the status of which function is enabled on the SYCLK4/GP[1] muxed pin. GP[1] pin function of the SYCLK4/GP[1] pin enabled (default). SYCLK4 pin function of the SYCLK4/GP[1] pin enabled.
14	MCBSP1_EN	0 1	McBSP1 Enable (MCBSP1_EN) status bit Shows the status of which function is enabled on the McBSP1/GPIO muxed pins. GPIO pin functions enabled (default). McBSP1 pin functions enabled.
13	PCI66	0 1	PCI Frequency Selection (PCI66) status bit Shows the status of the PCI operating frequency of either 66 MHz or 33 MHz. PCI operates at 33 MHz (default). PCI operates at 66 MHz.
12	Reserved		Reserved. Read-only, writes have no effect.
11	PCI_EEAI	0 1	PCI EEPROM Auto-Initialization (PCI_EEAI) status bit Shows whether the PCI auto-initialization via external EEPROM is enabled/disabled. PCI auto-initialization through external EEPROM is disabled; the PCI peripheral uses the specified PCI default values (default). PCI auto-initialization through external EEPROM is enabled; the PCI peripheral is configured through external I2C EEPROM provided the PCI peripheral pin is enabled (PCI_EN = 1).
10:9	MACSEL[1:0]	00 01 10 11	EMAC Interface Select (MACSEL[1:0]) status bits Shows which EMAC interface mode has been selected. 10/100 EMAC/MDIO with MII Interface (default) 10/100 EMAC/MDIO with RMII Interface 10/100/1000 EMAC/MDIO with GMII Interface 10/100/1000 EMAC/MDIO with RGMII Mode Interface [RGMII interface requires a 1.5 V I/O supply]
8	Reserved		Reserved. Read-only, writes have no effect.
7	UTOPIA_EN	0 1	UTOPIA enable (UTOPIA_EN) status bit Shows the status of whether the UTOPIA peripheral or the EMAC/MDIO peripherals are enabled. UTOPIA disabled; Ethernet MAC (EMAC) and MDIO enabled (default) UTOPIA enabled; EMAC and MDIO disabled

Table 3-4. Device Status Register (DEVSTAT) Field Descriptions (continued)

Bit	Field	Value	Description
6	LENDIAN	0 1	Device Endian mode (LENDIAN) Shows the status of whether the system is operating in Big Endian mode or Little Endian mode (default). System is operating in Big Endian mode. System is operating in Little Endian mode (default)
5	HPI_WIDTH	0 1	HPI bus width control bit. Shows the status of whether the HPI bus operates in 32-bit mode or in 16-bit mode (default). HPI operates in 16-bit mode. (default). HPI operates in 32-bit mode.
4	AECLKINSEL	0 1	EMIFA input clock select Shows the status of what clock mode is enabled or disabled for EMIFA. AECLKIN (default mode) SYSCLK3 (CPU/x) Clock Rate. The SYSCLK3 clock rate is software selectable via the Software PLL1 Controller. By default, SYSCLK3 is selected as CPU/8 clock rate.
3	BOOTMODE[3:0]	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 Others	Bootmode configuration bits Shows the status of what device bootmode configuration is operational. Bootmode [3:0] No boot (default mode) HPI/PCI boot Reserved Reserved EMIFA 8-bit ROM boot Reserved Reserved Reserved Reserved Reserved Reserved Reserved [1011 thru 1111]

3.5 JTAG ID Register Description

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. For the C6455 device, the JTAG ID register resides at address location 0x02A8 0008. The register hex value for the C6455 device is: 0x0008 A02F. For the actual register bit names and their associated bit field descriptions, see [Figure 3-2](#) and [Table 3-5](#).

31	28 27	12 11	1 0
VARIANT (4-bit)	PART NUMBER (16-bit)	MANUFACTURER (11-bit)	LSB
R-0000	R-0000 0000 1000 1010	R-0000 0010 111	R-1

LEGEND: R = Read only; -n = value after reset

Figure 3-2. JTAG ID Register - C6455 Register Value - 0x0008 A02F

Table 3-5. JTAG ID Register Field Descriptions

Bit	Field	Value	Description
31:28	VARIANT		Variant (4-Bit) value. C6455 value: 0000.
27:12	PART NUMBER		Part Number (16-Bit) value. C6455 value: 0000 0000 1000 1010.
11:1	MANUFACTURER		Manufacturer (11-Bit) value. C6455 value: 0000 0010 111.
0	LSB		LSB. This bit is read as a "1" for C6455.

3.6 Multiplexed Pins

Multiplexed pins are pins that are shared by more than one peripheral and are internally multiplexed. Some of these pins are configured by software, and the others are configured by external pullup/pulldown resistors only at reset. Those muxed pins that are configured by software should **not** be programmed to switch functionalities during run-time. Those muxed pins that are configured by external pullup/pulldown resistors are mutually exclusive; only one peripheral has primary control of the function of these pins after reset. [Table 3-6](#) identifies the multiplexed pins on the C6455 device; shows the default (primary) function and the default settings after reset; and describes the pins, registers, etc. necessary to configure specific multiplexed functions.

Table 3-6. C6455 Device Multiplexed Pins TBD

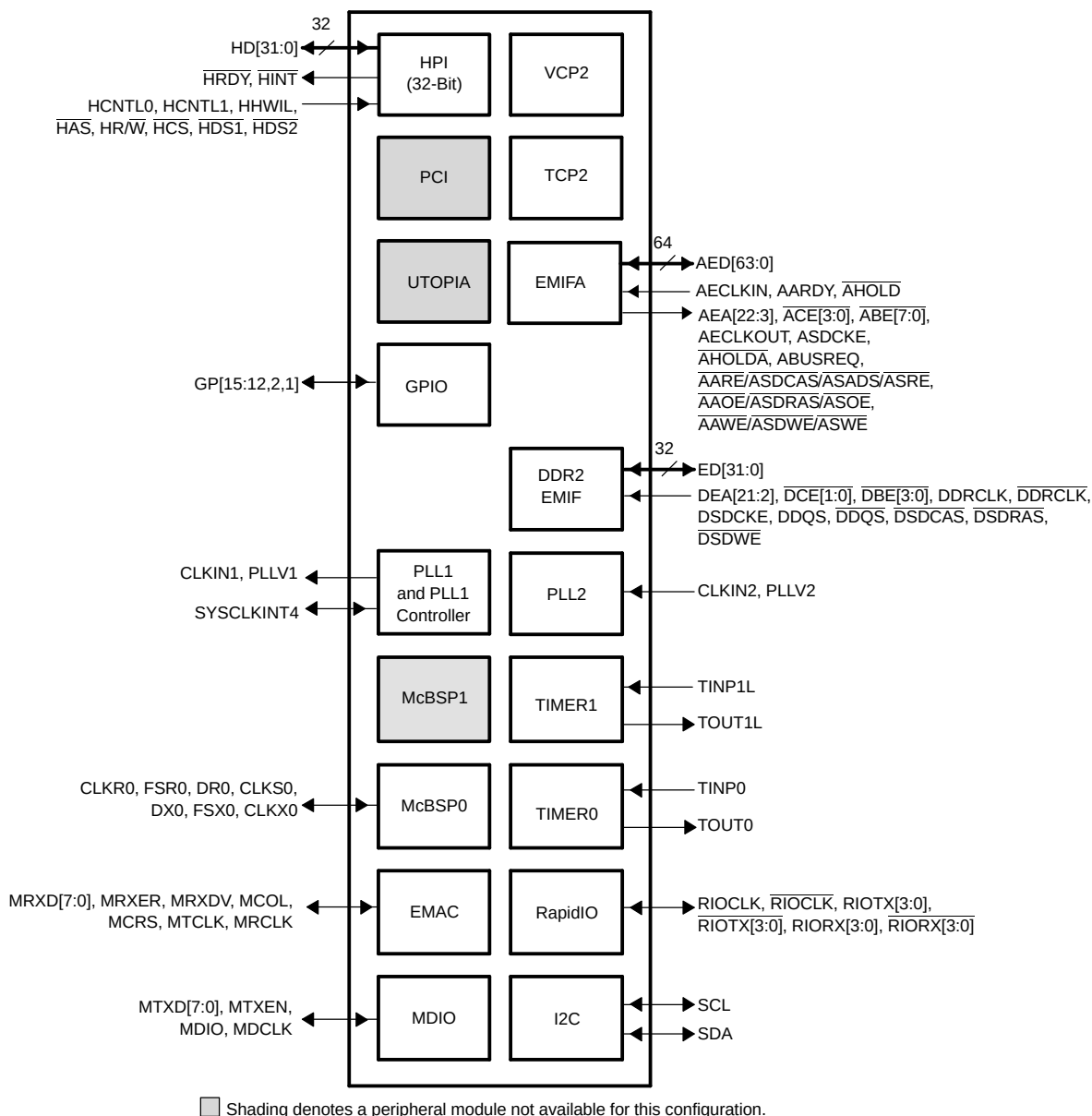
3.7 Debugging Considerations - TBD

It is recommended that external connections be provided to device configuration pins, including AEA[19:0]. Although internal pullup/pulldown resistors exist on these pins, providing external connectivity adds convenience to the user in debugging and flexibility in switching operating modes.

For the internal pullup/pulldown resistors for all device pins, see the terminal functions table.

3.8 Configuration Examples - TBD

Figure 3-3 and Figure 3-4 illustrate examples of peripheral selections/options that are configurable on the C6455 device.



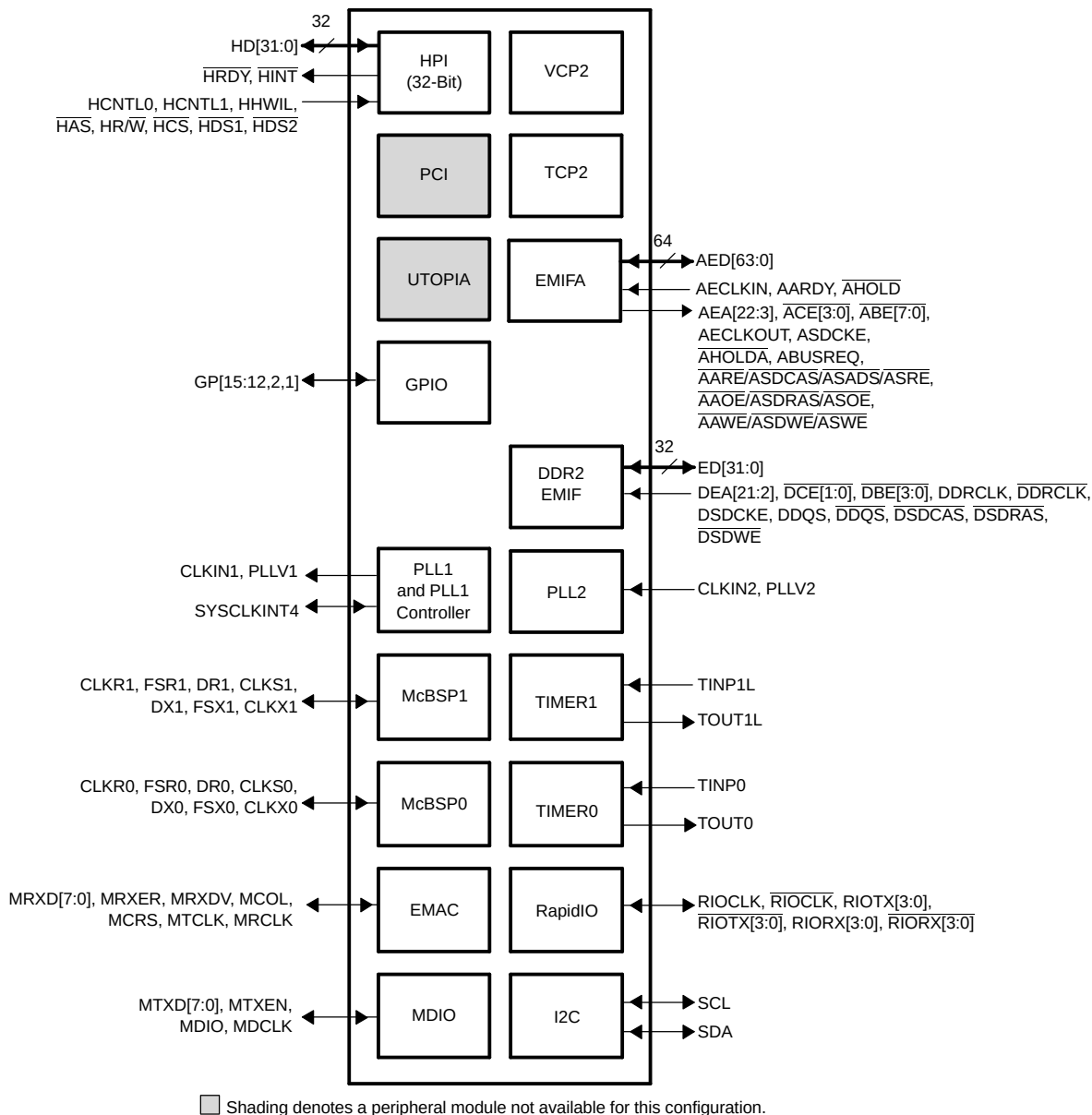
Power Saver Register Value: **TBD**
DEVSTAT Register: 0x0061 8161

PCI_EN (TBD pin) = 0 (PCI disabled, default)
EMIFA_EN (TBD pin) = 1 (EMIFA enabled)
DDR2_EN (TBD pin) = 1 (DDR2 enabled)

AEA[19:16] (BOOTMODE[3:0]) = 0001, (HPI Boot)
AEA[15] (AECLKIN_SEL) = 0, (AECLKIN, default)
AEA[14] (HPI_WIDTH) = 1, (HPI, 32-bit Operation)
AEA[13] (LENDIAN) = IPU, (Little Endian Mode, default)
AEA[12] (UTOPIA_EN) = 0, (UTOPIA disabled, default)
AEA[10:9] (MACSEL[1:0]) = 00, (10/100 MII Mode)

AEA[8] (PCI_EEA) = 0, (PCI EEPROM Auto-Init disabled, default)
AEA[7] = 0, (do not oppose IPD)
AEA[6] (PCI66) = 0, (PCI 33 MHz [default, don't care])
AEA[5] (MCBSP1_EN) = 0, (McBSP1 disabled, default)
AEA[4] (SYSCLKOUT_EN) = 1, (SYSCLK3 pin function)
AEA[2:0] (CFGPGP[2:0]) = 000 (default)

Figure 3-3. Configuration Example A (McBSP + HPI32 + I2C + EMIFA + DDR2 EMIF + TIMERS + RapidIO + EMAC (MII) + MDIO)



Power Saver Register Value: **TBD**
DEVSTAT Register: 0x0061 C161

PCI_EN (TBD pin) = 0 (PCI disabled, default)
EMIFA_EN (TBD pin) = 1 (EMIFA enabled)
DDR2_EN (TBD pin) = 1 (DDR2 enabled)

AEA[19:16] (BOOTMODE[3:0]) = 0001, (HPI Boot)
AEA[15] (AECLKIN_SEL) = 0, (AECLKIN, default)
AEA[14] (HPI_WIDTH) = 1, (HPI, 32-bit Operation)
AEA[13] (LENDIAN) = IPU, (Little Endian Mode, default)
AEA[12] (UTOPIA_EN) = 0, (UTOPIA disabled, default)
AEA[10:9] (MACSEL[1:0]) = 00, (10/100 MII Mode)

AEA[8] (PCI_EEAI) = 0, (PCI EEPROM Auto-Init disabled, default)
AEA[7] = 0, (do not oppose IPD)
AEA[6] (PCI66) = 0, (PCI 33 MHz [default, don't care])
AEA[5] (MCBSP1_EN) = 1, (McBSP1 enabled)
AEA[4] (SYSCLKOUT_EN) = 1, (SYSCLK3 pin function)
AEA[2:0] (CFGGP[2:0]) = 000 (default)

Figure 3-4. Configuration Example B (2 McBSPs + HPI32 + I2C + EMIFA + DDR2 EMIF + TIMERS + RapidIO + EMAC (GMII) + MDIO)

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4 Device Operating Conditions

4.1 Absolute Maximum Ratings Over Operating Case Temperature Range

Supply voltage ranges:	$CV_{DD}^{(1)}$	- 0.3 V to 1.8 V
	$DV_{DD33}^{(1)}$ TBD	-0.3 V to 4 V
Input voltage range:	V_I	-0.3 V to 4 V
Output voltage range:	V_O	-0.3 V to 4 V
Operating case temperature range, T_C : (default)		0°C to 90°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) All voltage values are with respect to V_{SS} .

4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core	1.16	1.2	1.23	V
DV_{DD33}	Supply voltage, I/O	3.14	3.3	3.46	V
DV_{DD18}	Supply voltage, I/O [required only for DDR2 EMIF IO]	1.71	1.8	1.89	V
DV_{DD15}	Supply voltage, I/O [required only for EMAC RGMII]	1.43	1.5	1.57	V
DV_{DD12}	Supply voltage, I/O [required only for RapidIO (RIO)]	1.14	1.2	1.26	V
V_{SS}	Supply ground	0	0	0	V
V_{IH}	High-level input voltage TBD	TBD			V
V_{IL}	Low-level input voltage TBD			TBD	V
T_C	Operating case temperature	0		90	°C

5 C64x+ Megamodule

The C64x+ Megamodule consists of several components — the C64x+ CPU Core, the L1 memory and cache controllers, the L2 memory and cache controller, the external memory controller with an internal DMA (IDMA), and the system components.

For more detailed information on the TMS320C64x+ Megamodule on the C6455 device, see the *TMS320C64x+ Megamodule Applications Report* (literature number SPRAA68).

5.1 Memory Architecture

All memory on the C6455 has a unique location in the memory map (see C6455 Memory Map Summary, [Table 2-2](#)).

5.2 C64x+ Megamodule Register Description(s)

Table 5-1. CPU MegaModule Powerdown Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0181 0000	CMD	Powerdown control command register
0184 0004 - 0184	-	TBD

Table 5-2. CPU MegaModule Memory Protection Registers (L1/L2 Control)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 A000	L2MPFAR	L2 memory protection fault address register
0184 A004	L2MPFSR	L2 memory protection fault status register
0184 A008	L2MPFCR	L2 memory protection fault command register
0184 A00C - 0184 A0FF	-	Reserved
0184 A100	L2MPLK0	L2 memory protection lock key bits [31:0]
0184 A104	L2MPLK1	L2 memory protection lock key bits [63:32]
0184 A108	L2MPLK2	L2 memory protection lock key bits [95:64]
0184 A10C	L2MPLK3	L2 memory protection lock key bits [127:96]
0184 A110	L2MPLKCMD	L2 memory protection lock key command register
0184 A114	L2MPLKSTAT	L2 memory protection lock key status register
0184 A118 - 0184 A1FF	-	Reserved
0184 A200	L2MPPA0	L2 memory protection page attribute register 0
0184 A204	L2MPPA1	L2 memory protection page attribute register 1
0184 A208	L2MPPA2	L2 memory protection page attribute register 2
0184 A20C	L2MPPA3	L2 memory protection page attribute register 3
0184 A210	L2MPPA4	L2 memory protection page attribute register 4
0184 A214	L2MPPA5	L2 memory protection page attribute register 5
0184 A218	L2MPPA6	L2 memory protection page attribute register 6
0184 A21C	L2MPPA7	L2 memory protection page attribute register 7
0184 A220	L2MPPA8	L2 memory protection page attribute register 8
0184 A224	L2MPPA9	L2 memory protection page attribute register 9
0184 A228	L2MPPA10	L2 memory protection page attribute register 10
0184 A22C	L2MPPA11	L2 memory protection page attribute register 11
0184 A230	L2MPPA12	L2 memory protection page attribute register 12
0184 A234	L2MPPA13	L2 memory protection page attribute register 13
0184 A238	L2MPPA14	L2 memory protection page attribute register 14
0184 A23C	L2MPPA15	L2 memory protection page attribute register 15
0184 A240	L2MPPA16	L2 memory protection page attribute register 16
0184 A244	L2MPPA17	L2 memory protection page attribute register 17
0184 A248	L2MPPA18	L2 memory protection page attribute register 18
0184 A24C	L2MPPA19	L2 memory protection page attribute register 19
0184 A250	L2MPPA20	L2 memory protection page attribute register 20
0184 A254	L2MPPA21	L2 memory protection page attribute register 21
0184 A258	L2MPPA22	L2 memory protection page attribute register 22
0184 A25C	L2MPPA23	L2 memory protection page attribute register 23
0184 A260	L2MPPA24	L2 memory protection page attribute register 24

Table 5-2. CPU MegaModule Memory Protection Registers (L1/L2 Control) (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 A264	L2MPPA25	L2 memory protection page attribute register 25
0184 A268	L2MPPA26	L2 memory protection page attribute register 26
0184 A26C	L2MPPA27	L2 memory protection page attribute register 27
0184 A270	L2MPPA28	L2 memory protection page attribute register 28
0184 A274	L2MPPA29	L2 memory protection page attribute register 29
0184 A278	L2MPPA30	L2 memory protection page attribute register 30
0184 A27C	L2MPPA31	L2 memory protection page attribute register 31
0184 A280	L2MPPA32	L2 memory protection page attribute register 32
0184 A284	L2MPPA33	L2 memory protection page attribute register 33
0184 A288	L2MPPA34	L2 memory protection page attribute register 34
0184 A28C	L2MPPA35	L2 memory protection page attribute register 35
0184 A290	L2MPPA36	L2 memory protection page attribute register 36
0184 A294	L2MPPA37	L2 memory protection page attribute register 37
0184 A298	L2MPPA38	L2 memory protection page attribute register 38
0184 A29C	L2MPPA39	L2 memory protection page attribute register 39
0184 A2A0	L2MPPA40	L2 memory protection page attribute register 40
0184 A2A4	L2MPPA41	L2 memory protection page attribute register 41
0184 A2A8	L2MPPA42	L2 memory protection page attribute register 42
0184 A2AC	L2MPPA43	L2 memory protection page attribute register 43
0184 A2B0	L2MPPA44	L2 memory protection page attribute register 44
0184 A2B4	L2MPPA45	L2 memory protection page attribute register 45
0184 A2B8	L2MPPA46	L2 memory protection page attribute register 46
0184 A2BC	L2MPPA47	L2 memory protection page attribute register 47
0184 A2C0	L2MPPA48	L2 memory protection page attribute register 48
0184 A2C4	L2MPPA49	L2 memory protection page attribute register 49
0184 A2C8	L2MPPA50	L2 memory protection page attribute register 50
0184 A2CC	L2MPPA51	L2 memory protection page attribute register 51
0184 A2D0	L2MPPA52	L2 memory protection page attribute register 52
0184 A2D4	L2MPPA53	L2 memory protection page attribute register 53
0184 A2D8	L2MPPA54	L2 memory protection page attribute register 54
0184 A2DC	L2MPPA55	L2 memory protection page attribute register 55
0184 A2E0	L2MPPA56	L2 memory protection page attribute register 56
0184 A2E4	L2MPPA57	L2 memory protection page attribute register 57
0184 A2E8	L2MPPA58	L2 memory protection page attribute register 58
0184 A2EC	L2MPPA59	L2 memory protection page attribute register 59
0184 A2F0	L2MPPA60	L2 memory protection page attribute register 60
0184 A2F4	L2MPPA61	L2 memory protection page attribute register 61
0184 A2F8	L2MPPA62	L2 memory protection page attribute register 62
0184 A2FC	L2MPPA63	L2 memory protection page attribute register 63
0184 A300 - 0184 A3FF	-	Reserved
0184 A400	L1PMPFAR	L1 program (L1P) memory protection fault address register
0184 A404	L1PMPFSR	L1P memory protection fault status register
0184 A408	L1PMPFCR	L1P memory protection fault command register
0184 A40C - 0184 A4FF	-	Reserved
0184 A500	L1PMPLK0	L1P memory protection lock key bits [31:0]
0184 A504	L1PMPLK1	L1P memory protection lock key bits [63:32]
0184 A508	L1PMPLK2	L1P memory protection lock key bits [95:64]

Table 5-2. CPU MegaModule Memory Protection Registers (L1/L2 Control) (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 A50C	L1PMPLK3	L1P memory protection lock key bits [127:96]
0184 A510	L1PMPLKCMD	L1P memory protection lock key command register
0184 A514	L1PMPLKSTAT	L1P memory protection lock key status register
0184 A518 - 0184 A5FF	-	Reserved
0184 A600	L1PMPPA0	L1P memory protection page attribute register 0
0184 A604	L1PMPPA1	L1P memory protection page attribute register 1
0184 A608	L1PMPPA2	L1P memory protection page attribute register 2
0184 A60C	L1PMPPA3	L1P memory protection page attribute register 3
0184 A610	L1PMPPA4	L1P memory protection page attribute register 4
0184 A614	L1PMPPA5	L1P memory protection page attribute register 5
0184 A618	L1PMPPA6	L1P memory protection page attribute register 6
0184 A61C	L1PMPPA7	L1P memory protection page attribute register 7
0184 A620	L1PMPPA8	L1P memory protection page attribute register 8
0184 A624	L1PMPPA9	L1P memory protection page attribute register 9
0184 A628	L1PMPPA10	L1P memory protection page attribute register 10
0184 A62C	L1PMPPA11	L1P memory protection page attribute register 11
0184 A630	L1PMPPA12	L1P memory protection page attribute register 12
0184 A634	L1PMPPA13	L1P memory protection page attribute register 13
0184 A638	L1PMPPA14	L1P memory protection page attribute register 14
0184 A63C	L1PMPPA15	L1P memory protection page attribute register 15
0184 A640	L1PMPPA16	L1P memory protection page attribute register 16
0184 A644	L1PMPPA17	L1P memory protection page attribute register 17
0184 A648	L1PMPPA18	L1P memory protection page attribute register 18
0184 A64C	L1PMPPA19	L1P memory protection page attribute register 19
0184 A650	L1PMPPA20	L1P memory protection page attribute register 20
0184 A654	L1PMPPA21	L1P memory protection page attribute register 21
0184 A658	L1PMPPA22	L1P memory protection page attribute register 22
0184 A65C	L1PMPPA23	L1P memory protection page attribute register 23
0184 A660	L1PMPPA24	L1P memory protection page attribute register 24
0184 A664	L1PMPPA25	L1P memory protection page attribute register 25
0184 A668	L1PMPPA26	L1P memory protection page attribute register 26
0184 A66C	L1PMPPA27	L1P memory protection page attribute register 27
0184 A670	L1PMPPA28	L1P memory protection page attribute register 28
0184 A674	L1PMPPA29	L1P memory protection page attribute register 29
0184 A678	L1PMPPA30	L1P memory protection page attribute register 30
0184 A67C	L1PMPPA31	L1P memory protection page attribute register 31
0184 A680 - 0184 ABFF	-	Reserved
0184 AC00	L1DMPFAR	L1 data (L1D) memory protection fault address register
0184 AC04	L1DMPFSR	L1D memory protection fault status register
0184 AC08	L1DMPFCR	L1D memory protection fault command register
0184 AC0C - 0184 ACFF	-	Reserved
0184 AD00	L1DMPLK0	L1D memory protection lock key bits [31:0]
0184 AD04	L1DMPLK1	L1D memory protection lock key bits [63:32]
0184 AD08	L1DMPLK2	L1D memory protection lock key bits [95:64]
0184 AD0C	L1DMPLK3	L1D memory protection lock key bits [127:96]
0184 AD10	L1DMPLKCMD	L1D memory protection lock key command register
0184 AD14	L1DMPLKSTAT	L1D memory protection lock key status register

Table 5-2. CPU MegaModule Memory Protection Registers (L1/L2 Control) (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 AD18 - 0184 ADFF	-	Reserved
0184 AE00	L1DMPPA0	L1D memory protection page attribute register 0
0184 AE04	L1DMPPA1	L1D memory protection page attribute register 1
0184 AE08	L1DMPPA2	L1D memory protection page attribute register 2
0184 AE0C	L1DMPPA3	L1D memory protection page attribute register 3
0184 AE10	L1DMPPA4	L1D memory protection page attribute register 4
0184 AE14	L1DMPPA5	L1D memory protection page attribute register 5
0184 AE18	L1DMPPA6	L1D memory protection page attribute register 6
0184 AE1C	L1DMPPA7	L1D memory protection page attribute register 7
0184 AE20	L1DMPPA8	L1D memory protection page attribute register 8
0184 AE24	L1DMPPA9	L1D memory protection page attribute register 9
0184 AE28	L1DMPPA10	L1D memory protection page attribute register 10
0184 AE2C	L1DMPPA11	L1D memory protection page attribute register 11
0184 AE30	L1DMPPA12	L1D memory protection page attribute register 12
0184 AE34	L1DMPPA13	L1D memory protection page attribute register 13
0184 AE38	L1DMPPA14	L1D memory protection page attribute register 14
0184 AE3C	L1DMPPA15	L1D memory protection page attribute register 15
0184 AE40	L1DMPPA16	L1D memory protection page attribute register 16
0184 AE44	L1DMPPA17	L1D memory protection page attribute register 17
0184 AE48	L1DMPPA18	L1D memory protection page attribute register 18
0184 AE4C	L1DMPPA19	L1D memory protection page attribute register 19
0184 AE50	L1DMPPA20	L1D memory protection page attribute register 20
0184 AE54	L1DMPPA21	L1D memory protection page attribute register 21
0184 AE58	L1DMPPA22	L1D memory protection page attribute register 22
0184 AE5C	L1DMPPA23	L1D memory protection page attribute register 23
0184 AE60	L1DMPPA24	L1D memory protection page attribute register 24
0184 AE64	L1DMPPA25	L1D memory protection page attribute register 25
0184 AE68	L1DMPPA26	L1D memory protection page attribute register 26
0184 AE6C	L1DMPPA27	L1D memory protection page attribute register 27
0184 AE70	L1DMPPA28	L1D memory protection page attribute register 28
0184 AE74	L1DMPPA29	L1D memory protection page attribute register 29
0184 AE78	L1DMPPA30	L1D memory protection page attribute register 30
0184 AE7C	L1DMPPA31	L1D memory protection page attribute register 31
0184 AE80 - 0185 FFFF	-	Reserved

Table 5-3. CPU MegaModule Interrupt Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0180 0000	EVTFLAG0	Event flag register 0 (Events [31:0])
0180 0004	EVTFLAG1	
0180 0008	EVTFLAG2	
0180 000C	EVTFLAG3	
0180 0010 - 0180 001C	-	Reserved
0180 0020	EVTSET0	Event set register 0 (Events [31:0])
0180 0024	EVTSET1	
0180 0028	EVTSET2	

Table 5-3. CPU MegaModule Interrupt Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0180 002C	EVTSET3	
0180 0030 - 0180 003C	-	Reserved
0180 0040	EVTCLR0	Event clear register 0 (Events [31:0])
0180 0044	EVTCLR1	
0180 0048	EVTCLR2	
0180 004C	EVTCLR3	
0180 0050 - 0180 007C	-	Reserved
0180 0080	EVTMASK0	Event mask register 0 (Events [31:0])
0180 0084	EVTMASK1	
0180 0088	EVTMASK2	
0180 008C	EVTMASK3	
0180 0090 - 0180 009C	-	Reserved
0180 00A0	MEVTFLAG0	Masked event flag status register 0 (Events [31:0])
0180 00A4	MEVTFLAG1	
0180 00A8	MEVTFLAG2	
0180 00AC	MEVTFLAG3	
0180 00B0 - 0180 00BC	-	Reserved
0180 00C0	EXCMASK0	Exception mask register 0 (Events [31:0])
0180 00C4	EXCMASK1	
0180 00C8	EXCMASK2	
0180 00CC	EXCMASK3	
0180 00D0 - 0180 00DC	-	Reserved
0180 00E0	MEXCFLAG0	Masked exception flag status register 0 (Events [31:0])
0180 00E4	MEXCFLAG1	
0180 00E8	MEXCFLAG2	
0180 00EC	MEXCFLAG3	
0180 00F0 - 0180 00FC	-	Reserved
0180 0100	-	Reserved
0180 0104	INTMUX1	Interrupt multiplexor register 0
0180 0108	INTMUX2	
0180 010C	INTMUX3	
0180 0110 - 0180 013C	-	Reserved
0180 0140	AEGMUX0	Advanced event generator mux register 0
0180 0144	AEGMUX1	
0180 0148 - 0180 017C	-	Reserved
0180 0180	INTXSTAT	Interrupt exception status register
0180 0184	INTXCLR	Interrupt exception clear register
0180 0188	INTDMASK	Dropped interrupt mask register
0180 0188 - 0180 01BC	-	Reserved
0180 01C0	EVTASRT	Event asserting register

Table 5-4. CPU MegaModule IDMA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0182 0000	IDMA0STAT	IDMA Channel 0 Status Register
0182 0004	IDMA0MASK	IDMA Channel 0 Mask Register
0182 0008	IDMA0SRC	IDMA Channel 0 Source Address Register
0182 000C	IDMA0DST	IDMA Channel 0 Destination Address Register
0182 0010	IDMA0CNT	IDMA Channel 0 Count Register
0182 0014 - 0182 00FC	-	Reserved
0182 0100	IDMA1STAT	IDMA Channel 1 Status Register
0182 0104	-	Reserved
0182 0108	IDMA1SRC	IDMA Channel 1 Source Address Register
0182 010C	IDMA1DST	IDMA Channel 1 Destination Address Register
0182 0110	IDMA1CNT	IDMA Channel 1 Count Register
0182 0114 - 0182 017C	-	Reserved
0182 0180	-	Reserved
0182 0184 - 0182 01FF	-	Reserved

Table 5-5. CPU MegaModule Configuration Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0182 0300	MPFAR	Memory Protection Fault Address Register
0182 0304	MPFSR	Memory Protection Fault Status Register
0182 0308	MPFCR	Memory Protection Fault Command Register

Table 5-6. CPU MegaModule Cache Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 0000	L2CFG	L2 Cache Configuration Register
0184 0004 - 0184 001C	-	Reserved
0184 0020	L1PCFG	L1P Configuration Register
0184 0024	L1PCC	L1P Cache Control Register
0184 0028 - 0184 003C	-	Reserved
0184 0040	L1DCFG	L1D Configuration Register
0184 0044	L1DCC	L1D Cache Control Register
0184 0048 - 0184 3FFC	-	Reserved
0184 4000	L2WBAR	L2 Writeback Base Address Register - for Block Writebacks
0184 4004	L2WWC	L2 Writeback Word Count Register
0184 4008 - 0184 400C	-	Reserved
0184 4010	L2WIBAR	L2 Writeback and Invalidate Base Address Register - for Block Writebacks
0184 4014	L2WIWC	L2 Writeback and Invalidate word count register
0184 4018	L2IBAR	L2 Invalidate Base Address Register
0184 401C	L2IWC	L2 Invalidate Word Count Register
0184 4020	L1PIBAR	L1P Invalidate Base Address Register
0184 4024	L1PIWC	L1P Invalidate Word Count Register
0184 4030	L1DWIBAR	L1D Writeback and Invalidate Base Address Register
0184 4034	L1DWIWC	L1D Writeback and Invalidate Word Count Register

Table 5-6. CPU MegaModule Cache Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 4038	-	Reserved
0184 4040	L1DWBAR	L1D Writeback Base Address Register - for Block Writebacks
0184 4044	L1DWWC	L1D Writeback Word Count Register
0184 4048	L1DIBAR	L1D Invalidate Base Address Register
0184 404C	L1DIWC	L1D Invalidate Word Count Register
	-	Reserved
0184 5000	L2WB	L2 Global Writeback Register
0184 5004	L2WBINV	L2 Global Writeback and Invalidate Register
0184 5008	L2INV	L2 Global Invalidate Register
0184 500C - 0184 5024	-	Reserved
0184 5028	L1PINV	L1P Global Invalidate Register
0184 502C - 0184 503C	-	Reserved
0184 5040	L1DWB	L1D Global Writeback Register
0184 5044	L1DWBINV	L1D Global Writeback and Invalidate Register
0184 5048	L1DINV	L1D Global Invalidate Register
0184 504C - 0184 7FFC	-	Reserved
0184 8000 - 0184 81FC	MAR0 to MAR127	Reserved
0184 8200	MAR128	Memory Attribute Register 128 [MAR128] Controls EMIFA CE0 Range 8000 0000 - 80FF FFFF
0184 8204	MAR129	Controls EMIFA CE0 Range 8100 0000 - 81FF FFFF
0184 8208	MAR130	Controls EMIFA CE0 Range 8200 0000 - 82FF FFFF
0184 820C	MAR131	Controls EMIFA CE0 Range 8300 0000 - 83FF FFFF
0184 8210	MAR132	Controls EMIFA CE0 Range 8400 0000 - 84FF FFFF
0184 8214	MAR133	Controls EMIFA CE0 Range 8500 0000 - 85FF FFFF
0184 8218	MAR134	Controls EMIFA CE0 Range 8600 0000 - 86FF FFFF
0184 821C	MAR135	Controls EMIFA CE0 Range 8700 0000 - 87FF FFFF
0184 8220	MAR136	Controls EMIFA CE0 Range 8800 0000 - 88FF FFFF
0184 8224	MAR137	Controls EMIFA CE0 Range 8900 0000 - 89FF FFFF
0184 8228	MAR138	Controls EMIFA CE0 Range 8A00 0000 - 8AFF FFFF
0184 822C	MAR139	Controls EMIFA CE0 Range 8B00 0000 - 8BFF FFFF
0184 8230	MAR140	Controls EMIFA CE0 Range 8C00 0000 - 8CFF FFFF
0184 8234	MAR141	Controls EMIFA CE0 Range 8D00 0000 - 8DFF FFFF
0184 8238	MAR142	Controls EMIFA CE0 Range 8E00 0000 - 8EFF FFFF
0184 823C	MAR143	Controls EMIFA CE0 Range 8F00 0000 - 8FFF FFFF
0184 8240 - 0184 827C	MAR144 to MAR159	Reserved
0184 8280	MAR160	Controls EMIFA CE2 Range A000 0000 - A0FF FFFF
0184 8284	MAR161	Controls EMIFA CE2 Range A100 0000 - A1FF FFFF
0184 8288	MAR162	Controls EMIFA CE2 Range A200 0000 - A2FF FFFF
0184 828C	MAR163	Controls EMIFA CE2 Range A300 0000 - A3FF FFFF
0184 8290	MAR164	Controls EMIFA CE2 Range A400 0000 - A4FF FFFF
0184 8294	MAR165	Controls EMIFA CE2 Range A500 0000 - A5FF FFFF
0184 8298	MAR166	Controls EMIFA CE2 Range A600 0000 - A6FF FFFF
0184 829C	MAR167	Controls EMIFA CE2 Range A700 0000 - A7FF FFFF
0184 82A0	MAR168	Controls EMIFA CE2 Range A800 0000 - A8FF FFFF
0184 82A4	MAR169	Controls EMIFA CE2 Range A900 0000 - A9FF FFFF
0184 82A8	MAR170	Controls EMIFA CE2 Range AA00 0000 - AAFF FFFF

Table 5-6. CPU MegaModule Cache Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 82AC	MAR171	Controls EMIFA CE2 Range AB00 0000 - ABFF FFFF
0184 82B0	MAR172	Controls EMIFA CE2 Range AC00 0000 - ACFF FFFF
0184 82B4	MAR173	Controls EMIFA CE2 Range AD00 0000 - ADFF FFFF
0184 82B8	MAR174	Controls EMIFA CE2 Range AE00 0000 - AEFF FFFF
0184 82BC	MAR175	Controls EMIFA CE2 Range AF00 0000 - AFFF FFFF
0184 82C0	MAR176	Controls EMIFA CE3 Range B000 0000 - B0FF FFFF
0184 82C4	MAR177	Controls EMIFA CE3 Range B100 0000 - B1FF FFFF
0184 82C8	MAR178	Controls EMIFA CE3 Range B200 0000 - B2FF FFFF
0184 82CC	MAR179	Controls EMIFA CE3 Range B300 0000 - B3FF FFFF
0184 82D0	MAR180	Controls EMIFA CE3 Range B400 0000 - B4FF FFFF
0184 82D4	MAR181	Controls EMIFA CE3 Range B500 0000 - B5FF FFFF
0184 82D8	MAR182	Controls EMIFA CE3 Range B600 0000 - B6FF FFFF
0184 82DC	MAR183	Controls EMIFA CE3 Range B700 0000 - B7FF FFFF
0184 82E0	MAR184	Controls EMIFA CE3 Range B800 0000 - B8FF FFFF
0184 82E4	MAR185	Controls EMIFA CE3 Range B900 0000 - B9FF FFFF
0184 82E8	MAR186	Controls EMIFA CE3 Range BA00 0000 - BAFF FFFF
0184 82EC	MAR187	Controls EMIFA CE3 Range BB00 0000 - BBFF FFFF
0184 82F0	MAR188	Controls EMIFA CE3 Range BC00 0000 - BCFF FFFF
0184 82F4	MAR189	Controls EMIFA CE3 Range BD00 0000 - BDFF FFFF
0184 82F8	MAR190	Controls EMIFA CE3 Range BE00 0000 - BEFF FFFF
0184 82FC	MAR191	Controls EMIFA CE3 Range BF00 0000 - BFFF FFFF
0184 8300	MAR192	Controls EMIFA CE4 Range C000 0000 - C0FF FFFF
0184 8304	MAR193	Controls EMIFA CE4 Range C100 0000 - C1FF FFFF
0184 8308	MAR194	Controls EMIFA CE4 Range C200 0000 - C2FF FFFF
0184 830C	MAR195	Controls EMIFA CE4 Range C300 0000 - C3FF FFFF
0184 8310	MAR196	Controls EMIFA CE4 Range C400 0000 - C4FF FFFF
0184 8314	MAR197	Controls EMIFA CE4 Range C500 0000 - C5FF FFFF
0184 8318	MAR198	Controls EMIFA CE4 Range C600 0000 - C6FF FFFF
0184 831C	MAR199	Controls EMIFA CE4 Range C700 0000 - C7FF FFFF
0184 8320	MAR200	Controls EMIFA CE4 Range C800 0000 - C8FF FFFF
0184 8324	MAR201	Controls EMIFA CE4 Range C900 0000 - C9FF FFFF
0184 8328	MAR202	Controls EMIFA CE4 Range CA00 0000 - CAFF FFFF
0184 832C	MAR203	Controls EMIFA CE4 Range CB00 0000 - CBFF FFFF
0184 8330	MAR204	Controls EMIFA CE4 Range CC00 0000 - CCFF FFFF
0184 8334	MAR205	Controls EMIFA CE4 Range CD00 0000 - CDFF FFFF
0184 8338	MAR206	Controls EMIFA CE4 Range CE00 0000 - CEFF FFFF
0184 833C	MAR207	Controls EMIFA CE4 Range CF00 0000 - CFFF FFFF
0184 8340	MAR208	Controls EMIFA CE5 Range D000 0000 - D0FF FFFF
0184 8344	MAR209	Controls EMIFA CE5 Range D100 0000 - D1FF FFFF
0184 8348	MAR210	Controls EMIFA CE5 Range D200 0000 - D2FF FFFF
0184 834C	MAR211	Controls EMIFA CE5 Range D300 0000 - D3FF FFFF
0184 8350	MAR212	Controls EMIFA CE5 Range D400 0000 - D4FF FFFF
0184 8354	MAR213	Controls EMIFA CE5 Range D500 0000 - D5FF FFFF
0184 8358	MAR214	Controls EMIFA CE5 Range D600 0000 - D6FF FFFF
0184 835C	MAR215	Controls EMIFA CE5 Range D700 0000 - D7FF FFFF
0184 8360	MAR216	Controls EMIFA CE5 Range D800 0000 - D8FF FFFF
0184 8364	MAR217	Controls EMIFA CE5 Range D900 0000 - D9FF FFFF

Table 5-6. CPU MegaModule Cache Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0184 8368	MAR218	Controls EMIFA CE5 Range DA00 0000 - DAFF FFFF
0184 836C	MAR219	Controls EMIFA CE5 Range DB00 0000 - DBFF FFFF
0184 8370	MAR220	Controls EMIFA CE5 Range DC00 0000 - DCFF FFFF
0184 8374	MAR221	Controls EMIFA CE5 Range DD00 0000 - DDFF FFFF
0184 8378	MAR222	Controls EMIFA CE5 Range DE00 0000 - DEFF FFFF
0184 837C	MAR223	Controls EMIFA CE5 Range DF00 0000 - DFFF FFFF
0184 8380	MAR224	Controls DDR2 CE0 Range E000 0000 - E0FF FFFF
0184 8384	MAR225	Controls DDR2 CE0 Range E100 0000 - E1FF FFFF
0184 8388	MAR226	Controls DDR2 CE0 Range E200 0000 - E2FF FFFF
0184 838C	MAR227	Controls DDR2 CE0 Range E300 0000 - E3FF FFFF
0184 8390	MAR228	Controls DDR2 CE0 Range E400 0000 - E4FF FFFF
0184 8394	MAR229	Controls DDR2 CE0 Range E500 0000 - E5FF FFFF
0184 8398	MAR230	Controls DDR2 CE0 Range E600 0000 - E6FF FFFF
0184 839C	MAR231	Controls DDR2 CE0 Range E700 0000 - E7FF FFFF
0184 83A0	MAR232	Controls DDR2 CE0 Range E800 0000 - E8FF FFFF
0184 83A4	MAR233	Controls DDR2 CE0 Range E900 0000 - E9FF FFFF
0184 83A8	MAR234	Controls DDR2 CE0 Range EA00 0000 - EAFF FFFF
0184 83AC	MAR235	Controls DDR2 CE0 Range EB00 0000 - EBFF FFFF
0184 83B0	MAR236	Controls DDR2 CE0 Range EC00 0000 - ECFF FFFF
0184 83B4	MAR237	Controls DDR2 CE0 Range ED00 0000 - EDFF FFFF
0184 83B8	MAR238	Controls DDR2 CE0 Range EE00 0000 - EEFF FFFF
0184 83BC	MAR239	Controls DDR2 CE0 Range EF00 0000 - EFFF FFFF
0184 83C0 - 0184 83FC	MAR240 to MAR255	Reserved

Table 5-7. CPU MegaModule BandWidth Management Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
0182 0200	CPUARBE	CPU Arbitration Register
0182 0204	IDMAARBE	IDMA Arbitration Register
0182 0208	SDMAARBE	Slave DMA Arbitration Register
0182 020C	MAMARBE	Master DMA Arbitration Register
0182 0210 - 0182 02FF	-	Reserved

Table 5-8. Device Configuration Registers (Chip-Level Registers)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
02A8 0000	DEVSTAT	Device Status Register	Read-only. Provides status of the User's device configuration on reset.
02A8 0004	PRI_ALLOC	TBD Register	TBD
02A8 0008	JTAGID	JTAG and BSDL Identification Register	Read-only. Provides 32-bit JTAG ID of the device.
02A8 000C - 02AB FFFF	-	Reserved	

6 C6455 Peripheral Information and Electrical Specifications

6.1 Parameter Information

6.1.1 Parameter Information Device-Specific Information

6.2 Recommended Clock and Control Signals Transition Behavior

6.3 Power-Down Modes Logic

6.4 Power-Supply Sequencing

C6455 device recommends the power-supply sequencing be followed:

TBD

6.5 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place as many capacitors (caps) as possible close to the DSP. These caps need to be close to the DSP, no more than 1.25 cm maximum distance to be effective. Physically smaller caps are better, such as 0402, but need to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value. As with the selection of any component, verification of capacitor availability over the product's production lifetime should be considered.

6.6 Power-Down Operation

One of the power goals for the C6455 is to reduce power dissipation due to inactive/unused peripherals. A provision to turn off clocks to unused peripherals is included. The gating of these clocks is derived from boot mode settings, device configuration registers within the C64x+ Megamodule power-down controller, and/or power-down settings within the peripheral.

Any module that is not being used at all (indicated by configuration settings at reset) will have its clock disabled in order to minimize power consumption. For C6455 device, modules that may be completely disabled at reset are I2C, McBSP, UTOPIA, EMAC, RapidIO, TCP2, and VCP2.

The C6455 device allows any peripheral to be powered down through software. This, too, results in gating of the clock(s) to the powered-down peripheral.

6.7 Powersaver

TBD

6.7.1 Powersaver Device-Specific Information

TBD

6.7.2 Powersaver Peripheral Register Description(s)

Table 6-1. Powersaver Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02AC 0000	-	Reserved

Table 6-1. Powersaver Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02AC 0004	LCK	Lock register
02AC 0008	MDCTL0	Module state control register 0
02AC 000C	-	Reserved
02AC 0010	-	Reserved
02AC 0014	MDSTAT0	Module status register 0
02AC 0018	MDSTAT1	Module status register 1
02AC 001C	-	Reserved
02AC 0020	-	Reserved
02AC 0024	-	Reserved
02AC 0028	-	Reserved
02AC 002C	EMIFCLKGAT	Clock gating for EMIFA, DDR2
02AC 0030 - 02AF FFFF	-	Reserved

6.8 Enhanced Direct Memory Access (EDMA) Controller

The EDMA controller handles all data transfers between the level-two (L2) cache/memory controller and the device peripherals on the C6455 DSP. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses.

6.8.1 EDMA Device-Specific Information

The EDMA on the C6455 device is further enhanced from any other C64x generation DSP device. The C6455 device separates out the functional components of the EDMA into several distinct components.

- Crossbar
- Channel Controller (CC)
- Transfer Controller (TC)

Crossbar: The Crossbar is an n-port to m-port crossbar that allows N master peripherals to connect to M slave peripherals. The Crossbar allows seamless arbitration between the N masters to each slave.

EDMA: The EDMA is the engine that performs slave-to-slave data transfers. Since all connections through the Crossbar are master/slave, the EDMA must exist to allow transfers off of global (i.e., non-peripheral-specific) system events or software-driven transfers. The EDMA consists of two subcomponents:

- Channel Controller (CC): The CC contains 64 channels synchronized to system events. The CC contains a parameterizeable RAM that holds transfer parameters for the 64 channels, plus reload space. Linking and chaining are used to allow synchronization between transfers and auto-reload capabilities for each channel. Enhancements include:
 - Orthogonal completion codes - the OCCs are now more exclusive when selecting whether to interrupt the CPU or chain to another channel. This simplifies the EDMA driver.
 - Quick DMA support (QDMA) - Formerly performed by the C64x Megamodule, the CC allows for software-driven transfers. Rather than requiring a system event, a transfer is started as soon as the parameters are written.
- Transfer Controller (TC): The TC is the EDMA engine that actually performs the reads and writes, and buffers the data being transferred in an intermediate FIFO. The TC contains 4 DMA channels, and is programmed by the CC.

For the C6455 EDMA block diagram, see [Figure 6-1](#).

Figure 6-1. EDMA Block Diagram

6.8.1.1 EDMA Channel Synchronization Events

The C64x+ EDMA3 supports up to TBD EDMA channels which service peripheral devices and external memory. TBD table lists the source of C64x+ EDMA3 synchronization events associated with each of the programmable EDMA channels. For the C6455 device, the association of an event to a channel is fixed; each of the EDMA channels has one specific event associated with it. These specific events are captured in the EDMA3 event registers (TBD, TBD) even if the events are disabled by the EDMA event enable registers (TBD, TBD). The priority of each event can be specified independently in the transfer parameters stored in the EDMA parameter RAM. For more detailed information on the EDMA module and how EDMA events are enabled, captured, processed, linked, chained, and cleared, etc., see the *TMS320C64x+ DSP EDMA3 Controller Reference Guide* (literature number SPRUTBD).

6.8.2 EDMA Peripheral Register Description(s)

Table 6-2. EDMA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 0000 - 02A0 00FC	-	Reserved
02A0 0100	DCHMAP0	EDMA Channel 0 Mapping to PaRAM
02A0 0104	DCHMAP1	EDMA Channel 1 Mapping to PaRAM
02A0 0108	DCHMAP2	EDMA Channel 2 Mapping to PaRAM
02A0 010C	DCHMAP3	EDMA Channel 3 Mapping to PaRAM
02A0 0110	DCHMAP4	EDMA Channel 4 Mapping to PaRAM
02A0 0114	DCHMAP5	EDMA Channel 5 Mapping to PaRAM
02A0 0118	DCHMAP6	EDMA Channel 6 Mapping to PaRAM
02A0 011C	DCHMAP7	EDMA Channel 7 Mapping to PaRAM
02A0 0120	DCHMAP8	EDMA Channel 8 Mapping to PaRAM
02A0 0124	DCHMAP9	EDMA Channel 9 Mapping to PaRAM
02A0 0128	DCHMAP10	EDMA Channel 10 Mapping to PaRAM
02A0 012C	DCHMAP11	EDMA Channel 11 Mapping to PaRAM
02A0 0130	DCHMAP12	EDMA Channel 12 Mapping to PaRAM
02A0 0134	DCHMAP13	EDMA Channel 13 Mapping to PaRAM
02A0 0138	DCHMAP14	EDMA Channel 14 Mapping to PaRAM
02A0 013C	DCHMAP15	EDMA Channel 15 Mapping to PaRAM
02A0 0140	DCHMAP16	EDMA Channel 16 Mapping to PaRAM
02A0 0144	DCHMAP17	EDMA Channel 17 Mapping to PaRAM
02A0 0148	DCHMAP18	EDMA Channel 18 Mapping to PaRAM
02A0 014C	DCHMAP19	EDMA Channel 19 Mapping to PaRAM
02A0 0150	DCHMAP20	EDMA Channel 20 Mapping to PaRAM
02A0 0154	DCHMAP21	EDMA Channel 21 Mapping to PaRAM
02A0 0158	DCHMAP22	EDMA Channel 22 Mapping to PaRAM
02A0 015C	DCHMAP23	EDMA Channel 23 Mapping to PaRAM
02A0 0160	DCHMAP24	EDMA Channel 24 Mapping to PaRAM
02A0 0164	DCHMAP25	EDMA Channel 25 Mapping to PaRAM
02A0 0168	DCHMAP26	EDMA Channel 26 Mapping to PaRAM
02A0 016C	DCHMAP27	EDMA Channel 27 Mapping to PaRAM

Table 6-2. EDMA Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 0170	DCHMAP28	EDMA Channel 28 Mapping to PaRAM
02A0 0174	DCHMAP29	EDMA Channel 29 Mapping to PaRAM
02A0 0178	DCHMAP30	EDMA Channel 30 Mapping to PaRAM
02A0 017C	DCHMAP31	EDMA Channel 31 Mapping to PaRAM
02A0 0180	DCHMAP32	EDMA Channel 32 Mapping to PaRAM
02A0 0184	DCHMAP33	EDMA Channel 33 Mapping to PaRAM
02A0 0188	DCHMAP34	EDMA Channel 34 Mapping to PaRAM
02A0 018C	DCHMAP35	EDMA Channel 35 Mapping to PaRAM
02A0 0190	DCHMAP36	EDMA Channel 36 Mapping to PaRAM
02A0 0194	DCHMAP37	EDMA Channel 37 Mapping to PaRAM
02A0 0198	DCHMAP38	EDMA Channel 38 Mapping to PaRAM
02A0 019C	DCHMAP39	EDMA Channel 39 Mapping to PaRAM
02A0 01A0	DCHMAP40	EDMA Channel 40 Mapping to PaRAM
02A0 01A4	DCHMAP41	EDMA Channel 41 Mapping to PaRAM
02A0 01A8	DCHMAP42	EDMA Channel 42 Mapping to PaRAM
02A0 01AC	DCHMAP43	EDMA Channel 43 Mapping to PaRAM
02A0 01B0	DCHMAP44	EDMA Channel 44 Mapping to PaRAM
02A0 01B4	DCHMAP45	EDMA Channel 45 Mapping to PaRAM
02A0 01B8	DCHMAP46	EDMA Channel 46 Mapping to PaRAM
02A0 01BC	DCHMAP47	EDMA Channel 47 Mapping to PaRAM
02A0 01C0	DCHMAP48	EDMA Channel 48 Mapping to PaRAM
02A0 01C4	DCHMAP49	EDMA Channel 49 Mapping to PaRAM
02A0 01C8	DCHMAP50	EDMA Channel 50 Mapping to PaRAM
02A0 01CC	DCHMAP51	EDMA Channel 51 Mapping to PaRAM
02A0 01D0	DCHMAP52	EDMA Channel 52 Mapping to PaRAM
02A0 01D4	DCHMAP53	EDMA Channel 53 Mapping to PaRAM
02A0 01D8	DCHMAP54	EDMA Channel 54 Mapping to PaRAM
02A0 01DC	DCHMAP55	EDMA Channel 55 Mapping to PaRAM
02A0 01E0	DCHMAP56	EDMA Channel 56 Mapping to PaRAM
02A0 01E4	DCHMAP57	EDMA Channel 57 Mapping to PaRAM
02A0 01E8	DCHMAP58	EDMA Channel 58 Mapping to PaRAM
02A0 01EC	DCHMAP59	EDMA Channel 59 Mapping to PaRAM
02A0 01F0	DCHMAP60	EDMA Channel 60 Mapping to PaRAM
02A0 01F4	DCHMAP61	EDMA Channel 61 Mapping to PaRAM
02A0 01F8	DCHMAP62	EDMA Channel 62 Mapping to PaRAM
02A0 01FC	DCHMAP63	EDMA Channel 63 Mapping to PaRAM
02A0 0200	QCHMAP0	EDMA QDMA Channel 0 Mapping to PaRAM
02A0 0204	QCHMAP1	EDMA QDMA Channel 1 Mapping to PaRAM
02A0 0208	QCHMAP2	EDMA QDMA Channel 2 Mapping to PaRAM
02A0 020C	QCHMAP3	EDMA QDMA Channel 3 Mapping to PaRAM
02A0 0210 - 02A0 021C	-	Reserved
02A0 0220 - 02A0 023C	-	Reserved
02A0 0240	DMAQNUM0	EDMA Que Number 0; Channels 00 thru 07
02A0 0244	DMAQNUM1	EDMA Que Number 1; Channels 08 thru 15
02A0 0248	DMAQNUM2	EDMA Que Number 2; Channels 16 thru 23
02A0 024C	DMAQNUM3	EDMA Que Number 3; Channels 24 thru 31
02A0 0250 - 02A0 025C	-	Reserved

Table 6-2. EDMA Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 0260	QDMAQNUM	EDMA QDMA Que Number
02A0 0264 - 02A0 027C	-	Reserved
02A0 0280	QUETCMAP	EDMA Queue to TC Mapping
02A0 0284	QUEPRI	EDMA Queue Priority
02A0 0288 - 02A0 02FC	-	Reserved
02A0 0300	EMR	EDMA Event Missed Register
02A0 0304	EMRH	EDMA Event Missed High Register
02A0 0308	EMCR	EDMA Event Missed Clear Register
02A0 030C	EMCRH	EDMA Event Missed Clear High Register
02A0 0310	QEMR	EDMA QDMA Event Missed Register
02A0 0314	QEMCR	EDMA QDMA Event Missed Clear Register
02A0 0318	CCERR	EDMA CC Error Register
02A0 031C	CCERRCLR	EDMA CC Error Clear Register
02A0 0320	EEVAL	EDMA
02A0 0324 - 02A0 033C	-	Reserved
02A0 0340	DRAE0	EDMA Region Access Enable 0 Register
02A0 0344	DRAEH0	EDMA Region Access High Enable 0 Register
02A0 0348	DRAE1	EDMA Region Access Enable 1 Register
02A0 034C	DRAEH1	EDMA Region Access High Enable 1 Register
02A0 0350	DRAE2	EDMA Region Access Enable 2 Register
02A0 0354	DRAEH2	EDMA Region Access High Enable 2 Register
02A0 0358	DRAE3	EDMA Region Access Enable 3 Register
02A0 035C	DRAEH3	EDMA Region Access High Enable 3 Register
02A0 0360	DRAE4	EDMA Region Access Enable 4 Register
02A0 0364	DRAEH4	EDMA Region Access High Enable 4 Register
02A0 0368	DRAE5	EDMA Region Access Enable 5 Register
02A0 036C	DRAEH5	EDMA Region Access High Enable 5 Register
02A0 0370	DRAE6	EDMA Region Access Enable 6 Register
02A0 0374	DRAEH6	EDMA Region Access High Enable 6 Register
02A0 0378	DRAE7	EDMA Region Access Enable 7 Register
02A0 0380	DRAEH7	EDMA Region Access High Enable 7 Register
02A0 0384	QRAE0	EDMA QDMA Region Access Enable 0
02A0 0388	QRAE1	EDMA QDMA Region Access Enable 1
02A0 038C	QRAE2	EDMA QDMA Region Access Enable 2
02A0 0390	QRAE3	EDMA QDMA Region Access Enable 3
02A0 0394 - 02A0 039C	-	Reserved
02A0 0400	Q0E0	EDMA Event Q0 Entry 0 / Event Q0 Base
02A0 0404	Q0E1	EDMA Event Q0 Entry 1 / Event Q0 Base
02A0 0408	Q0E2	EDMA Event Q0 Entry 2 / Event Q0 Base
02A0 040C	Q0E3	EDMA Event Q0 Entry 3 / Event Q0 Base
02A0 0410	Q0E4	EDMA Event Q0 Entry 4 / Event Q0 Base
02A0 0414	Q0E5	EDMA Event Q0 Entry 5 / Event Q0 Base
02A0 0418	Q0E6	EDMA Event Q0 Entry 6 / Event Q0 Base
02A0 041C	Q0E7	EDMA Event Q0 Entry 7 / Event Q0 Base
02A0 0420	Q0E8	EDMA Event Q0 Entry 8 / Event Q0 Base
02A0 0424	Q0E9	EDMA Event Q0 Entry 9 / Event Q0 Base
02A0 0428	Q0E10	EDMA Event Q0 Entry 10 / Event Q0 Base

Table 6-2. EDMA Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 042C	Q0E11	EDMA Event Q0 Entry 11 / Event Q0 Base
02A0 0430	Q0E12	EDMA Event Q0 Entry 12 / Event Q0 Base
02A0 0434	Q0E13	EDMA Event Q0 Entry 13 / Event Q0 Base
02A0 0438	Q0E14	EDMA Event Q0 Entry 14 / Event Q0 Base
02A0 043C	Q0E15	EDMA Event Q0 Entry 15 / Event Q0 Base
02A0 0440	Q1E0	EDMA Event Q1 Entry 0 / Event Q1 Base
02A0 0444	Q1E1	EDMA Event Q1 Entry 1 / Event Q1 Base
02A0 0448	Q1E2	EDMA Event Q1 Entry 2 / Event Q1 Base
02A0 044C	Q1E3	EDMA Event Q1 Entry 3 / Event Q1 Base
02A0 0450	Q1E4	EDMA Event Q1 Entry 4 / Event Q1 Base
02A0 0454	Q1E5	EDMA Event Q1 Entry 5 / Event Q1 Base
02A0 0458	Q1E6	EDMA Event Q1 Entry 6 / Event Q1 Base
02A0 045C	Q1E7	EDMA Event Q1 Entry 7 / Event Q1 Base
02A0 0460	Q1E8	EDMA Event Q1 Entry 8 / Event Q1 Base
02A0 0464	Q1E9	EDMA Event Q1 Entry 9 / Event Q1 Base
02A0 0468	Q1E10	EDMA Event Q1 Entry 10 / Event Q1 Base
02A0 046C	Q1E11	EDMA Event Q1 Entry 11 / Event Q1 Base
02A0 0470	Q1E12	EDMA Event Q1 Entry 12 / Event Q1 Base
02A0 0474	Q1E13	EDMA Event Q1 Entry 13 / Event Q1 Base
02A0 0478	Q1E14	EDMA Event Q1 Entry 14 / Event Q1 Base
02A0 047C	Q1E15	EDMA Event Q1 Entry 15 / Event Q1 Base
02A0 0480	Q2E0	EDMA Event Q2 Entry 0 / Event Q2 Base
02A0 0484	Q2E1	EDMA Event Q2 Entry 1 / Event Q2 Base
02A0 0488	Q2E2	EDMA Event Q2 Entry 2 / Event Q2 Base
02A0 048C	Q2E3	EDMA Event Q2 Entry 3 / Event Q2 Base
02A0 0490	Q2E4	EDMA Event Q2 Entry 4 / Event Q2 Base
02A0 0494	Q2E5	EDMA Event Q2 Entry 5 / Event Q2 Base
02A0 0498	Q2E6	EDMA Event Q2 Entry 6 / Event Q2 Base
02A0 049C	Q2E7	EDMA Event Q2 Entry 7 / Event Q2 Base
02A0 04A0	Q2E8	EDMA Event Q2 Entry 8 / Event Q2 Base
02A0 04A4	Q2E9	EDMA Event Q2 Entry 9 / Event Q2 Base
02A0 04A8	Q2E10	EDMA Event Q2 Entry 10 / Event Q2 Base
02A0 04AC	Q2E11	EDMA Event Q2 Entry 11 / Event Q2 Base
02A0 04B0	Q2E12	EDMA Event Q2 Entry 12 / Event Q2 Base
02A0 04B4	Q2E13	EDMA Event Q2 Entry 13 / Event Q2 Base
02A0 04B8	Q2E14	EDMA Event Q2 Entry 14 / Event Q2 Base
02A0 04BC	Q2E15	EDMA Event Q2 Entry 15 / Event Q2 Base
02A0 04C0 - 02A0 04CC	-	Reserved
02A0 04D0	Q3E0	EDMA Event Q3 Entry 0 / Event Q3 Base
02A0 04D4	Q3E1	EDMA Event Q3 Entry 1 / Event Q3 Base
02A0 04D8	Q3E2	EDMA Event Q3 Entry 2 / Event Q3 Base
02A0 04DC	Q3E3	EDMA Event Q3 Entry 3 / Event Q3 Base
02A0 04E0	Q3E4	EDMA Event Q3 Entry 4 / Event Q3 Base
02A0 04E4	Q3E5	EDMA Event Q3 Entry 5 / Event Q3 Base
02A0 04E8	Q3E6	EDMA Event Q3 Entry 6 / Event Q3 Base
02A0 04EC	Q3E7	EDMA Event Q3 Entry 7 / Event Q3 Base
02A0 04F0	Q3E8	EDMA Event Q3 Entry 8 / Event Q3 Base

Table 6-2. EDMA Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 04F4	Q3E9	EDMA Event Q3 Entry 9 / Event Q3 Base
02A0 04F8	Q3E10	EDMA Event Q3 Entry 10 / Event Q3 Base
02A0 04FC	Q3E11	EDMA Event Q3 Entry 11 / Event Q3 Base
02A0 0500	Q3E12	EDMA Event Q3 Entry 12 / Event Q3 Base
02A0 0504	Q3E13	EDMA Event Q3 Entry 13 / Event Q3 Base
02A0 0508	Q3E14	EDMA Event Q3 Entry 14 / Event Q3 Base
02A0 050C	Q3E15	EDMA Event Q3 Entry 15 / Event Q3 Base
02A0 0510 - 02A0 051C	-	Reserved
02A0 0520 - 02A0 05FC	-	Reserved
02A0 0600	QSTAT0	EDMA Queue 0 Status
02A0 0604	QSTAT1	EDMA Queue 1 Status
02A0 0608	QSTAT2	EDMA Queue 2 Status
02A0 060C	QSTAT3	EDMA Queue 3 Status
02A0 0610 - 02A0 061C	-	Reserved
02A0 0620	QWMTHRA	EDMA Queue Threshold A, for Q[3:0]
02A0 0624	-	Reserved
02A0 0628	QWMCLR	EDMA Queue Watermark Clear Command
02A0 062C - 02A0 063C	-	Reserved
02A0 0640	CCSTAT	CC Status
02A0 0644 - 02A0 06FC	-	Reserved
02A0 0700	-	Reserved
02A0 0704	-	Reserved
02A0 0708	-	Reserved
02A0 070C - 02A0 07FC	-	Reserved
02A0 0800	-	Reserved
02A0 0804	-	Reserved
02A0 0808	-	Reserved
02A0 080C	-	Reserved
02A0 0810	-	Reserved
02A0 0814	-	Reserved
02A0 0818	-	Reserved
02A0 081C	-	Reserved
02A0 0820 - 02A0 0FFC	-	Reserved
02A0 1000	ER (ERL)	EDMA Event Register
02A0 1004	ERH	EDMA Event High Register
02A0 1008	ECR	EDMA Event Clear Register
02A0 100C	ECRH	EDMA Event Clear High Register
02A0 1010	ESR	EDMA Event Set Register
02A0 1014	ESRH	EDMA Event Set High Register
02A0 1018	CER	EDMA Chained Event Register
02A0 101C	CERH	EDMA Chained Event High Register
02A0 1020	EER	EDMA Event Enable Register
02A0 1024	EERH	EDMA Event Enable High Register
02A0 1028	EECR	EDMA Event Enable Clear Register
02A0 102C	EECRH	EDMA Event Enable Clear High Register
02A0 1030	EESR	EDMA Event Enable Set Register
02A0 1034	EESRH	EDMA Event Enable Set High Register

Table 6-2. EDMA Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02A0 1038	SER	EDMA Secondary Event Register
02A0 103C	SERH	EDMA Secondary Event High Register
02A0 1040	SECR	EDMA Secondary Event Clear Register
02A0 1044	SECRH	EDMA Secondary Event Clear High Register
02A0 1048 - 02A0 104C	-	Reserved
02A0 1050	IER	EDMA Interrupt Enable Register
02A0 1054	IERH	EDMA Interrupt Enable High Register
02A0 1058	IECR	EDMA Interrupt Enable Clear Register
02A0 105C	IECRH	EDMA Interrupt Enable Clear High Register
02A0 1060	IESR	EDMA Interrupt Enable Set Register
02A0 1064	IESRH	EDMA Interrupt Enable Set High Register
02A0 1068	IPR	EDMA Interrupt Pending Register
02A0 106C	IPRH	EDMA Interrupt Pending High Register
02A0 1070	ICR	EDMA Interrupt Clear Register
02A0 1074	ICRH	EDMA Interrupt Clear High Register
02A0 1078	IEVAL	EDMA Interrupt Evaluation Register (Set/Eval)
02A0 107C	-	Reserved
02A0 1080	QER	EDMA QDMA Event Register
02A0 1084	QEER	EDMA QDMA Event Enable Register
02A0 1088	QEECR	EDMA QDMA Event Enable Clear Register
02A0 108C	QEESR	EDMA QDMA Event Enable Set Register
02A0 1090	QSER	EDMA QDMA Secondary Event Register
02A0 1094	QSECR	EDMA QDMA Secondary Event Clear Register
02A0 1098 - 02A0 3FFF	-	Reserved
EDMA Parameter (PaRAM)		
02A0 4000		Parameter Set 0
02A0 4020		Parameter Set 1
02A0 4040		Parameter Set 2
02A0 4060		Parameter Set 3
02A0 4080		Parameter Set 4
02A0 40A0		Parameter Set 5
02A0 40C0		Parameter Set 6
02A0 40E0		Parameter Set 7
02A0 4110		Parameter Set 8
02A0 4130		Parameter Set 9
02A0 4150		Parameter Set 10
02A0 4154 - 02A0 5FEC		... Parameter Set 11 thru Parameter Set 254
02A0 5FF0		Parameter Set 255
02A0 5FF4 - 02A0 7FE0	-	Reserved
02A0 7FE4 - 02A0 7FFF	-	Reserved

6.9 Interrupts

6.9.1 Interrupt Sources and Interrupt Selector

The CPU interrupts on the C6455 device are configured through the enhanced interrupt selector. The interrupt controller allows for up to 128 system events to be programmed to any of the twelve CPU interrupt inputs, the CPU exception input, or the advanced emulation logic. Table 6-3 shows the mapping of system events to the interrupt controller inputs. Event numbers 0-31 correspond to the default interrupt mapping of the device. The remaining events must be mapped using software.

Table 6-3. C6455 DSP Interrupts

EVENT NUMBER	INTERRUPT EVENT	INTERRUPT SOURCE
INT_00 ⁽¹⁾	EVT0	Interrupt Controller output of event combiner 0, for events 1 - 31.
INT_01 ⁽¹⁾	EVT1	Interrupt Controller output of event combiner 1, for events 32 - 63.
INT_02 ⁽¹⁾	EVT2	Interrupt Controller output of event combiner 2, for events 64 - 95.
INT_03 ⁽¹⁾	EVT3	Interrupt Controller output of event combiner 3, for events 96 - 127.
INT_04 - INT_08 ⁽²⁾	Reserved	Reserved. Do not use.
INT_09 ⁽²⁾	EMU_DTDMA	EMU interrupt for: 1. Host scan access 2. DTDMA transfer complete 3. AET interrupt
INT_10 ⁽²⁾	Reserved	Reserved. Do not use.
INT_11 ⁽²⁾	EMU_RTDXRX	EMU real-time data exchange (RTDX) receive complete
INT_12 ⁽²⁾	EMU_RTDXTX	EMU RTDX transmit complete
INT_13 ⁽²⁾	IDMA0	IDMA channel 0 interrupt
INT_14 ⁽²⁾	IDMA1	IDMA channel 1 interrupt
INT_15 ⁽²⁾	HINT	HPI/PCI host interrupt
INT_16	I2CINT	I2C interrupt
INT_17	MACINT	Ethernet MAC interrupt
INT_18	AEASYNCERR	EMIFA error interrupt
INT_19	Reserved	Reserved. Do not use.
INT_20	RIOINT0	RapidIO interrupt 0
INT_21	RIOINT1	RapidIO interrupt 1
INT_22	RIOERR	RapidIO error
INT_23	Reserved	Reserved. Do not use.
INT_24	CC_GINT	EDMA3 channel global completion interrupt
INT_25 - INT_29	Reserved	Reserved. Do not use.
INT_30	L2PDWAKE0	L2 wakeup interrupt 0
INT_31	L2PDWAKE1	L2 wakeup interrupt 1
INT_32	VCP2_INT	VCP2 error interrupt
INT_33	TCP2_INT	TCP2 error interrupt
INT_34 - INT_35	Reserved	Reserved. Do not use.
INT_36	UINT	UTOPIA interrupt
INT_37 - INT_39	Reserved	Reserved. Do not use.
INT_40	RINT0	McBSP0 receive interrupt
INT_41	XINT0	McBSP0 transmit interrupt
INT_42	RINT1	McBSP1 receive interrupt
INT_43	XINT1	McBSP1 transmit interrupt

(1) Interrupts INT_00 through INT_03 are non-maskable and fixed.

(2) Interrupts INT_04 through INT_15 are programmable by modifying the binary selector values in the Interrupt Selector Control registers fields. Table 6-3 shows the default interrupt sources for Interrupts INT_04 through INT_15. For more detailed information on interrupt sources and selection, see the *TMS320C6000 DSP Interrupt Selector Reference Guide* (literature number SPRU646).

Table 6-3. C6455 DSP Interrupts (continued)

EVENT NUMBER	INTERRUPT EVENT	INTERRUPT SOURCE
INT_44 - INT_49	Reserved	Reserved. Do not use.
INT_50	Reserved	Reserved. Do not use.
INT_51	GPINT0	GPIO interrupt
INT_52	GPINT1	GPIO interrupt
INT_53	GPINT2	GPIO interrupt
INT_54	GPINT3	GPIO interrupt
INT_55	GPINT4	GPIO interrupt
INT_56	GPINT5	GPIO interrupt
INT_57	GPINT6	GPIO interrupt
INT_58	GPINT7	GPIO interrupt
INT_59	GPINT8	GPIO interrupt
INT_60	GPINT9	GPIO interrupt
INT_61	GPINT10	GPIO interrupt
INT_62	GPINT11	GPIO interrupt
INT_63	GPINT12	GPIO interrupt
INT_64	GPINT13	GPIO interrupt
INT_65	GPINT14	GPIO interrupt
INT_66	GPINT15	GPIO interrupt
INT_67	TINT0L	Timer 0 interrupt low
INT_68	TINT0H	Timer 0 interrupt high
INT_69	TINT1L	Timer 1 interrupt low
INT_70	TINT1H	Timer 1 interrupt high
INT_71	CC_INT0	CC completion interrupt - Mask0
INT_72	CC_INT1	CC completion interrupt - Mask1
INT_73	CC_INT2	CC completion interrupt - Mask2
INT_74	CC_INT3	CC completion interrupt - Mask3
INT_75	CC_INT4	CC completion interrupt - Mask4
INT_76	CC_INT5	CC completion interrupt - Mask5
INT_77	CC_INT6	CC completion interrupt - Mask6
INT_78	CC_INT7	CC completion interrupt - Mask7
INT_79	CC_ERRINT	CC error interrupt
INT_80	CC_MPINT	CC memory protection interrupt
INT_81	TC_ERRINT0	TC0 error interrupt
INT_82	TC_ERRINT1	TC1 error interrupt
INT_83	TC_ERRINT2	TC2 error interrupt
INT_84	TC_ERRINT3	TC3 error interrupt
INT_85	CC_AET EVT	CC AET event
INT_86 - INT_95	Reserved	Reserved. Do not use.
INT_96	INTERR	Interrupt Controller dropped CPU interrupt event
INT_97	EMC_IDMAERR	EMC invalid IDMA parameters
INT_98	Reserved	Reserved. Do not use.
INT_99	Reserved	Reserved. Do not use.
INT_100	EFIINTA	EFI interrupt from side A
INT_101	EFIINTB	EFI interrupt from side B
INT_102 - INT_111	Reserved	Reserved. Do not use.
INT_112	Reserved	Reserved. Do not use.
INT_113	L1P_ED1	L1P single bit error detected during DMA read

Table 6-3. C6455 DSP Interrupts (continued)

EVENT NUMBER	INTERRUPT EVENT	INTERRUPT SOURCE
INT_114 - INT_115	Reserved	Reserved. Do not use.
INT_116	L2_ED1	L2 single bit error detected
INT_117	L2_ED2	L2 two bit error detected
INT_118	PDC_INT	Powerdown sleep interrupt
INT_119	Reserved	Reserved. Do not use.
INT_120	L1P_CMPA	L1P CPU memory protection fault
INT_121	L1P_DMPA	L1P DMA memory protection fault
INT_122	L1D_CMPA	L1D CPU memory protection fault
INT_123	L1D_DMPA	L1D DMA memory protection fault
INT_124	L2_CMPA	L2 CPU memory protection fault
INT_125	L2_DMPA	L2 DMA memory protection fault
INT_126	IDMA_CMPA	IDMA CPU memory protection fault
INT_127	IDMA_BUSERR	IDMA bus error interrupt

6.9.2 Interrupts Peripheral Register Description(s)

6.9.3 Interrupts Electrical Data/Timing

6.10 Reset

The C6455 device has several types of resets – Power-on Reset, Warm Reset, Max Reset, System Reset, and CPU Reset. Table 6-4 explains further the types of reset, the reset initiator, and the effects on the chip.

Table 6-4. Reset Types

TYPE	INITIATOR	EFFECT(s)
$\overline{\text{POR}}$ (power-on-reset)	Hardware circuit detects power on condition. $\overline{\text{POR}}$ pin active low.	Resets the entire chip including reset of the test/emulation logic. Total reset of chip (cold reset). Activates the POR signal on-chip.
Warm Reset	$\overline{\text{RESET}}$ pin active low	Resets everything except for test/emulation logic. Emulator stays alive during Warm Reset.
Max Reset	RapidIO Emulator	Same as a Warm Reset.
System Reset	Emulator	Soft Reset. A soft reset maintains memory contents and does not affect or reset the Device Configuration pins, the PLL1 and PLL2 peripherals, the PLL1 Controller, the PowerSaver module, or the Test/Emulation circuitry.
CPU Reset	HPI	Resets the CPU.

6.10.1 Power-on Reset ($\overline{\text{POR}}$ Pin)

Note: The reset ($\overline{\text{RESET}}$) pin **must** be held inactive (High) throughout the Power-On Reset.

1. During Power up, the power-on reset ($\overline{\text{POR}}$) pin **must** be low [active].
2. Once the power supplies are within valid operating conditions, the $\overline{\text{POR}}$ pin **must** be held low for a minimum of 256 CLKIN1 cycles before being pulled high. Within the minimum 256 CLKIN1 cycles, the following happens:

- a. The reset signals flow to the entire chip (including the test and emulation logic), resetting anything that uses reset asynchronously, and sends a Hi-z signal to all the I/O pads to prevent off-chip contention.
- b. The clocks are reset and are propagated throughout the chip to reset any logic that was using reset synchronously.

The $\overline{\text{RESETSTAT}}$ pin is active (low), indicating the device is in reset.

3. When the $\overline{\text{POR}}$ pin is released (driven inactive high), the configuration pin values are latched and device initialization begins.
4. After device initialization is complete, all system clocks are paused for 8 CLKIN1 cycles and then restarted.
5. The device is now out of reset, the $\overline{\text{RESETSTAT}}$ pin goes inactive (high), and the device execution begins.

6.10.2 Warm Reset

Note: The power-on reset ($\overline{\text{POR}}$) pin **must** be held inactive (high) throughout the Warm Reset.

1. During Power up, a Warm Reset is activated by pulling the reset ($\overline{\text{RESET}}$) pin low [active].
2. Once the power supplies are within valid operating conditions, the $\overline{\text{RESET}}$ pin **must** be held low for a minimum of 24 CLKIN1 cycles before being pulled high. Within the minimum 24 CLKIN1 cycles, the following happens:
 - a. The reset signals flow to the entire chip (excluding the PLL2 module and the test and emulation logic), resetting anything that uses reset asynchronously, and sends a Hi-z signal to all the I/O pads to prevent off-chip contention.
 - b. The clocks are reset and are propagated throughout the chip to reset any logic that was using reset synchronously.

The $\overline{\text{RESETSTAT}}$ pin is active (low), indicating the device is in reset.

3. When the $\overline{\text{RESET}}$ pin is released (driven inactive high), the configuration pin values are latched and device initialization begins.
4. After device initialization is complete, all system clocks are paused for 8 CLKIN1 cycles and then restarted.
5. The device is now out of reset, the $\overline{\text{RESETSTAT}}$ pin goes inactive (high), and the device execution begins.

6.10.3 Max Reset

A Max Reset is initiated by the RapidIO peripheral or by the emulator and has the same affect as a Warm Reset.

6.10.4 System Reset

A System Reset is initiated by the emulator. The System Reset is considered a "soft reset" — meaning the internal memory contents are maintained and neither the clock logic or the power control logic are affected.

A System (Soft) Reset does **not** reset the PLL1 and PLL2 peripherals, the PLL1 Controller, and the Powersaver modules or the Test/Emulation circuitry.

6.10.5 CPU Reset

A CPU Reset is initiated by the HPI peripheral. This reset *only* affects the CPU.

6.10.6 *Reset Electrical Data/Timing*

PRODUCT PREVIEW

6.11 Clock PLL1 and PLL1 Controller

6.11.1 PLL1 and PLL1 Controller Device-Specific Information

The C6455 device includes a PLL1 and a software programmable PLL1 Controller. The PLL1 controller is able to generate different clocks for different parts of the system (i.e., Megamodule, DSP core, Peripheral Data Bus, EMIFA, and other peripherals). [Figure 6-2](#) illustrates the PLL1, the PLL1 controller, and the clock generator logic.

There is no hardware CLKMODE selection on the C6455 device. The PLL multiply factor is set in software after reset.

PLL1 Controller Registers - PLLCSR, PLLM, PLLDIV0, PLLDIV1, PLLDIV2, PLLDIV3, OSCDIV1, WAKEUP, and CK3SEL - **TBD**

PLL1 external components - **TBD**

NOTE: SYSCLK3 is one of the outputs from the PLL1 Controller. Also a dedicated output for EMIFA and DDR2 EMIF - **TBD**

only multiplier and one divider are software controllable

SYSREFCLK:

C64x+ MegaModule

DIVIDER1: SYSCLK1 (/3; Fixed) all module clocks

EDMA

Chip infrastructure

CFG

Peripherals — VCP2, TCP2, EMIFA, DDR2 EMIF, and RapidIO

DIVIDER2: SYSCLK2 (/6; Fixed) module clocks [vs. driving clocks on pins like SYSCLK3 for EMIFA]

PCI

EMAC/MDIO

HPI

UTOPIA

McBSP

GPIO

TIMERS (2)

I2C

PLL1

Controller

Powersaver

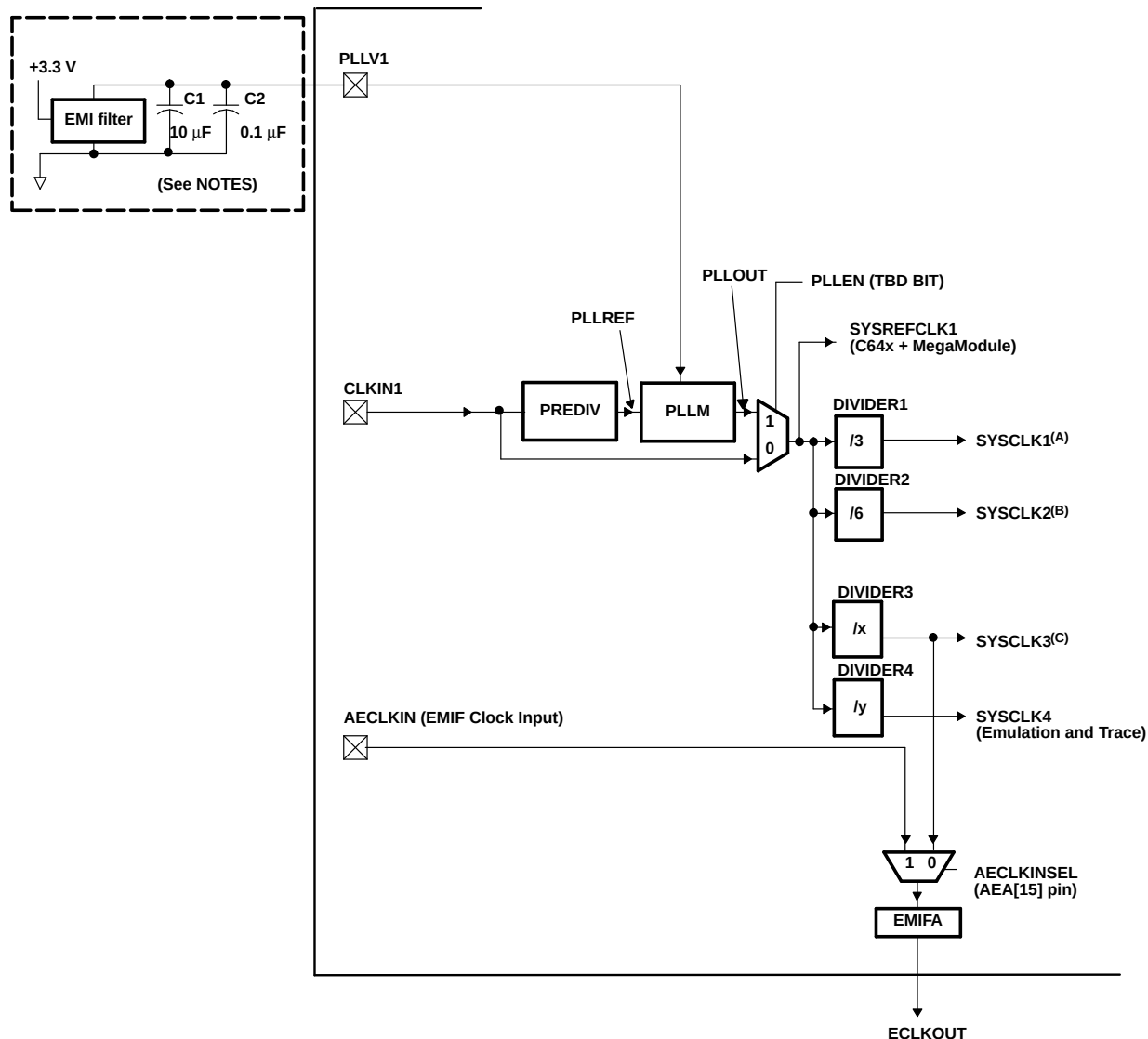
DIVIDER3: SYSCLK3 (/8; default) input clock source (I/O)

EMIFA

DIVIDER4: SYSCLK4 (/8) input clock source (I/O)

Emulation

Trace



- A. EDMA, Chip infrastructure, CFG, and VCP2, TCP2, EMIFA, DDR2 EMIF, and RapidIO Peripherals
- B. PCI, EMAC/MDIO, HPI, UTOPIA, McBSP, GPIO, TIMER, I2C, PLL1 Controller, and Powersaver
- C. EMIFA

(For the PLL Options, CLKMODE Pins Setup, and PLL Clock Frequency Ranges, see the “TMS320C6455 PLL Multiply Factor Options, Clock Frequency Ranges, and Typical Lock Time” table.)

NOTES: Place all PLL external components (C1, C2, and the EMI Filter) as close to the C6000™ DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.

For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (C1, C2, and the EMI Filter).

The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, V_{DD} .

EMI filter manufacturer Murata part number ACF451832-333, -223, -153, -103. Panasonic part number EXCCET193U.

Figure 6-2. External PLL1 Circuitry for Either PLL1 Multiply Modes or x1 (Bypass) Mode

PRODUCT PREVIEW

6.11.2 PLL1 Controller Peripheral Register Description(s)**Table 6-5. PLL1 Controller**

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
029A 0000	PLLPID	Peripheral identification register [value: 0x0001 0802]
029A 0004	-	Reserved
029A 0008	-	Reserved
029A 000C	-	Reserved
029A 0010	-	Reserved
029A 0014	-	Reserved
029A 0018 - 029A 00DC	-	Reserved
029A 00E0	FUSERR	Fusefarm error register
029A 00E4	RSTYPE	Reset type status register
029A 00E8	-	Reserved
029A 00EC	-	Reserved
029A 00F0	-	Reserved
029A 00F4	-	Reserved
029A 00F8	-	Reserved
029A 00FC	-	Reserved
029A 0100	-	Reserved
029A 0104	-	Reserved
029A 0108	-	Reserved
029A 010C	-	Reserved
029A 0110	PLLM	PLL multiplier control register
029A 0114	PREDIV	PLL pre-divider control register
029A 0118	-	Reserved
029A 011C	-	Reserved
029A 0120	PLLDIV3	PLL controller divider 3 register
029A 0124	-	Reserved
029A 0128	-	Reserved
029A 012C	-	Reserved
029A 0130	-	Reserved
029A 0134	-	Reserved
029A 0138	PLLCMD	PLL controller command register
029A 013C	PLLSTAT	PLL controller status register
029A 0140	-	Reserved
029A 0144	DCHANGE	PLLDIV ratio change status register
029A 0148	-	Reserved
029A 014C	-	Reserved
029A 0150	SYSTAT	SYSCLK status register
029A 0154	-	Reserved
029A 0158	-	Reserved
029A 015C	-	Reserved
029A 0160	PLLDIV4	PLL controller divider 4 register
029A 0164	-	Reserved
029A 0168	-	Reserved
029A 016C	-	Reserved

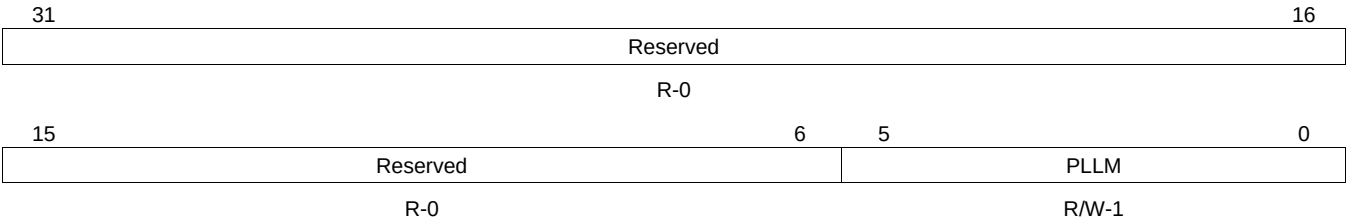
Table 6-5. PLL1 Controller (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
029A 0170	-	Reserved
029A 0174 - 029A 01EF	-	Reserved
029A 01F0 - 029A 01FF	-	Reserved
029A 0200 - 029B FFFF	-	Reserved

6.11.3 PLL1 Electrical Data/Timing

6.12 PLL1 Controller Registers

PLLPID
FUSERR
RSTYPE
PLLM



LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Figure 6-3. PLL1 Multiply Control Register (PLLM) [Hex Address: 029A 0110]

Table 6-6. PLL1 Multiply Control Register (PLLM) Field Descriptions

Bit	Field	Value	Description
31:6	Reserved	-	Reserved. Read-only, writes have no effect.

Table 6-6. PLL1 Multiply Control Register (PLLM) Field Descriptions (continued)

Bit	Field	Value	Description
5:0	PLLM		PLL1 Multiplier Select Bits Defines the frequency multiplier of the input reference clock in conjunction with the TBD. Note: The C6455 device <i>only</i> supports the x1 (BYPASS), x20, x25, x30 and x32 multiply options. 00000 x1 (BYPASS) 00001 x2 (Reserved) 00010 x3 (Reserved) 00011 x4 (Reserved) 00100 x5 (Reserved) 00101 x6 (Reserved) 00110 x7 (Reserved) 00111 x8 (Reserved) 01000 x9 (Reserved) 01001 x10 (Reserved) 01010 x11 (Reserved) 01011 x12 (Reserved) 01100 x13 (Reserved) 01101 x14 (Reserved) 01110 x15 (Reserved) 01111 x16 (Reserved) 10000 x17 (Reserved) 10001 x18 (Reserved) 10010 x19 (Reserved) 10011 x20 10100 x21 (Reserved) 10101 x22 (Reserved) 10110 x23 (Reserved) 10111 x24 (Reserved) 11000 x25 11001 x26 (Reserved) 11010 x27 (Reserved) 11011 x28 (Reserved) 11100 x29 (Reserved) 11101 x30 11110 x31 (Reserved) 11111 x32 PLLM select values 00001 through 01110, 10100 through 10111, 11101 through 11100, and 11110 are <i>not</i> supported.

PREDIV

PLLDIV1 and PLLDIV2 - have fixed values PLLDIV3, PLLDIV4 - PLL1 Controller Divider n Registers for SYSCLKn (PLLDIVn)

These registers control the value of the divider Dn for SYSCLKn. Each divider divides down SYSREFCLK1 (SYSCLK reference clock from either the BYPASS or PLL1 path).

PLLCMD

The PLL1 Controller Command Register contains the command bits for various PLLCTRL operations. The register bits always read back what was previously written. These bits are not self-modified by the PLLCTRL except through a reset where the bits are returned to default. The status of the command register can be viewed in the PLLSTAT register.

PLLSTAT

The fields in this register show the PLL1 Controller status (status of the PLLCMD register). TBD

DCHANGE

SYSTAT

6.13 Clock PLL2

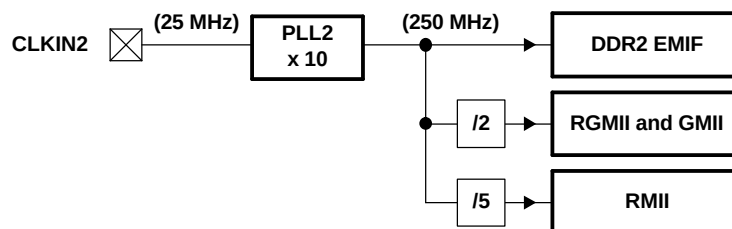


Figure 6-4. PLL2 Block Diagram

6.14 DDR2 EMIF

The 32-bit DDR2 EMIF (500 MHz data rate) is designed to operate with sustained throughput at the memory's data rate (up to 2.0 Gbps) as long as data requests are pending from the DDR2 EMIF.

6.14.1 DDR2 EMIF Device-Specific Information

6.14.2 DDR2 EMIF Peripheral Register Description(s)

Table 6-7. DDR2 EMIF Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
7800 0000	-	Reserved
7800 0004	SDSTS	DDR2 EMIF SDRAM Status Register
7800 0008	SDCFG	DDR2 EMIF SDRAM Configuration Register
7800 000C	SDCTL	DDR2 EMIF SDRAM Refresh Control Register
7800 0010	SDTIM	DDR2 EMIF SDRAM Timing Register
7800 0014 - 7800 004C	-	Reserved
7800 0050 - 7800 0078	-	Reserved
7800 007C - 7800 00BC	-	Reserved
7800 00C0 - 7800 00E0	-	Reserved
7800 00E4	DDRCTL	DDR2 EMIF PHY Control Register
7800 00E8	DDRSTS	DDR2 EMIF PHY Status Register
7800 00EC - 7800 00FC	-	Reserved
7800 0100 - 7FFF FFFF	-	Reserved

6.14.3 DDR2 EMIF Device-Specific Information

DDR2 EMIF Device Speed

TBD

6.14.4 DDR2 EMIF Electrical Data/Timing

TI only supports board designs that follow the board design guidelines outlined in the *TBD* application report (literature number SPRAATBD).

6.15 EMIFA

EMIFA supports a glueless interface to a variety of external devices or ASICs, including:

- Pipelined Synchronous-Burst SRAM (SBSRAM)
- Asynchronous devices including SRAM and ROM
- An external shared-memory device

6.15.1 EMIFA Device-Specific Information

AC timings verification - TBD

Timing analysis must be done to verify all AC timings are met. TI recommends utilizing I/O buffer information specification (IBIS) to analyze all AC timings.

To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number SPRA839).

To maintain signal integrity, serial termination resistors should be inserted into all EMIF output signal lines (see the Terminal Functions table for the EMIF output signals).

6.15.2 EMIFA Peripheral Register Description(s)

Table 6-8. EMIFA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
7000 0000	-	Reserved
7000 0004	-	Reserved
7000 0008	-	Reserved
7000 000C	-	Reserved
7000 0010	-	Reserved
7000 0014 - 7000 004C	-	Reserved
7000 0050 - 7000 007C	-	Reserved
7000 0080	CESEC2	EMIFA Chip Select 2 Configuration Register
7000 0084	CESEC3	EMIFA Chip Select 3 Configuration Register
7000 0088	CESEC4	EMIFA Chip Select 4 Configuration Register
7000 008C	CESEC5	EMIFA Chip Select 5 Configuration Register
7000 0090 - 7000 009C	-	Reserved
7000 00A0	ASYNCWAITCFG	EMIFA Async Wait Cycle Configuration Register
7000 00A4 - 7000 00BC	-	Reserved
7000 00C0	INTRAW	EMIFA Interrupt RAW Register
7000 00C4	INTMSK	EMIFA Interrupt Masked Register
7000 00C8	INTMSKSET	EMIFA Interrupt Mask Set Register

Table 6-8. EMIFA Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
7000 00CC	INTMSKCLR	EMIFA Interrupt Mask Clear Register
7000 00D0 - 7000 00DC	-	Reserved
7000 00E0 - 77FF FFFF	-	Reserved

6.15.3 EMIFA Electrical Data/Timing

6.16 I2C Peripheral

The inter-integrated circuit (I2C) module provides an interface between a C64x+ DSP and other devices compliant with Philips Semiconductors Inter-IC bus (I²C bus) specification version 2.1 and connected by way of an I²C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DSP through the I2C module.

6.16.1 I2C Device-Specific Information

The C6455 device includes an I2C peripheral module (I2C). NOTE: when using the I2C module, ensure there are external pullup resistors on the SDA and SCL pins.

The I2C modules on the C6455 may be used by the DSP to control local peripherals ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I2C port supports:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to remove noise 50 ns or less
- 7- and 10-Bit Device Addressing Modes
- Multi-Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- Slew-Rate Limited Open-Drain Output Buffers

[Figure 6-5](#) is a block diagram of the I2C module.

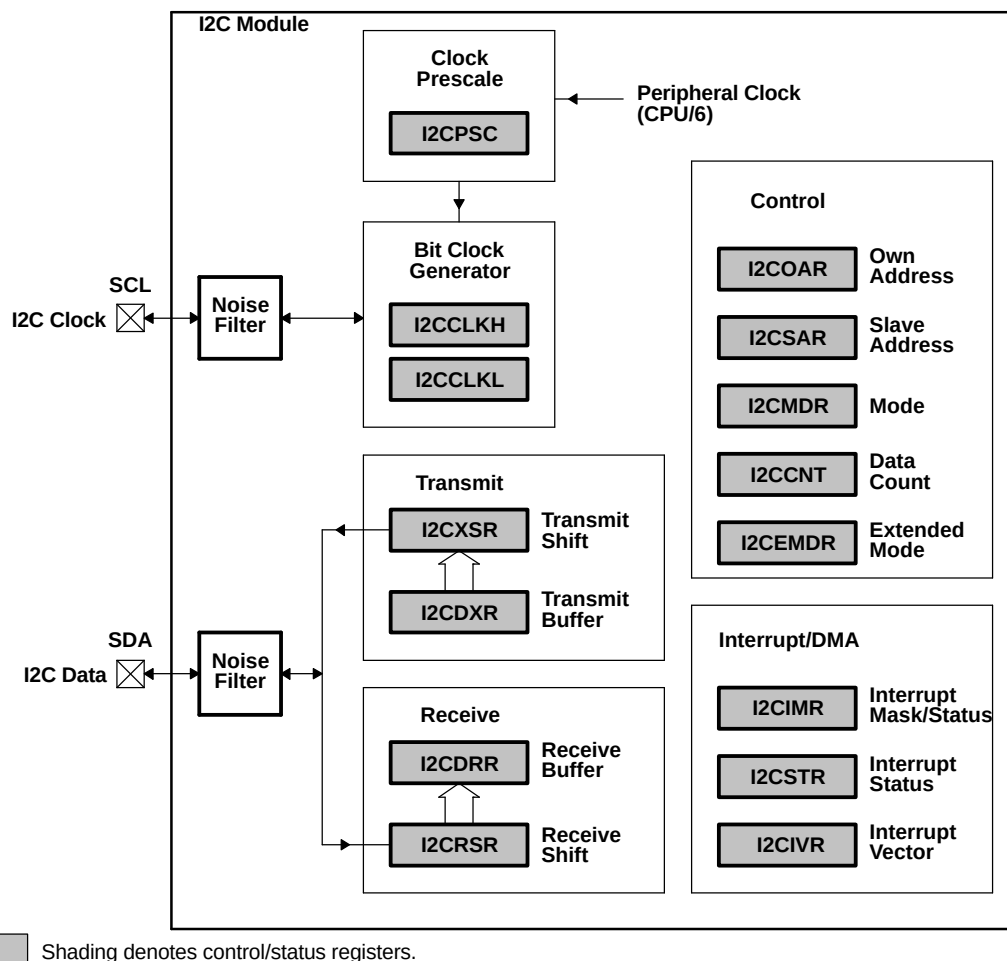


Figure 6-5. I2C Module Block Diagram

6.16.2 I2C Peripheral Register Description(s)

Table 6-9. I2C Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02B0 4000	I2COAR	I2C own address register
02B0 4004	I2CIMR	I2C interrupt mask/status register
02B0 4008	I2CSTR	I2C interrupt status register
02B0 400C	I2CCLKL	I2C clock low-time divider register
02B0 4010	I2CCLKH	I2C clock high-time divider register
02B0 4014	I2CCNT	I2C data count register
02B0 4018	I2CDRR	I2C data receive register
02B0 401C	I2CSAR	I2C slave address register
02B0 4020	I2CDXR	I2C data transmit register
02B0 4024	I2CMDR	I2C mode register
02B0 4028	I2CIVR	I2C interrupt vector register
02B0 402C	I2CEMDR	I2C Extended mode register
02B0 4030	I2CPSC	I2C prescaler register

Table 6-9. I2C Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02B0 4034	I2CPID1	I2C Peripheral Identification register 1 [Value: 0x0000 0105]
02B0 4038	I2CPID2	I2C Peripheral Identification register 2 [Value: 0x0000 0005]
02B0 403C - 02B0 405C	-	Reserved
02B0 4060 - 02B3 407F	-	Reserved
02B0 4080 - 02B3 FFFF	-	Reserved

6.16.3 I2C Electrical Data/Timing

6.17 Host-Port Interface (HPI) Peripheral

The C6455 device includes a user-configurable 16-bit or 32-bit Host-port interface (HPI16/HPI32).

The AEA14 pin controls the HPI_WIDTH, allowing the user to configure the HPI as a 16-bit or 32-bit peripheral.

The C6455 device uses the HPI data pins for peripheral configuration and bootmode set up. For more details on HPI peripheral configuration and the associated pins, see the Device Configurations section of this data sheet.

6.17.1 HPI Device-Specific Information

6.17.2 HPI Peripheral Register Description(s)

Table 6-10. HPI Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0288 0000	PID	Host port interface (HPI) data register [value: 0xTBD]	Host read/write access only
0288 0004	PWREMU_MGMT	HPI power and emulation management register	PWREMU_MGMT has both Host/CPU read/write access
0288 0008 - 0288 0024	-	Reserved	
0288 0028	-	Reserved	
0288 002C	-	Reserved	
0288 0030	HPIC	HPI control register	HPIC has both Host/CPU read/write access
0288 0034	HPIA (HPIAW) ⁽¹⁾	HPI address register (Write)	HPIA has both Host/CPU read/write access
0288 0008	HPIA (HPIAR) ⁽¹⁾	HPI address register (Read)	
0288 000C - 028B 007F	-	Reserved	
0288 0080 - 028B FFFF	-	Reserved	

- (1) Host access to the HPIA register updates both the HPIAW and HPIAR registers. The CPU can access HPIAW and HPIAR independently. Host access to the XHPIA register also updates both the XHPIAW and XHPIAR register. The CPU can access XHPIAW and XHPIAR independently.

6.17.3 HPI Electrical Data/Timing

6.18 Multichannel Buffered Serial Port (McBSP)

6.18.1 McBSP Device-Specific Information

6.18.1.1 McBSP Peripheral Register Description(s)

Table 6-11. McBSP 0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
028C 0000	DRR0	McBSP0 data receive register via Configuration Bus	The CPU and EDMA controller can only read this register; they cannot write to it.
3000 0000	DRR0	McBSP0 data receive register via EDMA Bus	
028C 0004	DXR0	McBSP0 data transmit register via Configuration Bus	
3000 0010	DXR0	McBSP0 data transmit register via EDMA Bus	
028C 0008	SPCR0	McBSP0 serial port control register	
028C 000C	RCR0	McBSP0 receive control register	
028C 0010	XCR0	McBSP0 transmit control register	
028C 0014	SRGR0	McBSP0 sample rate generator register	
028C 0018	MCR0	McBSP0 multichannel control register	
028C 001C	RCERE00	McBSP0 enhanced receive channel enable register 0	
028C 0020	XCERE00	McBSP0 enhanced transmit channel enable register 0	
028C 0024	PCR0	McBSP0 pin control register	
028C 0028	RCERE10	McBSP0 enhanced receive channel enable register 1	
028C 002C	XCERE10	McBSP0 enhanced transmit channel enable register 1	
028C 0030	RCERE20	McBSP0 enhanced receive channel enable register 2	
028C 0034	XCERE20	McBSP0 enhanced transmit channel enable register 2	
028C 0038	RCERE30	McBSP0 enhanced receive channel enable register 3	
028C 003C	XCERE30	McBSP0 enhanced transmit channel enable register 3	
028C 0040 - 028F FFFF	-	Reserved	

Table 6-12. McBSP 1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0290 0000	DRR1	McBSP1 data receive register via Configuration Bus	The CPU and EDMA controller can only read this register; they cannot write to it.
3400 0000	DRR1	McBSP1 data receive register via EDMA bus	
0290 0004	DXR1	McBSP1 data transmit register via configuration bus	
3400 0010	DXR1	McBSP1 data transmit register via EDMA bus	
0290 0008	SPCR1	McBSP1 serial port control register	
0290 000C	RCR1	McBSP1 receive control register	
0290 0010	XCR1	McBSP1 transmit control register	
0290 0014	SRGR1	McBSP1 sample rate generator register	

Table 6-12. McBSP 1 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0290 0018	MCR1	McBSP1 multichannel control register	
0290 001C	RCERE01	McBSP1 enhanced receive channel enable register 0	
0290 0020	XCERE01	McBSP1 enhanced transmit channel enable register 0	
0290 0024	PCR1	McBSP1 pin control register	
0290 0028	RCERE11	McBSP1 enhanced receive channel enable register 1	
0290 002C	XCERE11	McBSP1 enhanced transmit channel enable register 1	
0290 0030	RCERE21	McBSP1 enhanced receive channel enable register 2	
0290 0034	XCERE21	McBSP1 enhanced transmit channel enable register 2	
0290 0038	RCERE31	McBSP1 enhanced receive channel enable register 3	
0290 003C	XCERE31	McBSP1 enhanced transmit channel enable register 3	
0290 0040 - 0293 FFFF	-	Reserved	

6.18.2 McBSP Electrical Data/Timing

6.19 Ethernet MAC (EMAC)

The EMAC controls the flow of packet data from the DSP to the PHY.

6.19.1 EMAC Device-Specific Information

The ethernet media access controller (EMAC) provides an efficient interface between the C6455 DSP core processor and the network. The C6455 EMAC supports 10Base-T, 100Base-TX, 1000Base-TX or 10 Mbits/second (Mbps) in either half- or full-duplex, 100 Mbps in either half- or full-duplex, 1000 Mbps in full-duplex, with hardware flow control and quality of service (QOS) support. The C6455 EMAC makes use of a custom interface to the DSP core that allows efficient data transmission and reception. For more details on the EMAC, see the *TBD Module Reference Guide* (literature number SPRUTBD).

The Ethernet MAC (EMAC) peripheral consists of several components:

- CP-GMAC Gigabit Ethernet MAC module, supporting 10/100/1000 Mbit. Natively supports and GMII interfaces.
- MDIO: Management-data input/output module
- RGMII: (G)MII to R(G)MII gasket
- EMAC wrapper: Wrapper of bridge CP-GMAC and MDIO to the chip (CFG and DMA)

The RGMII gasket is a module that converts the full-point MII/GMII interface supported natively by the CP-GPMAC to the reduced pinout RMII/RGMII interfaces. All four flavors must be available at the chip-level, though all are mutually exclusive and some are shared with other device pins. The RGMII is a 2.5-V interface, so it **must** have dedicated package pins (i.e., DV_{DD25}). The MII/GMII/RGMII interfaces are all 3.3 V, and are multiplexed with the UTOPIA interface pins.

6.19.2 EMAC Peripheral Register Description(s)

Table 6-13. Ethernet MAC (EMAC) Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 0000	TXIDVER	Transmit Identification and Version Register
02C8 0004	TXCONTROL	Transmit Control Register
02C8 0008	TXTEARDOWN	Transmit Teardown Register
02C8 000F	-	Reserved
02C8 0010	RXIDVER	Receive Identification and Version Register
02C8 0014	RXCONTROL	Receive Control Register
02C8 0018	RXTEARDOWN	Receive Teardown Register
02C8 001C	-	Reserved
02C8 0020 - 02C8 007C	-	Reserved
02C8 0180	TXINTSTATRAW	Transmit Interrupt Status (Unmasked) Register
02C8 0184	TXINTSTATMASKED	Transmit Interrupt Status (Masked) Register
02C8 0188	TXINTMASKSET	Transmit Interrupt Mask Set Register
02C8 018C	TXINTMASKCLEAR	Transmit Interrupt Mask Clear Register
02C8 0190	MACINVECTOR	MAC Input Vector Register
02C8 0194 - 02C8 019C	-	Reserved
02C8 01A0	RXINTSTATRAW	Receive Interrupt Status (Unmasked) Register
01C8 01A4	RXINTSTATMASKED	Receive Interrupt Status (Masked) Register
01C8 01A8	RXINTMASKSET	Receive Interrupt Mask Set Register
01C8 01AC	RXINTMASKCLEAR	Receive Interrupt Mask Clear Register
01C8 01B0	MACINTSTATRAW	MAC Interrupt Status (Unmasked) Register
01C8 01B4	MACINTSTATMASKED	MAC Interrupt Status (Masked) Register
01C8 01B8	MACINTMASKSET	MAC Interrupt Mask Set Register
01C8 01BC	MACINTMASKCLEAR	MAC Interrupt Mask Clear Register
02C8 00C0 - 02C8 00FC	-	Reserved
02C8 0100	RXMBPENABLE	Receive Multicast/Broadcast/Promiscuous Channel Enable Register
02C8 0104	RXUNICASTSET	Receive Unicast Set Register
02C8 0108	RXUNICASTCLEAR	Receive Unicast Clear Register
02C8 010C	RXMAXLEN	Receive Maximum Length Register
02C8 0110	RXBUFFEROFFSET	Receive Buffer Offset Register
02C8 0114	RXFILTERLOWTHRESH	Receive Filter Low Priority Packets Threshold Register
02C8 0118 - 02C8 011C	-	Reserved
02C8 0120	RX0FLOWTHRESH	Receive Channel 0 Flow Control Threshold Register
02C8 0124	RX1FLOWTHRESH	Receive Channel 1 Flow Control Threshold Register
02C8 0128	RX2FLOWTHRESH	Receive Channel 2 Flow Control Threshold Register
02C8 012C	RX3FLOWTHRESH	Receive Channel 3 Flow Control Threshold Register
02C8 0130	RX4FLOWTHRESH	Receive Channel 4 Flow Control Threshold Register
02C8 0134	RX5FLOWTHRESH	Receive Channel 5 Flow Control Threshold Register
02C8 0138	RX6FLOWTHRESH	Receive Channel 6 Flow Control Threshold Register
02C8 013C	RX7FLOWTHRESH	Receive Channel 7 Flow Control Threshold Register
02C8 0140	RX0FREEBUFFER	Receive Channel 0 Free Buffer Count Register
02C8 0144	RX1FREEBUFFER	Receive Channel 1 Free Buffer Count Register
02C8 0148	RX2FREEBUFFER	Receive Channel 2 Free Buffer Count Register
02C8 014C	RX3FREEBUFFER	Receive Channel 3 Free Buffer Count Register
02C8 0150	RX4FREEBUFFER	Receive Channel 4 Free Buffer Count Register
02C8 0154	RX5FREEBUFFER	Receive Channel 5 Free Buffer Count Register
02C8 0158	RX6FREEBUFFER	Receive Channel 6 Free Buffer Count Register

Table 6-13. Ethernet MAC (EMAC) Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 015C	RX7FREEBUFFER	Receive Channel 7 Free Buffer Count Register
02C8 0160	MACCONTROL	MAC Control Register
02C8 0164	MACSTATUS	MAC Status Register
02C8 0168	EMCONTROL	Emulation Control Register
02C8 016C	FIFOCONTROL	Transmit and Received FIFO Control Register
02C8 0170	MACCFIG	MAC Configuration Read Register
02C8 0174	SOFTRESET	Soft Reset Register
02C8 0178 - 02C8 01CC	-	Reserved
02C8 01D0	MACSRCADDRLO	MAC Address Lower 32-bits Register
02C8 01D4	MACSRCADDRHI	MAC Address Upper 32-bits Register
02C8 01D8	MACHASH1	MAC Address Hash Register 1
02C8 01DC	MACHASH2	MAC Address Hash Register 2
02C8 01E0	BOFFTEST	Backoff Test Register
02C8 01E4	TPACETEST	Transmit Pacing Test Register
02C8 01E8	RXPAUSE	Receive Pause Timer Register
02C8 01EC	TXPAUSE	Transmit Pause Timer Register
02C8 01F0 - 02C8 01FC	-	Reserved
02C8 0200 - 02C8 02FC	(see Table 6-14)	EMAC Statistics Registers
02C8 0300 - 02C8 03FC	RXFIFOPROCTESTACCESS	Receive FIFO Processor Test Access Registers Only accessible when the "min" bit in the MACCONTROL register is set (32-bit access only)
02C8 0400 - 02C8 04FC	TXFIFOPROCTESTACCESS	Transmit FIFO Processor Test Access Registers Only accessible when the "memtest" bit in the MACCONTROL register is set (32-bit access only)
02C8 0500 - 02C8 05FC	RXADDMATCHLOG	Receive Address Matching Logic
02C8 0600	TX0HDP	Transmit Channel 0 DMA Head Descriptor Pointer Register
02C8 0604	TX1HDP	Transmit Channel 1 DMA Head Descriptor Pointer Register
02C8 0608	TX2HDP	Transmit Channel 2 DMA Head Descriptor Pointer Register
02C8 060C	TX3HDP	Transmit Channel 3 DMA Head Descriptor Pointer Register
02C8 0610	TX4HDP	Transmit Channel 4 DMA Head Descriptor Pointer Register
02C8 0614	TX5HDP	Transmit Channel 5 DMA Head Descriptor Pointer Register
02C8 0618	TX6HDP	Transmit Channel 6 DMA Head Descriptor Pointer Register
02C8 061C	TX7HDP	Transmit Channel 7 DMA Head Descriptor Pointer Register
02C8 0620	RX0HDP	Receive Channel 0 DMA Head Descriptor Pointer Register
02C8 0624	RX1HDP	Receive Channel 1 DMA Head Descriptor Pointer Register
02C8 0628	RX2HDP	Receive Channel 2 DMA Head Descriptor Pointer Register
02C8 062C	RX3HDP	Receive Channel 3 DMA Head Descriptor Pointer Register
02C8 0630	RX4HDP	Receive Channel 4 DMA Head Descriptor Pointer Register
02C8 0634	RX5HDP	Receive Channel 5 DMA Head Descriptor Pointer Register
02C8 0638	RX6HDP	Receive Channel 6 DMA Head Descriptor Pointer Register
02C8 063C	RX7HDP	Receive Channel 7 DMA Head Descriptor Pointer Register
02C8 0640	TX0INTACK	Transmit Channel 0 Interrupt Acknowledge Register
02C8 0644	TX1INTACK	Transmit Channel 1 Interrupt Acknowledge Register
02C8 0648	TX2INTACK	Transmit Channel 2 Interrupt Acknowledge Register
02C8 064C	TX3INTACK	Transmit Channel 3 Interrupt Acknowledge Register
02C8 0650	TX4INTACK	Transmit Channel 4 Interrupt Acknowledge Register
02C8 0654	TX5INTACK	Transmit Channel 5 Interrupt Acknowledge Register
02C8 0658	TX6INTACK	Transmit Channel 6 Interrupt Acknowledge Register

Table 6-13. Ethernet MAC (EMAC) Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 065C	TX7INTACK	Transmit Channel 7 Interrupt Acknowledge Register
02C8 0660	RX0INTACK	Receive Channel 0 Interrupt Acknowledge Register
02C8 0664	RX1INTACK	Receive Channel 1 Interrupt Acknowledge Register
02C8 0668	RX2INTACK	Receive Channel 2 Interrupt Acknowledge Register
02C8 066C	RX3INTACK	Receive Channel 3 Interrupt Acknowledge Register
02C8 0670	RX4INTACK	Receive Channel 4 Interrupt Acknowledge Register
02C8 0674	RX5INTACK	Receive Channel 5 Interrupt Acknowledge Register
02C8 0678	RX6INTACK	Receive Channel 6 Interrupt Acknowledge Register
02C8 067C	RX7INTACK	Receive Channel 7 Interrupt Acknowledge Register
02C8 0680 - 02C8 06FC	-	Reserved
02C8 0700 - 02C8 077C	-	Reserved was State RAM Test Access Registers Processor Read and Write Access to Head Descriptor Pointers and Interrupt Acknowledge Registers
02C8 0780 - 02C8 0FFF	-	Reserved

Table 6-14. EMAC Statistics Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 0200	RXGOODFRAMES	Good Receive Frames Register
02C8 0204	RXBCASTFRAMES	Broadcast Receive Frames Register
02C8 0208	RXMCASTFRAMES	Multicast Receive Frames Register
02C8 020C	RXPAUSEFRAMES	Pause Receive Frames Register
02C8 0210	RXCRCERRORS	Receive CRC Errors Register
02C8 0214	RXALIGNCODEERRORS	Receive Alignment/Code Errors Register
02C8 0218	RXOVERSIZED	Receive Oversized Frames Register
02C8 021C	RXJABBER	Receive Jabber Frames Register
02C8 0220	RXUNDERSIZED	Receive Undersized Frames Register
02C8 0224	RXFRAGMENTS	Receive Frame Fragments Register
02C8 0228	RXFILTERED	Filtered Receive Frames Register
02C8 022C	RXQOSFILTERED	Receive QOS Filtered Frames Register
02C8 0230	RXOCTETS	Receive Octet Frames Register
02C8 0234	TXGOODFRAMES	Good Transmit Frames Register
02C8 0238	TXBCASTFRAMES	Broadcast Transmit Frames Register
02C8 023C	TXMCASTFRAMES	Multicast Transmit Frames Register
02C8 0240	TXPAUSEFRAMES	Pause Transmit Frames Register
02C8 0244	TXDEFERRED	Deferred Transmit Frames Register
02C8 0248	TXCOLLISION	Collision Register
02C8 024C	TXSINGLECOLL	Single Collision Transmit Frames Register
02C8 0250	TXMULTICOLL	Multiple Collision Transmit Frames Register
02C8 0254	TXEXCESSIVECOLL	Excessive Collisions Register
02C8 0258	TXLATECOLL	Late Collisions Register
02C8 025C	TXUNDERRUN	Transmit Underrun Register
02C8 0260	TXCARRIERSLOSS	Transmit Carrier Sense Errors Register
02C8 0264	TXOCTETS	Transmit Octet Frames Register
02C8 0268	FRAME64	Transmit and Receive 64 Octet Frames Register

Table 6-14. EMAC Statistics Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 026C	FRAME65T127	Transmit and Receive 65 to 127 Octet Frames Register
02C8 0270	FRAME128T255	Transmit and Receive 128 to 255 Octet Frames Register
02C8 0274	FRAME256T511	Transmit and Receive 256 to 511 Octet Frames Register
02C8 0278	FRAME512T1023	Transmit and Receive 512 to 1023 Octet Frames Register
02C8 027C	FRAME1024TUP	Transmit and Receive 1024 or Above Octet Frames Register
02C8 0280	NETOCTETS	Network Octet Frames Register
02C8 0284	RXSOFOVERRUNS	Receive Start of Frame Overruns Register
02C8 0288	RXMOFOVERRUNS	Receive Middle of Frame Overruns Register
02C8 028C	RXDMAOVERRUNS	Receive DMA Overruns Register
02C8 0290 - 02C8 02FC	-	Reserved

Table 6-15. EMAC Wrapper

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 1000 - 02C8 17FF		EMAC Control Module Descriptor Memory
TBD - TBD	-	Reserved

Table 6-16. EMAC CPPI RAM

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 2000 - 02C8 3FFF	TBD	EMAC CPPI RAM

6.19.3 Management Data Input/Output (MDIO)

The MDIO module controls PHY configuration and status monitoring.

6.19.3.1 MDIO Device-Specific Information

The management data input/output (MDIO) module (which is part of the EMAC peripheral) continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system. Once a PHY candidate has been selected by the DSP, the MDIO module transparently monitors its link state by reading the PHY status register. Link change events are stored in the MDIO module and can optionally interrupt the DSP, allowing the DSP to poll the link status of the device without continuously performing costly MDIO accesses. For more details on the MDIO, see the *TBD Module Reference Guide* (literature number SPRUTBD).

6.19.3.2 MDIO Peripheral Register Description(s)

Table 6-17. MDIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 1800	VERSION	MDIO Version Register
02C8 1804	CONTROL	MDIO Control Register

Table 6-17. MDIO Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02C8 1808	ALIVE	MDIO PHY Alive Status Register
02C8 180C	LINK	MDIO PHY Link Status Register
02C8 1810	LINKINTRAW	MDIO Link Status Change Interrupt (Unmasked) Register
02C8 1814	LINKINTMASKED	MDIO Link Status Change Interrupt (Masked) Register
02C8 1818 - 02C8 181C	-	Reserved
02C8 1820	USERINTRAW	MDIO User Command Complete Interrupt (Unmasked) Register
02C8 1824	USERINTMASKED	MDIO User Command Complete Interrupt (Masked) Register
02C8 1828	USERINTMASKSET	MDIO User Command Complete Interrupt Mask Set Register
02C8 182C	USERINTMASKCLEAR	MDIO User Command Complete Interrupt Mask Clear Register
02C8 1830 - 02C8 187C	-	Reserved
02C8 1880	USERACCESS0	MDIO User Access Register 0
02C8 1884	USERPHYSEL0	MDIO User PHY Select Register 0
02C8 1888	USERACCESS1	MDIO User Access Register 1
02C8 188C	USERPHYSEL1	MDIO User PHY Select Register 1
02C8 1890 - 02C8 1FFF	-	Reserved

6.19.3.3 MDIO Electrical Data/Timing

6.20 Timers

The timers can be used to: time events, count events, generate pulses, interrupt the CPU, and send synchronization events to the EDMA.

6.20.1 Timers Device-Specific Information

The C6455 device has a total of two 64-bit general-purpose timers (Timer0 and Timer1), that are configurable as four 32-bit general-purpose timers.

6.20.2 Timers Peripheral Register Description(s)

Table 6-18. Timer 0 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0294 0000	PID12	Timer 0 peripheral identification register [value: 0xTBD]	
0294 0004	EMUMGT_CLK SPD	Timer 0 emulation management/clock speed register	
0294 0008	-	Reserved	
0294 000C	-	Reserved	
0294 0010	TIM12	Timer 0 counter register 12	
0294 0014	TIM34	Timer 0 counter register 34	
0294 0018	PRD12	Timer 0 period register 12	
0294 001C	PRD34	Timer 0 period register 34	
0294 0020	TCR	Timer 0 control register	
0294 0024	TGCR	Timer 0 global control register	
0294 0028	WDTCR	Timer 0 watchdog timer control register	
0294 002C	-	Reserved	

Table 6-18. Timer 0 Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0294 0030	-	Reserved	
0294 0034 - 0297 FFFF	-	Reserved	

Table 6-19. Timer 1 Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME	COMMENTS
0298 0000	PID12	Timer 1 peripheral identification register [value: 0xTBD]	
0298 0004	EMUMGT_CLK SPD	Timer 1 emulation management/clock speed register	
0298 0008	-	Reserved	
0298 000C	-	Reserved	
0298 0010	TIM12	Timer 1 counter register 12	
0298 0014	TIM34	Timer 1 counter register 34	
0298 0018	PRD12	Timer 1 period register 12	
0298 001C	PRD34	Timer 1 period register 34	
0298 0020	TCR	Timer 1 control register	
0298 0024	TGCR	Timer 1 global control register	
0298 0028	WDTCR	Timer 1 watchdog timer control register	
0298 002C	-	Reserved	
0298 0030	-	Reserved	
0298 0034 - 0299 FFFF	-	Reserved	

6.20.3 Timers Electrical Data/Timing

6.21 Enhanced Viterbi-Decoder Coprocessor (VCP2)

6.21.1 VCP2 Device-Specific Information

The C6455 device has a high-performance embedded coprocessor [Viterbi-Decoder Coprocessor (VCP2)] that significantly speeds up channel-decoding operations on-chip. The VCP2 operating at CPU clock divided-by-4 can decode over 694 7.95-Kbps adaptive multi-rate (AMR) [K = 9, R = 1/3] voice channels. The VCP2 supports constraint lengths K = 5, 6, 7, 8, and 9, rates R = 3/4, 1/2, 1/3, 1/4, and 1/5, and flexible polynomials, while generating hard decisions or soft decisions. Communications between the VCP2 and the CPU are carried out through the EDMA controller.

The VCP2 supports:

- Unlimited frame sizes
- Code rates 3/4, 1/2, 1/3, 1/4, and 1/5
- Constraint lengths 5, 6, 7, 8, and 9
- Programmable encoder polynomials
- Programmable reliability and convergence lengths
- Hard and soft decoded decisions
- Tail and convergent modes
- Yamamoto logic

- Tail biting logic
- Various input and output FIFO lengths

For more detailed information on the VCP2, see the *TMS320C64x DSP Viterbi-Decoder Coprocessor 2 (VCP2) Reference Guide* (literature number SPRUTBD). And TBD

6.21.2 VCP2 Peripheral Register Description(s)

Table 6-20. VCP2 Registers

EDMA BUS HEX ADDRESS RANGE	CONFIGURATION BUS HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
5800 0000	-	VCPI0	VCP2 input configuration register 0
5800 0004	-	VCPI1	VCP2 input configuration register 1
5800 0008	-	VCPI2	VCP2 input configuration register 2
5800 000C	-	VCPI3	VCP2 input configuration register 3
5800 0010	-	VCPI4	VCP2 input configuration register 4
5800 0014	-	VCPI5	VCP2 input configuration register 5
		-	Reserved
5800 0048	-	VCPOUT0	VCP2 output register 0
5800 004C	-	VCPOUT1	VCP2 output register 1
		-	Reserved
5800 00A0	N/A	VCPWBM	VCP2 branch metrics write register
		-	Reserved
5800 00C0	N/A	VCPRDECS	VCP2 decisions read register
N/A	02B8 0000	VCPPID	VCP2 peripheral identification register [Value: 0xTBD]
N/A	02B8 0018	VCPEXE	VCP2 execution register
N/A	02B8 0020	VCPEND	VCP2 endian register
N/A	02B8 0040	VCPSTAT0	VCP2 status register 0
N/A	02B8 0044	VCPSTAT1	VCP2 status register 1
N/A	02B8 0050	VCPERR	VCP2 error register
		-	Reserved
N/A	02B8 0060	VCPECTL	VCP2 emulation control register
N/A	02B8 0064 - 02B9 FFFF	-	Reserved

6.21.3 VCP2 Electrical Data/Timing

6.22 Enhanced Turbo Decoder Coprocessor (TCP2)

6.22.1 TCP2 Device-Specific Information

The C6455 device has a high-performance embedded coprocessor [Turbo-Decoder Coprocessor (TCP2)] that significantly speeds up channel-decoding operations on-chip. The TCP2 operating at CPU clock divided-by-3 can decode up to fifty 384-Kbps or eight 2-Mbps turbo encoded channels (assuming 6 iterations). The TCP2 implements the max*log-map algorithm and is designed to support all polynomials and rates required by Third-Generation Partnership Projects (3GPP and 3GPP2), with fully programmable frame length and turbo interleaver. Decoding parameters such as the number of iterations and stopping criteria are also programmable. Communications between the TCP2 and the CPU are carried out through the EDMA controller.

The TCP2 supports:

- Parallel concatenated convolutional turbo decoding using the MAP algorithm
- All turbo code rates greater than or equal to 1/5
- 3GPP and CDMA2000 turbo encoder trellis
- 3GPP and CDMA2000 block sizes in standalone mode
- Larger block sizes in shared processing mode
- Both max log MAP and log MAP decoding
- Sliding windows algorithm with variable reliability and prolog lengths
- The prolog reduction algorithm
- Execution of a minimum and maximum number of iterations
- The SNR stopping criteria algorithm
- The CRC stopping criteria algorithm

For more detailed information on the TCP2, see the *TMS320C64x DSP Turbo-Decoder Coprocessor (TCP) Reference Guide* (literature number SPRU534). And TBD

6.22.2 TCP2 Peripheral Register Description(s)

Table 6-21. TCP2 Registers

EDMA BUS HEX ADDRESS RANGE	CONFIGURATION BUS HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
5000 0000	-	TCPIC0	TCP2 input configuration register 0
5000 0004	-	TCPIC1	TCP2 input configuration register 1
5000 0008	-	TCPIC2	TCP2 input configuration register 2
5000 000C	-	TCPIC3	TCP2 input configuration register 3
5000 0010	-	TCPIC4	TCP2 input configuration register 4
5000 0014	-	TCPIC5	TCP2 input configuration register 5
5000 0018	-	TCPIC6	TCP2 input configuration register 6
5000 001C	-	TCPIC7	TCP2 input configuration register 7
5000 0020	-	TCPIC8	TCP2 input configuration register 8
5000 0024	-	TCPIC9	TCP2 input configuration register 9
5000 0028	-	TCPIC10	TCP2 input configuration register 10
5000 002C	-	TCPIC11	TCP2 input configuration register 11
5000 0030	-	TCPIC12	TCP2 input configuration register 12
5000 0034	-	TCPIC13	TCP2 input configuration register 13
5000 0038	-	TCPIC14	TCP2 input configuration register 14
5000 003C	-	TCPIC15	TCP2 input configuration register 15
5000 0040	-	TCPOUTP0	TCP2 output parameters register 0
5000 0044	-	TCPOUTP1	TCP2 output parameters register 1
5000 0048	-	TCPOUTP2	TCP2 output parameters register 2
5001 0000	N/A	TCPSP	TCP2 systematics and parities memory
5003 0000	N/A	TCPEXT0	TCP2 extrinsics memory 0
5006 0000	N/A	TCPAP	TCP2 apriori memory
5008 0000	N/A	TCPINTER	TCP2 interleaver memory
500A 0000	N/A	TCPHD	TCP2 hard decisions memory
	02BA 0000	TCPPID	TCP2 peripheral identification register [Value: 0xTBD]
N/A	02BA 004C	TCPEXE	TCP2 execution register

Table 6-21. TCP2 Registers (continued)

EDMA BUS HEX ADDRESS RANGE	CONFIGURATION BUS HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
N/A	02BA 0050	TCPEND	TCP2 endian register
N/A	02BA 0060	TCPEER	TCP2 error register
N/A	02BA 0068	TCPSTAT	TCP2 status register
N/A	02BA 0070	TCPECTL	TCP2 emulation control register
N/A	02BA 005C - 02BB FFFF	-	Reserved

6.22.3 TCP2 Electrical Data/Timing

6.23 Peripheral Component Interconnect (PCI)

6.23.1 PCI Device-Specific Information

Table 6-22. PCI Peripheral Registers

PCI HOST ACCESS HEX ADDRESS OFFSET	DSP ACCESS HEX ADDRESS RANGE	ACRONYM	PCI HOST ACCESS REGISTER NAME	DSP ACCESS REGISTER NAME
	02C0 0000			Reserved
	02C0 0004			Reserved
	02C0 0008			Reserved
	02C0 000C			Reserved
	02C0 0010			PCIIF Status Set
	02C0 0014			PCIIF Status Clear
	02C0 0018			Reserved
	02C0 001C			Reserved
	02C0 0020			PCIIF Host Interrupt Enable Set
	02C0 0024			PCIIF Host Interrupt Enable Clear
	02C0 0028			Reserved
	02C0 002C			Reserved
	02C0 0030			PCIIF Back End Application Interrupt Enable Set
	02C0 0034			PCIIF Back End Application Interrupt Enable Clear
	02C0 0038			PCIIF Back End Application Clock Management
	02C0 003C - 02C0 007C			Reserved
	02C0 0080 - 02C0 00FC			Reserved
0x00	02C0 0100		Vendor ID/Device ID	PCIIF Vendor ID/Device ID Mirror
0x04	02C0 0104		Command/Status	PCIIF Command/Status Mirror
0x08	02C0 0108		Class Code/Revision ID	PCIIF Class Code/Revision ID Mirror
0x0C	02C0 010C		BIST/Header Type/Latency Timer/Cacheline Size	PCIIF BIST/Header Type/Latency Timer/Cacheline Size Mirror

Table 6-22. PCI Peripheral Registers (continued)

PCI HOST ACCESS HEX ADDRESS OFFSET	DSP ACCESS HEX ADDRESS RANGE	ACRONYM	PCI HOST ACCESS REGISTER NAME	DSP ACCESS REGISTER NAME
0x10	02C0 0110		Base Address 0	PCIIF Base Address 0 Mask
0x14	02C0 0114		Base Address 1	PCIIF Base Address 1 Mask
0x18	02C0 0118		Base Address 2	PCIIF Base Address 2 Mask
0x1C	02C0 011C		Base Address 3	PCIIF Base Address 3 Mask
0x20	02C0 0120		Base Address 4	PCIIF Base Address 4 Mask
0x24	02C0 0124		Base Address 5	PCIIF Base Address 5 Mask
0x28	02C0 0128		Reserved	Reserved
0x2C	02C0 012C		Subsystem ID/Subsystem Vendor ID	PCIIF Subsystem Vendor ID/Subsystem ID Mirror
0x30	02C0 0130		Reserved	Reserved
0x34	02C0 0134		Capabilities Pointer	PCIIF Capabilities Pointer Mirror
0x38	02C0 0138		Reserved	Reserved
0x3C	02C0 013C		Max Latency/Min Grant/Interrupt Pin/Interrupt Line	PCIIF Max Latency/Min Grant/Interrupt Pin/Interrupt Line Mirror
0x40	02C0 0140		Power Management Capabili- ties	Power Management Capabili- ties Mirror
0x44	02C0 0144		Power Management Con- trol/Status	Power Management Con- trol/Status Mirror
0x48 - 0xFF	02C0 0148 - 02C0 015C		Reserved	Reserved
	02C0 0160			PCIIF Power Management D0 State Control
	02C0 0164			PCIIF Power Management D1 State Control
	02C0 0168			PCIIF Power Management D2 State Control
	02C0 016C			PCIIF Power Management D3 State Control
-	02C0 0170 - 02C0 017C		-	Reserved
-	02C0 0180		-	PCIIF Slave Control
-	02C0 0184		-	Reserved
-	02C0 0188 - 02C0 019C		-	Reserved
-	02C0 01A0 - 02C0 01AC		-	Reserved
-	02C0 01B0 - 02C0 01BC		-	Reserved
-	02C0 01C0		-	Slave Base Address Trans- lation Register 0
-	02C0 01C4		-	Slave Base Address Trans- lation Register 1
-	02C0 01C8		-	Slave Base Address Trans- lation Register 2
-	02C0 01CC		-	Slave Base Address Trans- lation Register 3
-	02C0 01D0		-	Slave Base Address Trans- lation Register 4
-	02C0 01D4		-	Slave Base Address Trans- lation Register 5
-	02C0 01D8 - 02C0 01DC		-	Reserved
-	02C0 01E0		-	PCIIF Base Address Regis- ter 0 Mirror
-	02C0 01E4		-	PCIIF Base Address Regis- ter 1 Mirror

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Table 6-22. PCI Peripheral Registers (continued)

PCI HOST ACCESS HEX ADDRESS OFFSET	DSP ACCESS HEX ADDRESS RANGE	ACRONYM	PCI HOST ACCESS REGISTER NAME	DSP ACCESS REGISTER NAME
-	02C0 01E8		-	PCIIF Base Address Register 2 Mirror
-	02C0 01EC		-	PCIIF Base Address Register 3 Mirror
-	02C0 01F0		-	PCIIF Base Address Register 4 Mirror
-	02C0 01F4		-	PCIIF Base Address Register 5 Mirror
-	02C0 01F8 - 02C0 02FC		-	Reserved
-	02C0 0300		-	Master Configuration/IO Access Data
-	02C0 0304		-	Master Configuration/IO Access Address
-	02C0 0308		-	Master Configuration/IO Access Command
-	02C0 030C		-	Reserved
-	02C0 0310		-	Master Configuration Register
-	02C0 0314		-	ADD_SUBS_0
-	02C0 0318		-	ADD_SUBS_1
-	02C0 031C		-	ADD_SUBS_2
-	02C0 0320		-	ADD_SUBS_3
-	02C0 0324		-	ADD_SUBS_4
-	02C0 0328		-	ADD_SUBS_5
-	02C0 032C		-	ADD_SUBS_6
-	02C0 0330		-	ADD_SUBS_7
-	02C0 0334		-	ADD_SUBS_8
-	02C0 0338		-	ADD_SUBS_9
-	02C0 033C		-	ADD_SUBS_10
-	02C0 0340		-	ADD_SUBS_11
-	02C0 0344		-	ADD_SUBS_12
-	02C0 0348		-	ADD_SUBS_13
-	02C0 034C		-	ADD_SUBS_14
-	02C0 0350		-	ADD_SUBS_15
-	02C0 0354		-	ADD_SUBS_16
-	02C0 0358		-	ADD_SUBS_17
-	02C0 035C		-	ADD_SUBS_18
-	02C0 0360		-	ADD_SUBS_19
-	02C0 0364		-	ADD_SUBS_20
-	02C0 0368		-	ADD_SUBS_21
-	02C0 036C		-	ADD_SUBS_22
-	02C0 0370		-	ADD_SUBS_23
-	02C0 0374		-	ADD_SUBS_24
-	02C0 0378		-	ADD_SUBS_25
-	02C0 037C		-	ADD_SUBS_26
-	02C0 0380		-	ADD_SUBS_27
-	02C0 0384		-	ADD_SUBS_28
-	02C0 0388		-	ADD_SUBS_29
-	02C0 038C		-	ADD_SUBS_30

Table 6-22. PCI Peripheral Registers (continued)

PCI HOST ACCESS HEX ADDRESS OFFSET	DSP ACCESS HEX ADDRESS RANGE	ACRONYM	PCI HOST ACCESS REGISTER NAME	DSP ACCESS REGISTER NAME
-	02C0 0390		-	ADD_SUBS_31
-	02C0 0394		-	vendor device id_prog
-	02C0 0398		-	cmd_stat_prog
-	02C0 039C		-	class_code_rev_id_prog
-	02C0 03A0		-	subsys_vendor_id_subsys_id_prog
-	02C0 03A4		-	max_lat_min_grant_prog
-	02C0 03A8		-	LRESET_REG
-	02C0 03AC		-	CONFIG_DONE_REG
-	02C0 03B0		-	base_addr_mask_reg0_prog
-	02C0 03B4		-	base_addr_mask_reg1_prog
-	02C0 03B8		-	base_addr_mask_reg2_prog
-	02C0 03BC		-	base_addr_mask_reg3_prog
-	02C0 03C0		-	base_addr_mask_reg4_prog
-	02C0 03C4		-	base_addr_mask_reg5_prog
-	02C0 03C8		-	base_address_reg0_prog
-	02C0 03CC		-	base_address_reg1_prog
-	02C0 03D0		-	base_address_reg2_prog
-	02C0 03D4		-	base_address_reg3_prog
-	02C0 03D8		-	base_address_reg4_prog
-	02C0 03DC		-	base_address_reg5_prog
-	02C0 03E0 - 02C0 03FC		-	Reserved

6.23.2 PCI Peripheral Register Description(s)

6.23.3 PCI Electrical Data/Timing

6.24 UTOPIA

6.24.1 UTOPIA Device-Specific Information

The Universal Test and Operations PHY Interface for ATM (UTOPIA) peripheral is a 50 MHz, 8-Bit Slave-only interface. The UTOPIA is more simplistic than the Ethernet MAC, in that the UTOPIA is serviced directly by the EDMA. The UTOPIA peripheral contains two, two-cell FIFOs, one for transmit and one for receive, with which to buffer up data sent/received across the pins. There is a transmit and a receive event to the EDMA to enable servicing.

For more detailed information on the UTOPIA peripheral, see the *TMS320C64x+ DSP Universal Test and Operations PHY interface for ATM (UTOPIA) Reference Guide* (literature number SPRUTBD).

6.24.2 UTOPIA Peripheral Register Description(s)

Table 6-23. UTOPIA Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02B4 0000	UCR	UTOPIA control register
02B4 0004	-	Reserved
02B4 0008	-	Reserved
02B4 000C	UIER	UTOPIA interrupt enable register
02B4 0010	UIPR	UTOPIA interrupt pending register
02B4 0014	CDR	Clock detect register
02B4 0018	EIER	Error interrupt enable register
02B4 001C	EIPR	Error interrupt pending register
02B4 0020 - 02B4 01FF	-	Reserved
02B4 0200 - 02B7 FFFF	-	Reserved

Table 6-24. UTOPIA Data Queues (Receive and Transmit) Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
3C00 0000 - 3CFF FFFF	URQ	UTOPIA receive (Rx) data queue
3D00 0000 - 3DFF FFFF	UXQ	UTOPIA transmit (Tx) data queue

6.24.3 UTOPIA Electrical Data/Timing

6.25 Serial Rapid I/O (RIO) Port

6.25.1 Serial RIO Device-Specific Information

The Serial RapidIO peripheral is new for the C6455 device, and is a master peripheral.

The PHY part of the RIO consists of the physical layer and includes the input and output buffers (each serial link consists of a differential pair), the 8b/10b encoder/decoder, the PLL clock recovery, and the parallel-to-serial/serial-to-parallel converters.

Beyond the PHY Port, the RapidIO peripheral includes support for all of the RapidIO protocol, including packet header interpretation, packet forwarding, interrupts, etc.

The RapidIO interface unit on the C6455 device is a high-performance, low-pin count interconnect aimed for embedded market. The use of the RapidIO interconnect in a baseband board design can create a homogeneous interconnect environment, providing even more connectivity and control among the components. RapidIO is based on the memory and device addressing concepts of processor buses where the transaction processing is managed completely by hardware. This enables the RapidIO interconnect to lower the system cost by providing lower latency, reduced overhead of packet data processing, and higher system bandwidth, all of which are key for wireless interfaces. The RapidIO interconnect offers very low pin count interfaces with scalable system bandwidth based on 10-Gigabit per second (Gbps) bidirectional links.

The RapidIO interface should be designed to operate at a data rate of 3 125 Gbps per differential pair. This equals 12.5 raw Gbps for the 4x RapidIO port, or approximately 9 Gbps data throughput rate (without 8b/10b encoding and packet headers). For the 1x RapidIO ports, this equals 2.25 Gbps data throughput rate.

6.25.2 Serial RIO Peripheral Register Description(s)

Table 6-25. RapidIO Control Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 0000	RIOPID	RapidIO Peripheral Identification Register
02D0 0004	RIO_PCR	RapidIO Peripheral Control Register
02D0 0008	RIO_DFT1	RapidIO DFT Control 1 Register
02D0 000C	RIO_DFT2	RapidIO DFT Control 2 Register
02D0 0010	-	Reserved
02D0 0014	-	Reserved
02D0 0018	-	Reserved
02D0 001C	-	Reserved
02D0 0020	RIO_PER_SET_CNTL	RapidIO Peripheral Settings Control Register
02D0 0024	RIO_PER_SET_CNTL2	RapidIO SerDes Enable PLL Control Register
02D0 0028 - 02D0 002C	-	Reserved
02D0 0030	RIO_GBL_EN	RapidIO Peripheral Global Enable Register
02D0 0034	RIO_GBL_EN_STAT	RapidIO Peripheral Global Enable Status Register
02D0 0038	RIO_BLK0_EN	RapidIO Block0 Enable Register
02D0 003C	RIO_BLK0_EN_STAT	RapidIO Block0 Enable Status Register
02D0 0040	RIO_BLK1_EN	RapidIO Block1 Enable Register
02D0 0044	RIO_BLK1_EN_STAT	RapidIO Block1 Enable Status Register
02D0 0048	RIO_BLK2_EN	RapidIO Block2 Enable Register
02D0 004C	RIO_BLK2_EN_STAT	RapidIO Block2 Enable Status Register
02D0 0050	RIO_BLK3_EN	RapidIO Block3 Enable Register
02D0 0054	RIO_BLK3_EN_STAT	RapidIO Block3 Enable Status Register
02D0 0058	RIO_BLK4_EN	RapidIO Block4 Enable Register
02D0 005C	RIO_BLK4_EN_STAT	RapidIO Block4 Enable Status Register
02D0 0060	RIO_BLK5_EN	RapidIO Block5 Enable Register
02D0 0064	RIO_BLK5_EN_STAT	RapidIO Block5 Enable Status Register
02D0 0068	RIO_BLK6_EN	RapidIO Block6 Enable Register
02D0 006C	RIO_BLK6_EN_STAT	RapidIO Block6 Enable Status Register
02D0 0070	RIO_BLK7_EN	RapidIO Block7 Enable Register
02D0 0074	RIO_BLK7_EN_STAT	RapidIO Block7 Enable Status Register
02D0 0078	RIO_BLK8_EN	RapidIO Block8 Enable Register
02D0 007C	RIO_BLK8_EN_STAT	RapidIO Block8 Enable Status Register
02D0 0080	RIO_GBL_PD_REQ	RapidIO Peripheral Global Powerdown Request Register
02D0 0084	RIO_GBL_PD_ACK	RapidIO Peripheral Global Powerdown Acknowledge Register
02D0 0088	RIO_GBL_PD_STAT	RapidIO Peripheral Global Powerdown Status Register
02D0 008C	RIO_BLK0_PD_REQ	RapidIO BLK0 Powerdown Request Register
02D0 0090	RIO_BLK0_PD_ACK	RapidIO BLK0 Powerdown Acknowledge Register
02D0 0094	RIO_BLK0_PD_STAT	RapidIO BLK0 Power Down Status Register
02D0 0098	RIO_BLK1_PD_REQ	RapidIO BLK1 Powerdown Acknowledge Register
02D0 009C	RIO_BLK1_PD_ACK	RapidIO BLK1 Powerdown Status Register
02D0 00A0	RIO_BLK1_PD_STAT	RapidIO BLK1 Powerdown Status Register
02D0 00A4	RIO_BLK2_PD_REQ	RapidIO BLK2 Powerdown Request Register
02D0 00A8	RIO_BLK2_PD_ACK	RapidIO BLK2 Powerdown Acknowledge Register
02D0 00AC	RIO_BLK2_PD_STAT	RapidIO BLK2 Powerdown Status Register

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Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 00B0	RIO_BLK3_PD_REQ	RapidIO BLK3 Powerdown Request Register
02D0 00B4	RIO_BLK3_PD_ACK	RapidIO BLK3 Powerdown Acknowledge Register
02D0 00B8	RIO_BLK3_PD_STAT	RapidIO BLK3 Powerdown Status Register
02D0 00BC	RIO_BLK4_PD_REQ	RapidIO BLK4 Powerdown Request Register
02D0 00C0	RIO_BLK4_PD_ACK	RapidIO BLK4 Powerdown Acknowledge Register
02D0 00C4	RIO_BLK4_PD_STAT	RapidIO BLK4 Powerdown Status Register
02D0 00C8	RIO_BLK5_PD_REQ	RapidIO BLK5 Powerdown Request Register
02D0 00CC	RIO_BLK5_PD_ACK	RapidIO BLK5 Powerdown Acknowledge Register
02D0 00D0	RIO_BLK5_PD_STAT	RapidIO BLK5 Powerdown Status Register
02D0 00D4	RIO_BLK6_PD_REQ	RapidIO BLK6 Powerdown Request Register
02D0 00D8	RIO_BLK6_PD_ACK	RapidIO BLK6 Powerdown Acknowledge Register
02D0 00DC	RIO_BLK6_PD_STAT	RapidIO BLK6 Powerdown Status Register
02D0 00E0	RIO_BLK7_PD_REQ	RapidIO BLK7 Powerdown Request Register
02D0 00E4	RIO_BLK7_PD_ACK	RapidIO BLK7 Powerdown Acknowledge Register
02D0 00E8	RIO_BLK7_PD_STAT	RapidIO BLK7 Powerdown Status Register
02D0 00EC	RIO_BLK8_PD_REQ	RapidIO BLK8 Powerdown Request Register
02D0 00F0	RIO_BLK8_PD_ACK	RapidIO BLK8 Powerdown Acknowledge Register
02D0 00F4	RIO_BLK8_PD_STAT	RapidIO BLK8 Powerdown Status Register
02D0 00F8 - 02D0 00FC	-	Reserved
02D0 0100	RIO_SERDES_CFGRX0_CNTL	RapidIO SerDes RX Channel 0 CFG Register
02D0 0104	RIO_SERDES_CFGRX1_CNTL	RapidIO SerDes RX Channel 1 CFG Register
02D0 0108	RIO_SERDES_CFGRX2_CNTL	RapidIO SerDes RX Channel 2 CFG Register
02D0 010C	RIO_SERDES_CFGRX3_CNTL	RapidIO SerDes RX Channel 3 CFG Register
02D0 0110	RIO_SERDES_CFGTX0_CNTL	RapidIO SerDes TX Channel 0 CFG Register
02D0 0114	RIO_SERDES_CFGTX1_CNTL	RapidIO SerDes TX Channel 1 CFG Register
02D0 0118	RIO_SERDES_CFGTX2_CNTL	RapidIO SerDes TX Channel 2 CFG Register
02D0 011C	RIO_SERDES_CFGTX3_CNTL	RapidIO SerDes TX Channel 3 CFG Register
02D0 0120	RIO_SERDES_CFG1_CNTL	RapidIO SerDes Macro 1 CFG Control Register
02D0 0124	-	Reserved
02D0 0128	RIO_SERDES_CFG2_CNTL	RapidIO SerDes Macro 2 CFG Control Register
02D0 012C	-	Reserved
02D0 0130	RIO_SERDES_CFG3_CNTL	RapidIO SerDes Macro 3 CFG Control Register
02D0 0134	-	Reserved
02D0 0138	RIO_SERDES_CFG4_CNTL	RapidIO SerDes Macro 4 CFG Control Register
02D0 013C	-	Reserved
02D0 0140	RIO_SERDES_TESTCFG1_CNTL	RapidIO SerDes Macro 1 TESTCFG Control Register
02D0 0144	RIO_SERDES_TESTCFG2_CNTL	RapidIO SerDes Macro 2 TESTCFG Control Register
02D0 0148	RIO_SERDES_TESTCFG3_CNTL	RapidIO SerDes Macro 3 TESTCFG Control Register
02D0 014C	RIO_SERDES_TESTCFG4_CNTL	RapidIO SerDes Macro 4 TESTCFG Control Register
02D0 0150 - 02D0 01FC	-	Reserved
02D0 0200	RIO_CPU0_ICSR	RapidIO CPU0 Interrupt Status Register
02D0 0204	-	Reserved
02D0 0208	RIO_CPU0_ICCR	RapidIO CPU0 Interrupt Clear Register
02D0 020C	-	Reserved

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 0210	RIO_CPU1_ICSR	RapidIO CPU1 Interrupt Status Register
02D0 0214	-	Reserved
02D0 0218	RIO_CPU1_ICCR	RapidIO CPU1 Interrupt Clear Register
02D0 021C	-	Reserved
02D0 0220	RIO_CPU2_ICSR	RapidIO CPU2 Interrupt Status Register
02D0 0224	-	Reserved
02D0 0228	RIO_CPU2_ICCR	RapidIO CPU2 Interrupt Clear Register
02D0 022C	-	Reserved
02D0 0230	RIO_CPU3_ICSR	RapidIO CPU3 Interrupt Status Register
02D0 0234	-	Reserved
02D0 0238	RIO_CPU3_ICCR	RapidIO CPU3 Interrupt Clear Register
02D0 023C	-	Reserved
02D0 0240	RIO_RX_CPPI_ICSR	RapidIO RX CPPI Interrupt Status Register
02D0 0244 - 02D0 024C	-	Reserved
02D0 0250	RIO_TX_CPPI_ICSR	RapidIO TX CPPI Interrupt Status Register
02D0 0254 - 02D0 025C	-	Reserved
02D0 0260	RIO_LSU_ICSR	RapidIO LSU Status Interrupt Register
02D0 0264	-	Reserved
02D0 0268	RIO_LSU_ICCR	RapidIO LSU Clear Interrupt Register
02D0 026C	-	Reserved
02D0 0270	RIO_ERR_RST_EVNT_ICSR	RapidIO Error, Reset, and Special Event Status Interrupt Register
02D0 0274	-	Reserved
02D0 0278	RIO_ERR_RST_EVNT_ICCR	RapidIO Error, Reset, and Special Event Clear Interrupt Register
02D0 027C	-	Reserved
02D0 0280	RIO_CPU0_ICRR	RapidIO CPU0 Interrupt Condition Routing Register
02D0 0284	RIO_CPU0_ICRR2	RapidIO CPU0 Interrupt Condition Routing Register 2
02D0 0288 - 02D0 028C	-	Reserved
02D0 0290	RIO_CPU1_ICRR	RapidIO CPU1 Interrupt Condition Routing Register
02D0 0294	RIO_CPU1_ICRR2	RapidIO CPU1 Interrupt Condition Routing Register 2
02D0 0298 - 02D0 029C	-	Reserved
02D0 02A0	RIO_CPU2_ICRR	RapidIO CPU2 Interrupt Condition Routing Register
02D0 02A4	RIO_CPU2_ICRR2	RapidIO CPU2 Interrupt Condition Routing Register 2
02D0 02A8 - 02D0 02AC	-	Reserved
02D0 02B0	RIO_CPU3_ICRR	RapidIO CPU3 Interrupt Condition Routing Register
02D0 02B4	RIO_CPU3_ICRR2	RapidIO CPU3 Interrupt Condition Routing Register 2
02D0 02B8 - 02D0 02BC	-	Reserved
02D0 02C0	RIO_RX_CPPI_ICRR	RapidIO RX CPPI Interrupt Condition Routing Register
02D0 02C4	RIO_RX_CPPI_ICRR2	RapidIO RX CPPI Interrupt Condition Routing Register 2
02D0 02C8	RIO_RX_CPPI_ICRR3	RapidIO RX CPPI Interrupt Condition Routing Register 3
02D0 02CC	-	Reserved
02D0 02D0	RIO_TX_CPPI_ICRR	RapidIO TX CPPI Interrupt Condition Routing Register
02D0 02D4	RIO_TX_CPPI_ICRR2	RapidIO TX CPPI Interrupt Condition Routing Register 2
02D0 02D8	RIO_TX_CPPI_ICRR3	RapidIO TX CPPI Interrupt Condition Routing Register 3
02D0 02DC	-	Reserved
02D0 02E0	RIO_LSU_ICRR	RapidIO LSU Module Interrupt Condition Routing Register
02D0 02E4	RIO_LSU_ICRR2	RapidIO LSU Module Interrupt Condition Routing Register 2
02D0 02E8	RIO_LSU_ICRR3	RapidIO LSU Module Interrupt Condition Routing Register 3

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 02EC	RIO_LSU_ICRR4	RapidIO LSU Module Interrupt Condition Routing Register 4
02D0 02F0	RIO_ERR_RST_EVNT_ICRR	RapidIO Error/Reset/special event Interrupt Condition Routing Register
02D0 02F4	RIO_ERR_RST_EVNT_ICRR2	RapidIO Error/Reset/special event Interrupt Condition Routing Register 2
02D0 02F8	RIO_ERR_RST_EVNT_ICRR3	RapidIO Error/Reset/special event Interrupt Condition Routing Register 3
02D0 02FC	-	Reserved
02D0 0300	RIO_INTDST0_Decode	RapidIO INTDST0 Interrupt Status Decode Register
02D0 0304	RIO_INTDST1_Decode	RapidIO INTDST1 Interrupt Status Decode Register
02D0 0308	RIO_INTDST2_Decode	RapidIO INTDST2 Interrupt Status Decode Register
02D0 030C	RIO_INTDST3_Decode	RapidIO INTDST3 Interrupt Status Decode Register
02D0 0310	RIO_INTDST4_Decode	RapidIO INTDST4 Interrupt Status Decode Register
02D0 0314	RIO_INTDST5_Decode	RapidIO INTDST5 Interrupt Status Decode Register
02D0 0318	RIO_INTDST6_Decode	RapidIO INTDST6 Interrupt Status Decode Register
02D0 031C	RIO_INTDST7_Decode	RapidIO INTDST7 Interrupt Status Decode Register
02D0 0320	RIO_INTDST0_Rate_CNTL	RapidIO INTDST0 Interrupt Rate Control Register
02D0 0324	RIO_INTDST1_Rate_CNTL	RapidIO INTDST1 Interrupt Rate Control Register
02D0 0328	RIO_INTDST2_Rate_CNTL	RapidIO INTDST2 Interrupt Rate Control Register
02D0 032C	RIO_INTDST3_Rate_CNTL	RapidIO INTDST3 Interrupt Rate Control Register
02D0 0330	RIO_INTDST4_Rate_CNTL	RapidIO INTDST4 Interrupt Rate Control Register
02D0 0334	RIO_INTDST5_Rate_CNTL	RapidIO INTDST5 Interrupt Rate Control Register
02D0 0338	RIO_INTDST6_Rate_CNTL	RapidIO INTDST6 Interrupt Rate Control Register
02D0 033C	RIO_INTDST7_Rate_CNTL	RapidIO INTDST7 Interrupt Rate Control Register
02D0 0340 - 02D0 03FC	-	Reserved
02D0 0400	RIO_LSU1_Reg0	RapidIO LSU1 Control Reg0 Register
02D0 0404	RIO_LSU1_Reg1	RapidIO LSU1 Control Reg1 Register
02D0 0408	RIO_LSU1_Reg2	RapidIO LSU1 Control Reg2 Register
02D0 040C	RIO_LSU1_Reg3	RapidIO LSU1 Control Reg3 Register
02D0 0410	RIO_LSU1_Reg4	RapidIO LSU1 Control Reg4 Register
02D0 0414	RIO_LSU1_Reg5	RapidIO LSU1 Command Reg5 Register
02D0 0418	RIO_LSU1_Reg6	RapidIO LSU1 Status Reg6 Register
02D0 041C	RIO_LSU1_FLOW_MASKS	RapidIO Core0 LSU Congestion Control Flow Mask Register
02D0 0420	RIO_LSU2_Reg0	RapidIO LSU2 Control Reg0 Register
02D0 0424	RIO_LSU2_Reg1	RapidIO LSU2 Control Reg1 Register
02D0 0428	RIO_LSU2_Reg2	RapidIO LSU2 Control Reg2 Register
02D0 042C	RIO_LSU2_Reg3	RapidIO LSU2 Control Reg3 Register
02D0 0430	RIO_LSU2_Reg4	RapidIO LSU2 Control Reg4 Register
02D0 0434	RIO_LSU2_Reg5	RapidIO LSU2 Command Reg5 Register
02D0 0438	RIO_LSU2_Reg6	RapidIO LSU2 Status Reg6 Register
02D0 043C	RIO_LSU2_FLOW_MASKS	RapidIO Core1 LSU Congestion Control Flow Mask Register
02D0 0440	RIO_LSU3_Reg0	RapidIO LSU3 Control Reg0 Register
02D0 0444	RIO_LSU3_Reg1	RapidIO LSU3 Control Reg1 Register
02D0 0448	RIO_LSU3_Reg2	RapidIO LSU3 Control Reg2 Register
02D0 044C	RIO_LSU3_Reg3	RapidIO LSU3 Control Reg3 Register
02D0 0450	RIO_LSU3_Reg4	RapidIO LSU3 Control Reg4 Register
02D0 0454	RIO_LSU3_Reg5	RapidIO LSU3 Command Reg5 Register
02D0 0458	RIO_LSU3_Reg6	RapidIO LSU3 Status Reg6 Register

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 045C	RIO_LSU3_FLOW_MASKS	RapidIO Core2 LSU Congestion Control Flow Mask Register
02D0 0460	RIO_LSU4_Reg0	RapidIO LSU4 Control Reg0 Register
02D0 0464	RIO_LSU4_Reg1	RapidIO LSU4 Control Reg1 Register
02D0 0468	RIO_LSU4_Reg2	RapidIO LSU4 Control Reg2 Register
02D0 046C	RIO_LSU4_Reg3	RapidIO LSU4 Control Reg3 Register
02D0 0470	RIO_LSU4_Reg4	RapidIO LSU4 Control Reg4 Register
02D0 0474	RIO_LSU4_Reg5	RapidIO LSU4 Command Reg5 Register
02D0 0478	RIO_LSU4_Reg6	RapidIO LSU4 Status Reg6 Register
02D0 047C	RIO_LSU4_FLOW_MASKS	RapidIO Core3 LSU Congestion Control Flow Mask Register
02D0 0480 - 02D0 04FC	-	Reserved
02D0 0500	RIO_Queue0_TxDMA_HDP	RapidIO Queue0 TX DMA Head Descriptor Pointer Register
02D0 0504	RIO_Queue1_TxDMA_HDP	RapidIO Queue1 TX DMA Head Descriptor Pointer Register
02D0 0508	RIO_Queue2_TxDMA_HDP	RapidIO Queue2 TX DMA Head Descriptor Pointer Register
02D0 050C	RIO_Queue3_TxDMA_HDP	RapidIO Queue3 TX DMA Head Descriptor Pointer Register
02D0 0510	RIO_Queue4_TxDMA_HDP	RapidIO Queue4 TX DMA Head Descriptor Pointer Register
02D0 0514	RIO_Queue5_TxDMA_HDP	RapidIO Queue5 TX DMA Head Descriptor Pointer Register
02D0 0518	RIO_Queue6_TxDMA_HDP	RapidIO Queue6 TX DMA Head Descriptor Pointer Register
02D0 051C	RIO_Queue7_TxDMA_HDP	RapidIO Queue7 TX DMA Head Descriptor Pointer Register
02D0 0520	RIO_Queue8_TxDMA_HDP	RapidIO Queue8 TX DMA Head Descriptor Pointer Register
02D0 0524	RIO_Queue9_TxDMA_HDP	RapidIO Queue9 TX DMA Head Descriptor Pointer Register
02D0 0528	RIO_Queue10_TxDMA_HDP	RapidIO Queue10 TX DMA Head Descriptor Pointer Register
02D0 052C	RIO_Queue11_TxDMA_HDP	RapidIO Queue11 TX DMA Head Descriptor Pointer Register
02D0 0530	RIO_Queue12_TxDMA_HDP	RapidIO Queue12 TX DMA Head Descriptor Pointer Register
02D0 0534	RIO_Queue13_TxDMA_HDP	RapidIO Queue13 TX DMA Head Descriptor Pointer Register
02D0 0538	RIO_Queue14_TxDMA_HDP	RapidIO Queue14 TX DMA Head Descriptor Pointer Register
02D0 053C	RIO_Queue15_TxDMA_HDP	RapidIO Queue15 TX DMA Head Descriptor Pointer Register
02D0 0540	RIO_Queue16_TxDMA_HDP	RapidIO Queue16 TX DMA Head Descriptor Pointer Register
02D0 0544	RIO_Queue17_TxDMA_HDP	RapidIO Queue17 TX DMA Head Descriptor Pointer Register
02D0 0548	RIO_Queue18_TxDMA_HDP	RapidIO Queue18 TX DMA Head Descriptor Pointer Register
02D0 054C	RIO_Queue19_TxDMA_HDP	RapidIO Queue19 TX DMA Head Descriptor Pointer Register
02D0 0550 - 02D0 057C	-	Reserved
02D0 0580	RIO_Queue0_TxDMA_CP	RapidIO Queue0 TX DMA Completion Pointer Register
02D0 0584	RIO_Queue1_TxDMA_CP	RapidIO Queue1 TX DMA Completion Pointer Register
02D0 0588	RIO_Queue2_TxDMA_CP	RapidIO Queue2 TX DMA Completion Pointer Register
02D0 058C	RIO_Queue3_TxDMA_CP	RapidIO Queue3 TX DMA Completion Pointer Register
02D0 0590	RIO_Queue4_TxDMA_CP	RapidIO Queue4 TX DMA Completion Pointer Register
02D0 0594	RIO_Queue5_TxDMA_CP	RapidIO Queue5 TX DMA Completion Pointer Register
02D0 0598	RIO_Queue6_TxDMA_CP	RapidIO Queue6 TX DMA Completion Pointer Register
02D0 059C	RIO_Queue7_TxDMA_CP	RapidIO Queue7 TX DMA Completion Pointer Register
02D0 05A0	RIO_Queue8_TxDMA_CP	RapidIO Queue8 TX DMA Completion Pointer Register
02D0 05A4	RIO_Queue9_TxDMA_CP	RapidIO Queue9 TX DMA Completion Pointer Register
02D0 05A8	RIO_Queue10_TxDMA_CP	RapidIO Queue10 TX DMA Completion Pointer Register
02D0 05AC	RIO_Queue11_TxDMA_CP	RapidIO Queue11 TX DMA Completion Pointer Register
02D0 05B0	RIO_Queue12_TxDMA_CP	RapidIO Queue12 TX DMA Completion Pointer Register
02D0 05B4	RIO_Queue13_TxDMA_CP	RapidIO Queue13 TX DMA Completion Pointer Register
02D0 05B8	RIO_Queue14_TxDMA_CP	RapidIO Queue14 TX DMA Completion Pointer Register
02D0 05BC	RIO_Queue15_TxDMA_CP	RapidIO Queue15 TX DMA Completion Pointer Register

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 05C0	RIO_Queue16_TxDMA_CP	RapidIO Queue16 TX DMA Completion Pointer Register
02D0 05C4	RIO_Queue17_TxDMA_CP	RapidIO Queue17 TX DMA Completion Pointer Register
02D0 05C8	RIO_Queue18_TxDMA_CP	RapidIO Queue18 TX DMA Completion Pointer Register
02D0 05CC	RIO_Queue19_TxDMA_CP	RapidIO Queue19 TX DMA Completion Pointer Register
02D0 05D0 - 02D0 05FC	-	Reserved
02D0 0600	RIO_Queue0_RxDMA_HDP	RapidIO Queue0 RX DMA Head Descriptor Pointer Register
02D0 0604	RIO_Queue1_RxDMA_HDP	RapidIO Queue1 RX DMA Head Descriptor Pointer Register
02D0 0608	RIO_Queue2_RxDMA_HDP	RapidIO Queue2 RX DMA Head Descriptor Pointer Register
02D0 060C	RIO_Queue3_RxDMA_HDP	RapidIO Queue3 RX DMA Head Descriptor Pointer Register
02D0 0610	RIO_Queue4_RxDMA_HDP	RapidIO Queue4 RX DMA Head Descriptor Pointer Register
02D0 0614	RIO_Queue5_RxDMA_HDP	RapidIO Queue5 RX DMA Head Descriptor Pointer Register
02D0 0618	RIO_Queue6_RxDMA_HDP	RapidIO Queue6 RX DMA Head Descriptor Pointer Register
02D0 061C	RIO_Queue7_RxDMA_HDP	RapidIO Queue7 RX DMA Head Descriptor Pointer Register
02D0 0620	RIO_Queue8_RxDMA_HDP	RapidIO Queue8 RX DMA Head Descriptor Pointer Register
02D0 0624	RIO_Queue9_RxDMA_HDP	RapidIO Queue9 RX DMA Head Descriptor Pointer Register
02D0 0628	RIO_Queue10_RxDMA_HDP	RapidIO Queue10 RX DMA Head Descriptor Pointer Register
02D0 062C	RIO_Queue11_RxDMA_HDP	RapidIO Queue11 RX DMA Head Descriptor Pointer Register
02D0 0630	RIO_Queue12_RxDMA_HDP	RapidIO Queue12 RX DMA Head Descriptor Pointer Register
02D0 0634	RIO_Queue13_RxDMA_HDP	RapidIO Queue13 RX DMA Head Descriptor Pointer Register
02D0 0638	RIO_Queue14_RxDMA_HDP	RapidIO Queue14 RX DMA Head Descriptor Pointer Register
02D0 063C	RIO_Queue15_RxDMA_HDP	RapidIO Queue15 RX DMA Head Descriptor Pointer Register
02D0 0640	RIO_Queue16_RxDMA_HDP	RapidIO Queue16 RX DMA Head Descriptor Pointer Register
02D0 0644	RIO_Queue17_RxDMA_HDP	RapidIO Queue17 RX DMA Head Descriptor Pointer Register
02D0 0648	RIO_Queue18_RxDMA_HDP	RapidIO Queue18 RX DMA Head Descriptor Pointer Register
02D0 064C	RIO_Queue19_RxDMA_HDP	RapidIO Queue19 RX DMA Head Descriptor Pointer Register
02D0 0650 - 02D0 067C	-	Reserved
02D0 0680	RIO_Queue0_RxDMA_CP	RapidIO Queue0 RX DMA Completion Pointer Register
02D0 0684	RIO_Queue1_RxDMA_CP	RapidIO Queue1 RX DMA Completion Pointer Register
02D0 0688	RIO_Queue2_RxDMA_CP	RapidIO Queue2 RX DMA Completion Pointer Register
02D0 068C	RIO_Queue3_RxDMA_CP	RapidIO Queue3 RX DMA Completion Pointer Register
02D0 0690	RIO_Queue4_RxDMA_CP	RapidIO Queue4 RX DMA Completion Pointer Register
02D0 0694	RIO_Queue5_RxDMA_CP	RapidIO Queue5 RX DMA Completion Pointer Register
02D0 0698	RIO_Queue6_RxDMA_CP	RapidIO Queue6 RX DMA Completion Pointer Register
02D0 069C	RIO_Queue7_RxDMA_CP	RapidIO Queue7 RX DMA Completion Pointer Register
02D0 06A0	RIO_Queue8_RxDMA_CP	RapidIO Queue8 RX DMA Completion Pointer Register
02D0 06A4	RIO_Queue9_RxDMA_CP	RapidIO Queue9 RX DMA Completion Pointer Register
02D0 06A8	RIO_Queue10_RxDMA_CP	RapidIO Queue10 RX DMA Completion Pointer Register
02D0 06AC	RIO_Queue11_RxDMA_CP	RapidIO Queue11 RX DMA Completion Pointer Register
02D0 06B0	RIO_Queue12_RxDMA_CP	RapidIO Queue12 RX DMA Completion Pointer Register
02D0 06B4	RIO_Queue13_RxDMA_CP	RapidIO Queue13 RX DMA Completion Pointer Register
02D0 06B8	RIO_Queue14_RxDMA_CP	RapidIO Queue14 RX DMA Completion Pointer Register
02D0 06BC	RIO_Queue15_RxDMA_CP	RapidIO Queue15 RX DMA Completion Pointer Register
02D0 06C0	RIO_Queue16_RxDMA_CP	RapidIO Queue16 RX DMA Completion Pointer Register
02D0 06C4	RIO_Queue17_RxDMA_CP	RapidIO Queue17 RX DMA Completion Pointer Register
02D0 06C8	RIO_Queue18_RxDMA_CP	RapidIO Queue18 RX DMA Completion Pointer Register
02D0 06CC	RIO_Queue19_RxDMA_CP	RapidIO Queue19 RX DMA Completion Pointer Register
02D0 06D0 - 02D0 06FC	-	Reserved

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 0700	RIO_TX_QUEUE_TEAR_DOWN	RapidIO TX Queue Teardown Register
02D0 0704	RIO_TX_CPPI_FLOW_MASKS0	RapidIO TX CPPI Supported Flow Masks 0 Register
02D0 0708	RIO_TX_CPPI_FLOW_MASKS1	RapidIO TX CPPI Supported Flow Masks 1 Register
02D0 070C	RIO_TX_CPPI_FLOW_MASKS2	RapidIO TX CPPI Supported Flow Masks 2 Register
02D0 0710	RIO_TX_CPPI_FLOW_MASKS3	RapidIO TX CPPI Supported Flow Masks 3 Register
02D0 0714	RIO_TX_CPPI_FLOW_MASKS4	RapidIO TX CPPI Supported Flow Masks 4 Register
02D0 0718 - 02D0 073C	-	Reserved
02D0 0740	RIO_RX_QUEUE_TEAR_DOWN	RapidIO RX Queue Teardown Register
02D0 0744	RIO_RX_CPPI_CNTL	RapidIO RX CPPI Control Register
02D0 0748 - 02D0 077C	-	Reserved
02D0 0780	RIO_RXU_MMBX0_MAP1	RapidIO Multi-Segment 0 Message to Queue Map 1 Register
02D0 0784	RIO_RXU_MMBX0_MAP2	RapidIO Multi-Segment 0 Message to Queue Map 2 Register
02D0 0788	RIO_RXU_MMBX0_MAP3	RapidIO Multi-Segment 0 Message to Queue Map 3 Register
02D0 078C	RIO_RXU_MMBX0_MAP4	RapidIO Multi-Segment 0 Message to Queue Map 4 Register
02D0 0790	RIO_RXU_MMBX1_MAP1	RapidIO Multi-Segment 1 Message to Queue Map 1 Register
02D0 0794	RIO_RXU_MMBX1_MAP2	RapidIO Multi-Segment 1 Message to Queue Map 2 Register
02D0 0798	RIO_RXU_MMBX1_MAP3	RapidIO Multi-Segment 1 Message to Queue Map 3 Register
02D0 079C	RIO_RXU_MMBX1_MAP4	RapidIO Multi-Segment 1 Message to Queue Map 4 Register
02D0 07A0	RIO_RXU_MMBX2_MAP1	RapidIO Multi-Segment 2 Message to Queue Map 1 Register
02D0 07A4	RIO_RXU_MMBX2_MAP2	RapidIO Multi-Segment 2 Message to Queue Map 2 Register
02D0 07A8	RIO_RXU_MMBX2_MAP3	RapidIO Multi-Segment 2 Message to Queue Map 3 Register
02D0 07AC	RIO_RXU_MMBX2_MAP4	RapidIO Multi-Segment 2 Message to Queue Map 4 Register
02D0 07B0	RIO_RXU_MMBX3_MAP1	RapidIO Multi-Segment 3 Message to Queue Map 1 Register
02D0 07B4	RIO_RXU_MMBX3_MAP2	RapidIO Multi-Segment 3 Message to Queue Map 2 Register
02D0 07B8	RIO_RXU_MMBX3_MAP3	RapidIO Multi-Segment 3 Message to Queue Map 3 Register
02D0 07BC	RIO_RXU_MMBX3_MAP4	RapidIO Multi-Segment 3 Message to Queue Map 4 Register
02D0 07C0 - 02D0 07DC	-	Reserved
02D0 07E0	RIO_TX_QUEUE_CNTL0	RapidIO TX Queue Control 0 Register TBD
02D0 07E4	RIO_TX_QUEUE_CNTL1	RapidIO TX Queue Control 1 Register
02D0 07E8	RIO_TX_QUEUE_CNTL2	RapidIO TX Queue Control 2 Register
02D0 07EC	RIO_TX_QUEUE_CNTL3	RapidIO TX Queue Control 3 Register
02D0 07F0 - 02D0 07FC	-	Reserved
02D0 0800	RIO_RXU_SMBX00_MAP	RapidIO Single-Segment 00 Message to Queue Map Register
02D0 0804	RIO_RXU_SMBX01_MAP	RapidIO Single-Segment 01 Message to Queue Map Register
02D0 0808	RIO_RXU_SMBX02_MAP	RapidIO Single-Segment 02 Message to Queue Map Register
02D0 080C	RIO_RXU_SMBX03_MAP	RapidIO Single-Segment 03 Message to Queue Map Register
02D0 0810	RIO_RXU_SMBX04_MAP	RapidIO Single-Segment 04 Message to Queue Map Register
02D0 0814	RIO_RXU_SMBX05_MAP	RapidIO Single-Segment 05 Message to Queue Map Register
02D0 0818	RIO_RXU_SMBX06_MAP	RapidIO Single-Segment 06 Message to Queue Map Register
02D0 081C	RIO_RXU_SMBX07_MAP	RapidIO Single-Segment 07 Message to Queue Map Register
02D0 0820	RIO_RXU_SMBX08_MAP	RapidIO Single-Segment 08 Message to Queue Map Register
02D0 0824	RIO_RXU_SMBX09_MAP	RapidIO Single-Segment 09 Message to Queue Map Register
02D0 0828	RIO_RXU_SMBX10_MAP	RapidIO Single-Segment 10 Message to Queue Map Register
02D0 082C	RIO_RXU_SMBX11_MAP	RapidIO Single-Segment 11 Message to Queue Map Register
02D0 0830	RIO_RXU_SMBX12_MAP	RapidIO Single-Segment 12 Message to Queue Map Register
02D0 0834	RIO_RXU_SMBX13_MAP	RapidIO Single-Segment 13 Message to Queue Map Register
02D0 0838	RIO_RXU_SMBX14_MAP	RapidIO Single-Segment 14 Message to Queue Map Register

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 083C	RIO_RXU_SMBX15_MAP	RapidIO Single-Segment 15 Message to Queue Map Register
02D0 0840	RIO_RXU_SMBX16_MAP	RapidIO Single-Segment 16 Message to Queue Map Register
02D0 0844	RIO_RXU_SMBX17_MAP	RapidIO Single-Segment 17 Message to Queue Map Register
02D0 0848	RIO_RXU_SMBX18_MAP	RapidIO Single-Segment 18 Message to Queue Map Register
02D0 084C	RIO_RXU_SMBX19_MAP	RapidIO Single-Segment 19 Message to Queue Map Register
02D0 0850	RIO_RXU_SMBX20_MAP	RapidIO Single-Segment 20 Message to Queue Map Register
02D0 0854	RIO_RXU_SMBX21_MAP	RapidIO Single-Segment 21 Message to Queue Map Register
02D0 0858	RIO_RXU_SMBX22_MAP	RapidIO Single-Segment 22 Message to Queue Map Register
02D0 085C	RIO_RXU_SMBX23_MAP	RapidIO Single-Segment 23 Message to Queue Map Register
02D0 0860	RIO_RXU_SMBX24_MAP	RapidIO Single-Segment 24 Message to Queue Map Register
02D0 0864	RIO_RXU_SMBX25_MAP	RapidIO Single-Segment 25 Message to Queue Map Register
02D0 0868	RIO_RXU_SMBX26_MAP	RapidIO Single-Segment 26 Message to Queue Map Register
02D0 086C	RIO_RXU_SMBX27_MAP	RapidIO Single-Segment 27 Message to Queue Map Register
02D0 0870	RIO_RXU_SMBX28_MAP	RapidIO Single-Segment 28 Message to Queue Map Register
02D0 0874	RIO_RXU_SMBX29_MAP	RapidIO Single-Segment 29 Message to Queue Map Register
02D0 0878	RIO_RXU_SMBX30_MAP	RapidIO Single-Segment 30 Message to Queue Map Register
02D0 087C	RIO_RXU_SMBX31_MAP	RapidIO Single-Segment 31 Message to Queue Map Register
02D0 0880	RIO_RXU_SMBX32_MAP	RapidIO Single-Segment 32 Message to Queue Map Register
02D0 0884	RIO_RXU_SMBX33_MAP	RapidIO Single-Segment 33 Message to Queue Map Register
02D0 0888	RIO_RXU_SMBX34_MAP	RapidIO Single-Segment 34 Message to Queue Map Register
02D0 088C	RIO_RXU_SMBX35_MAP	RapidIO Single-Segment 35 Message to Queue Map Register
02D0 0890	RIO_RXU_SMBX36_MAP	RapidIO Single-Segment 36 Message to Queue Map Register
02D0 0894	RIO_RXU_SMBX37_MAP	RapidIO Single-Segment 37 Message to Queue Map Register
02D0 0898	RIO_RXU_SMBX38_MAP	RapidIO Single-Segment 38 Message to Queue Map Register
02D0 089C	RIO_RXU_SMBX39_MAP	RapidIO Single-Segment 39 Message to Queue Map Register
02D0 08A0	RIO_RXU_SMBX40_MAP	RapidIO Single-Segment 40 Message to Queue Map Register
02D0 08A4	RIO_RXU_SMBX41_MAP	RapidIO Single-Segment 41 Message to Queue Map Register
02D0 08A8	RIO_RXU_SMBX42_MAP	RapidIO Single-Segment 42 Message to Queue Map Register
02D0 08AC	RIO_RXU_SMBX43_MAP	RapidIO Single-Segment 43 Message to Queue Map Register
02D0 08B0	RIO_RXU_SMBX44_MAP	RapidIO Single-Segment 44 Message to Queue Map Register
02D0 08B4	RIO_RXU_SMBX45_MAP	RapidIO Single-Segment 45 Message to Queue Map Register
02D0 08B8	RIO_RXU_SMBX46_MAP	RapidIO Single-Segment 46 Message to Queue Map Register
02D0 08BC	RIO_RXU_SMBX47_MAP	RapidIO Single-Segment 47 Message to Queue Map Register
02D0 08C0	RIO_RXU_SMBX48_MAP	RapidIO Single-Segment 48 Message to Queue Map Register
02D0 08C4	RIO_RXU_SMBX49_MAP	RapidIO Single-Segment 49 Message to Queue Map Register
02D0 08C8	RIO_RXU_SMBX50_MAP	RapidIO Single-Segment 50 Message to Queue Map Register
02D0 08CC	RIO_RXU_SMBX51_MAP	RapidIO Single-Segment 51 Message to Queue Map Register
02D0 08D0	RIO_RXU_SMBX52_MAP	RapidIO Single-Segment 52 Message to Queue Map Register
02D0 08D4	RIO_RXU_SMBX53_MAP	RapidIO Single-Segment 53 Message to Queue Map Register
02D0 08D8	RIO_RXU_SMBX54_MAP	RapidIO Single-Segment 54 Message to Queue Map Register
02D0 08DC	RIO_RXU_SMBX55_MAP	RapidIO Single-Segment 55 Message to Queue Map Register
02D0 08E0	RIO_RXU_SMBX56_MAP	RapidIO Single-Segment 56 Message to Queue Map Register
02D0 08E4	RIO_RXU_SMBX57_MAP	RapidIO Single-Segment 57 Message to Queue Map Register
02D0 08E8	RIO_RXU_SMBX58_MAP	RapidIO Single-Segment 58 Message to Queue Map Register
02D0 08EC	RIO_RXU_SMBX59_MAP	RapidIO Single-Segment 59 Message to Queue Map Register
02D0 08F0	RIO_RXU_SMBX60_MAP	RapidIO Single-Segment 60 Message to Queue Map Register
02D0 08F4	RIO_RXU_SMBX61_MAP	RapidIO Single-Segment 61 Message to Queue Map Register

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 08F8	RIO_RXU_SMBX62_MAP	RapidIO Single-Segment 62 Message to Queue Map Register
02D0 08FC	RIO_RXU_SMBX63_MAP	RapidIO Single-Segment 63 Message to Queue Map Register
02D0 0900	RIO_FLOW_CNTL0	RapidIO Flow Control Table Entry Register0
02D0 0904	RIO_FLOW_CNTL1	RapidIO Flow Control Table Entry Register1
02D0 0908	RIO_FLOW_CNTL2	RapidIO Flow Control Table Entry Register2
02D0 090C	RIO_FLOW_CNTL3	RapidIO Flow Control Table Entry Register3
02D0 0910	RIO_FLOW_CNTL4	RapidIO Flow Control Table Entry Register4
02D0 0914	RIO_FLOW_CNTL5	RapidIO Flow Control Table Entry Register5
02D0 0918	RIO_FLOW_CNTL6	RapidIO Flow Control Table Entry Register6
02D0 091C	RIO_FLOW_CNTL7	RapidIO Flow Control Table Entry Register7
RapidIO Peripheral-Specific Registers		
02D0 0920 - 02D0 0FFC	-	Reserved
02D0 1000	RIO_DEV_ID	RapidIO Device Identity CAR Register
02D0 1004	RIO_DEV_INFO	RapidIO Device Information CAR Register
02D0 1008	RIO_ASBLY_ID	RapidIO Assembly Identity CAR Register
02D0 100C	RIO_ASBLY_INFO	RapidIO Assembly Information CAR Register
02D0 1010	RIO_PE_FEAT	RapidIO Processing Element Features CAR Register
02D0 1014	RIO_SW_PORT	RapidIO Switch Port Information CAR Register
02D0 1018	RIO_SRC_OP	RapidIO Source Operations CAR Register
02D0 101C	RIO_DEST_OP	RapidIO Destination Operations CAR Register
02D0 1020 - 02D0 1038	-	Reserved
02D0 1040	-	Reserved
02D0 1044 - 02D0 1048	-	Reserved
02D0 104C	RIO_PE_LL_CTL	RapidIO Processing Element Logical Layer Control CSR Register
02D0 1050	-	Reserved
02D0 1058	RIO_LCL_CFG_HBAR	RapidIO Local Configuration Space Base Address 0 CSR Register
02D0 105C	RIO_LCL_CFG_BAR	RapidIO Local Configuration Space Base Address 1 CSR Register
02D0 1060	RIO_BASE_ID	RapidIO Base Device ID CSR Register
02D0 1064	-	Reserved
02D0 1068	RIO_HOST_BASE_ID_LOCK	RapidIO Host Base Device ID Lock CSR Register
02D0 106C	RIO_COMP_TAG	RapidIO Component Tag CSR Register
02D0 1070 - 02D0 10F8	-	Reserved
02D0 10FC	-	Reserved
RapidIO Extended Features - LP Serial Registers		
02D0 1100	RIO_SP_MB_HEAD	RapidIO 1x/4x LP-Serial Port Maintenance Block Header Register
02D0 1104 - 02D0 1118	-	Reserved
02D0 111C	-	Reserved
02D0 1120	RIO_SP_LT_CTL	RapidIO Port Link Time-Out Control CSR Register
02D0 1124	RIO_SP_RT_CTL	RapidIO Port Response Time-Out Control CSR Register
02D0 1128	-	Reserved
02D0 112C	-	Reserved
02D0 1130 - 02D0 1138	-	Reserved
02D0 113C	RIO_SP_GEN_CTL	RapidIO Port General Control CSR Register
02D0 1140	RIO_SP0_LM_REQ	RapidIO Port 0 Link Maintenance Request CSR Register
02D0 1144	RIO_SP0_LM_RESP	RapidIO Port 0 Link Maintenance Response CSR Register
02D0 1148	RIO_SP0_ACKID_STAT	RapidIO Port 0 Local AckID Status CSR Register
02D0 114C - 02D0 1150	-	Reserved

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 1154	-	Reserved
02D0 1158	RIO_SP0_ERR_STAT	RapidIO Port 0 Error and Status CSR Register
02D0 115C	RIO_SP0_CTL	RapidIO Port 0 Control CSR Register
02D0 1160	RIO_SP1_LM_REQ	RapidIO Port 1 Link Maintenance Request CSR Register
02D0 1164	RIO_SP1_LM_RESP	RapidIO Port 1 Link Maintenance Response CSR Register
02D0 1168	RIO_SP1_ACKID_STAT	RapidIO Port 1 Local AckID Status CSR Register
02D0 116C- 02D0 1170	-	Reserved
02D0 1174	-	Reserved
02D0 1178	RIO_SP1_ERR_STAT	RapidIO Port 1 Error and Status CSR Register
02D0 117C	RIO_SP1_CTL	RapidIO Port 1 Control CSR Register
02D0 1180	RIO_SP2_LM_REQ	RapidIO Port 2 Link Maintenance Request CSR Register
02D0 1184	RIO_SP2_LM_RESP	RapidIO Port 2 Link Maintenance Response CSR Register
02D0 1188	RIO_SP2_ACKID_STAT	RapidIO Port 2 Local AckID Status CSR Register
02D0 118C - 02D0 1190	-	Reserved
02D0 1194	-	Reserved
02D0 1198	RIO_SP2_ERR_STAT	RapidIO Port 2 Error and Status CSR Register
02D0 119C	RIO_SP2_CTL	RapidIO Port 2 Control CSR Register
02D0 11A0	RIO_SP3_LM_REQ	RapidIO Port 3 Link Maintenance Request CSR Register
02D0 11A4	RIO_SP3_LM_RESP	RapidIO Port 3 Link Maintenance Response CSR Register
02D0 11A8	RIO_SP3_ACKID_STAT	RapidIO Port 3 Local AckID Status CSR Register
02D0 11AC - 02D0 11B0	-	Reserved
02D0 11B4	-	Reserved
02D0 11B8	RIO_SP3_ERR_STAT	RapidIO Port 3 Error and Status CSR Register
02D0 11BC	RIO_SP3_CTL	RapidIO Port 3 Control CSR Register
02D0 11C0 - 02D0 1FFC	-	Reserved
RapidIO Extended Feature - Error Management Registers		
02D0 2000	RIO_ERR_RPT_BH	RapidIO Error Reporting Block Header Register
02D0 2004	-	Reserved
02D0 2008	RIO_ERR_DET	RapidIO Logical/Transport Layer Error Detect CSR Register
02D0 200C	RIO_ERR_EN	RapidIO Logical/Transport Layer Error Enable CSR Register
02D0 2010	RIO_H_ADDR_CAPT	RapidIO Logical/Transport Layer High Address Capture CSR Register
02D0 2014	RIO_ADDR_CAPT	RapidIO Logical/Transport Layer Address Capture CSR Register
02D0 2018	RIO_ID_CAPT	RapidIO Logical/Transport Layer Device ID Capture CSR Register
02D0 201C	RIO_CTRL_CAPT	RapidIO Logical/Transport Layer Control Capture CSR Register
02D0 2020 - 02D0 2024	-	Reserved
02D0 2028	RIO_PW_TGT_ID	RapidIO Port-Write Target Device ID CSR Register
02D0 202C	RIO_PKT_TIME_LIVE	RapidIO Packet Time-to-Live CSR Register
02D0 2030 - 02D0 203C	-	Reserved
02D0 2040	RIO_SP0_ERR_DET	RapidIO Port 0 Error Detect CSR Register
02D0 2044	RIO_SP0_RATE_EN	RapidIO Port 0 Error Enable CSR Register
02D0 2048	RIO_SP0_ERR_ATTR_CAPT_DBG0	RapidIO Port 0 Attributes Error Capture CSR Register
02D0 204C	RIO_SP0_ERR_CAPT_0_DBG1	RapidIO Port 0 Packet/Control Symbol Error Capture CSR0 Register
02D0 2050	RIO_SP0_ERR_CAPT_1_DBG2	RapidIO Port 0 Packet/Control Symbol Error Capture CSR1 Register
02D0 2054	RIO_SP0_ERR_CAPT_2_DBG3	RapidIO Port 0 Packet/Control Symbol Error Capture CSR2 Register
02D0 2058	RIO_SP0_ERR_CAPT_3_DBG4	RapidIO Port 0 Packet/Control Symbol Error Capture CSR3 Register
02D0 205C - 02D0 2064	-	Reserved

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D0 2068	RIO_SP0_ERR_RATE	RapidIO Port 0 Error Rate CSR Register
02D0 206C	RIO_SP0_ERR_THRESH	RapidIO Port 0 Error Rate Threshold CSR Register
02D0 2070 - 02D0 207C	-	Reserved
02D0 2080	RIO_SP1_ERR_DET	RapidIO Port 1 Error Detect CSR Register
02D0 2084	RIO_SP1_RATE_EN	RapidIO Port 1 Error Enable CSR Register
02D0 2088	RIO_SP1_ERR_ATTR_CAPT	RapidIO Port 1 Attributes Error Capture CSR Register
02D0 208C	RIO_SP1_ERR_CAPT_0	RapidIO Port 1 Packet/Control Symbol Error Capture CSR0 Register
02D0 2090	RIO_SP1_ERR_CAPT_1	RapidIO Port 1 Packet/Control Symbol Error Capture CSR1 Register
02D0 2094	RIO_SP1_ERR_CAPT_2	RapidIO Port 1 Packet/Control Symbol Error Capture CSR2 Register
02D0 2098	RIO_SP1_ERR_CAPT_3	RapidIO Port 1 Packet/Control Symbol Error Capture CSR3 Register
02D0 209C - 02D0 20A4	-	Reserved
02D0 20A8	RIO_SP1_ERR_RATE	RapidIO Port 1 Error Rate CSR Register
02D0 20AC	RIO_SP1_ERR_THRESH	RapidIO Port 1 Error Rate Threshold CSR Register
02D0 20B0 - 02D0 20BC	-	Reserved
02D0 20C0	RIO_SP2_ERR_DET	RapidIO Port 2 Error Detect CSR Register
02D0 20C4	RIO_SP2_RATE_EN	RapidIO Port 2 Error Enable CSR Register
02D0 20C8	RIO_SP2_ERR_ATTR_CAPT	RapidIO Port 2 Attributes Error Capture CSR Register
02D0 20CC	RIO_SP2_ERR_CAPT_0	RapidIO Port 2 Packet/Control Symbol Error Capture CSR0 Register
02D0 20D0	RIO_SP2_ERR_CAPT_1	RapidIO Port 2 Packet/Control Symbol Error Capture CSR1 Register
02D0 20D4	RIO_SP2_ERR_CAPT_2	RapidIO Port 2 Packet/Control Symbol Error Capture CSR2 Register
02D0 20D8	RIO_SP2_ERR_CAPT_3	RapidIO Port 2 Packet/Control Symbol Error Capture CSR3 Register
02D0 20DC - 02D0 20E4	-	Reserved
02D0 20E8	RIO_SP2_ERR_RATE	RapidIO Port 2 Error Rate CSR Register
02D0 20EC	RIO_SP3_RATE_EN	RapidIO Port 3 Error Enable CSR Register
02D0 20F0 - 02D0 20FC	-	Reserved
02D0 2100	RIO_SP3_ERR_DET	RapidIO Port 3 Error Detect CSR Register
02D0 2104	RIO_SP3_RATE_EN	RapidIO Port 3 Error Enable CSR Register
02D0 2108	RIO_SP3_ERR_ATTR_CAPT	RapidIO Port 3 Attributes Error Capture CSR Register
02D0 210C	RIO_SP3_ERR_CAPT_0	RapidIO Port 3 Packet/Control Symbol Error Capture CSR0 Register
02D0 2110	RIO_SP3_ERR_CAPT_1	RapidIO Port 3 Packet/Control Symbol Error Capture CSR1 Register
02D0 2114	RIO_SP3_ERR_CAPT_2	RapidIO Port 3 Packet/Control Symbol Error Capture CSR2 Register
02D0 2118	RIO_SP3_ERR_CAPT_3	RapidIO Port 3 Packet/Control Symbol Error Capture CSR3 Register
02D0 211C - 02D0 2124	-	Reserved
02D0 2128	RIO_SP3_ERR_RATE	RapidIO Port 3 Error Rate CSR Register
02D0 212C	RIO_SP3_ERR_THRESH	RapidIO Port 3 Error Rate Threshold CSR Register
02D0 2130 - 02D1 0FFC	-	Reserved
Implementation Registers		
02D1 1000 - 02D1 1FFC	-	Reserved
02D1 2000	RIO_SP_IP_DISCOVERY_TIMER	RapidIO Port IP Discovery Timer in 4x Mode Register
02D0 2004	RIO_SP_IP_MODE	RapidIO Port IP Mode CSR Register
02D1 2008 - 02D1 200C	-	Reserved
02D1 2010	RIO_SP_IP_PW_IN_CAPT0	RapidIO Port-Write-In Capture 0 CSR Register
02D1 2014	RIO_SP_IP_PW_IN_CAPT1	RapidIO Port-Write-In Capture 1 CSR Register
02D1 2018	RIO_SP_IP_PW_IN_CAPT2	RapidIO Port-Write-In Capture 2 CSR Register
02D1 201C	RIO_SP_IP_PW_IN_CAPT3	RapidIO Port-Write-In Capture 3 CSR Register
02D1 2020 - 02D1 3FFC	-	Reserved

Table 6-25. RapidIO Control Registers (continued)

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02D1 4000	RIO_SP0_RST_OPT	RapidIO Port 0 Reset Option CSR Register
02D1 4004	RIO_SP0_CTL_INDEP	RapidIO Port 0 Control Independent Register
02D1 4008	RIO_SP0_SILENCE_TIMER	RapidIO Port 0 Silence Timer Register
02D1 400C	RIO_SP0_MULT_EVNT_CS	RapidIO Port 0 Multicast-Event Control Symbol Request Register
02D1 4010	-	Reserved
02D1 4014	RIO_SP0_CS_TX	RapidIO Port 0 Control Symbol Transmit Register
02D1 4018 - 02D1 40FC	-	Reserved
02D1 4100	RIO_SP1_RST_OPT	RapidIO Port 1 Reset Option CSR Register
02D1 4104	RIO_SP1_CTL_INDEP	RapidIO Port 1 Control Independent Register
02D1 4108	RIO_SP1_SILENCE_TIMER	RapidIO Port 1 Silence Timer Register
02D1 410C	RIO_SP1_MULT_EVNT_CS	RapidIO Port 1 Multicast-Event Control Symbol Request Register
02D1 4110	-	Reserved
02D1 4114	RIO_SP1_CS_TX	RapidIO Port 1 Control Symbol Transmit Register
02D1 4118 - 02D1 41FC	-	Reserved
02D1 4200	RIO_SP2_RST_OPT	RapidIO Port 2 Reset Option CSR Register
02D1 4204	RIO_SP2_CTL_INDEP	RapidIO Port 2 Control Independent Register
02D1 4208	RIO_SP2_SILENCE_TIMER	RapidIO Port 2 Silence Timer Register
02D1 420C	RIO_SP2_MULT_EVNT_CS	RapidIO Port 2 Multicast-Event Control Symbol Request Register
02D1 4210	-	Reserved
02D1 4214	RIO_SP2_CS_TX	RapidIO Port 2 Control Symbol Transmit Register
02D1 4218 - 02D1 42FC	-	Reserved
02D1 4300	RIO_SP3_RST_OPT	RapidIO Port 3 Reset Option CSR Register
02D1 4304	RIO_SP3_CTL_INDEP	RapidIO Port 3 Control Independent Register
02D1 4308	RIO_SP3_SILENCE_TIMER	RapidIO Port 3 Silence Timer Register
02D1 430C	RIO_SP3_MULT_EVNT_CS	RapidIO Port 3 Multicast-Event Control Symbol Request Register
02D1 4310	-	Reserved
02D1 4314	RIO_SP3_CS_TX	RapidIO Port 3 Control Symbol Transmit Register
02D1 4318 - 02D2 0FFF	-	Reserved
02D2 1000 - 02DF FFFF	-	Reserved

6.25.3 Serial RIO Electrical Data/Timing

TI only supports board designs that follow the board design guidelines outlined in the *TBD* application report (literature number SPRAATBD).

6.26 General-Purpose Input/Output (GPIO)

6.26.1 GPIO Device-Specific Information

On the C6455 the GPIO peripheral pins GP[TBD:TBD] are muxed with the UTOPIA, PCI, and McBSP1 peripheral pins and the SYSCLK3 signal. For more detailed information on device/peripheral configuration and the C6455 device pin muxing, see the Device Configurations section of this data sheet.

6.26.2 GPIO Peripheral Register Description(s)

Table 6-26. GPIO Registers

HEX ADDRESS RANGE	ACRONYM	REGISTER NAME
02B0 0000	PID	GPIO peripheral identification register [value: 0xTBD]
02B0 0004	PCR	GPIO peripheral control register
02B0 0008	GPIO_BINTEN	GPIO interrupt per bank enable register
02B0 000C	-	Reserved
02B0 0010	GPIO_DIR	GPIO direction register
02B0 0014	GPIO_OUT_DATA	GPIO output data register
02B0 0018	GPIO_SET_DATA	GPIO set data register
02B0 001C	GPIO_CLR_DATA	GPIO clear data register
02B0 0020	GPIO_IN_DATA	GPIO input data register
02B0 0024	GPIO_RIS_TRIG	GPIO rising edge interrupt register
02B0 0028	GPIO_FAL_TRIG	GPIO falling edge interrupt register
02B0 002C	GPIO_INSTAT	GPIO interrupt status register
02B0 0030 - 02B0 008C	-	Reserved
02B0 0090 - 02B0 00FF	-	Reserved
02B0 0100 - 02B0 3FFF	-	Reserved

6.26.3 GPIO Electrical Data/Timing

6.27 IEEE 1149.1 JTAG

The JTAG interface is used for BSDL testing and emulation of the DSP device.

6.27.1 JTAG Device-Specific Information

6.27.1.1 IEEE 1149.1 JTAG Compatibility Statement

For maximum reliability, the C6455 DSP includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the DSP's internal emulation logic will always be properly initialized.

6.27.2 JTAG Peripheral Register Description(s)

6.27.3 JTAG Electrical Data/Timing

7 Mechanical Data

7.1 Thermal Data

The following table(s) show the thermal resistance characteristics for the PBGA - ZTZ mechanical package.

Table 7-1. Thermal Resistance Characteristics (S-PBGA Package) [ZTZ]

NO		°C/W	Air Flow (m/s ⁽¹⁾)
1	R θ_{JC} Junction-to-case	1.45	N/A
2	R θ_{JB} Junction-to-board	8.34	N/A
3	R θ_{JA} Junction-to-free air	16.1	0.00
4		13.0	1.0
5		11.9	2.0
6		10.7	3.0
7	Psi $_{JT}$ Junction-to-package top	0.37	0.00
		0.89	1.0
		1.01	1.5
		1.17	3.00
8	Psi $_{JB}$ Junction-to-board	7.6	0.00
		6.7	1.0
		6.4	1.5
		5.8	3.00

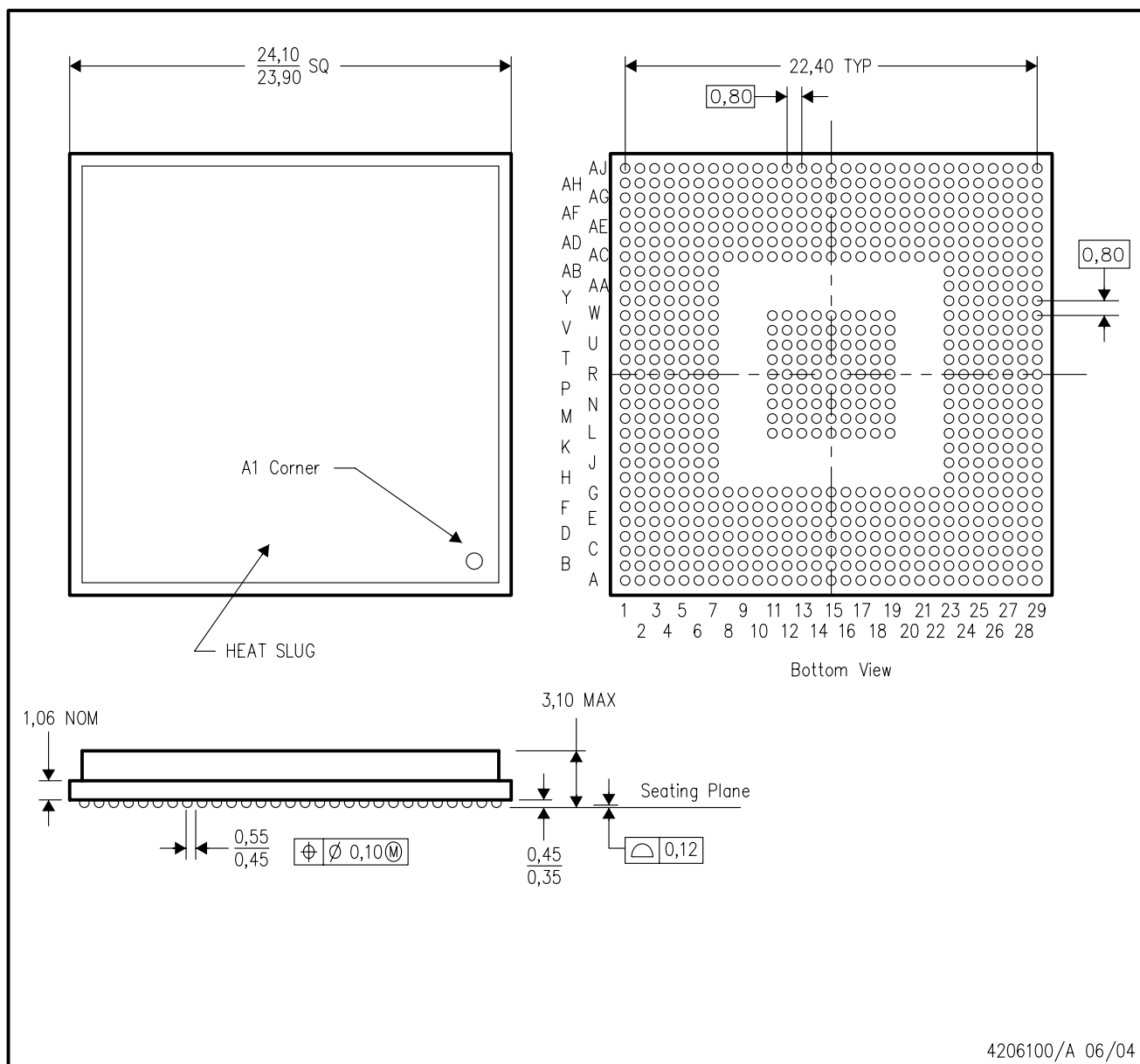
(1) m/s = meters per second

7.2 Packaging Information

The following packaging information and addendum reflect the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

ZTZ (S-PBGA-N697)

PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Thermally enhanced plastic package with heat slug (HSL).
 - Flip chip application only.
 - This package is lead-free.

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