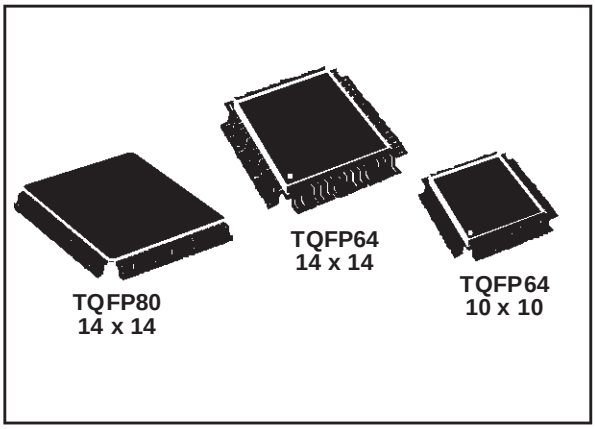
ST72521M/R/AR

8-BIT MCU WITH NESTED INTERRUPTS, FLASH, 10-BIT ADC, FIVE TIMERS, SPI, SCI, I²C, CAN INTERFACE

DATA BRIEFING

- **Memories**
  - 32K to 60K dual voltage High Density Flash (HDFlash) or ROM with read-out protection capability. In-Application Programming and In-Circuit Programming for HDFlash devices
  - 1K to 2K RAM
- **Cloc anced reset system**
  - Enhanced low voltage supervisor (LVD) for main supply and auxiliary voltage detector (AVD) with interrupt capability
  - Clock sources: crystal/ceramic resonator oscillators, internal or external RC oscillator, clock security system and bypass for external clock
  - PLL for 2x frequency multiplication
  - Four power saving modes: Halt, Active-Halt, Wait and Slow
- **Interrupt Management**
  - Nested interrupt controller
  - 14 interrupt vectors plus TRAP and RESET
  - TLI dedicated top level interrupt pin
  - 15 external interrupt lines (on 4 vectors)
- **Up to 64 I/O Ports**
  - 48 multifunctional bidirectional I/O lines
  - 34 alternate function lines
  - 16 high sink outputs
- **5 Timers**
  - Main Clock Controller with: Real time base, Beep and Clock-out capabilities
  - Configurable watchdog timer
  - Two 16-bit timers with: 2 input captures, 2 output compares, external clock input on one timer, PWM and pulse generator modes
  - 8-bit PWM Auto-Reload timer with: 2 input captures, 4 PWM outputs, output compare and time base interrupt, external clock with event detector



- **4 Communications Interfaces**
  - SPI synchronous serial interface
  - SCI asynchronous serial interface (LIN compatible)
  - I²C multimaster interface
  - CAN interface (2.0B Passive)
- **Analog peripheral**
  - 10-bit ADC with 16 input pins
- **Instruction Set**
  - 8-bit Data Manipulation
  - 63 Basic Instructions
  - 17 main Addressing Modes
  - 8 x 8 Unsigned Multiply Instruction
  - True Bit Manipulation
- **Development Tools**
  - Full hardware/software development package
  - In-Circuit Testing capability

Device Summary

Features	ST72(F)521(M/R/AR)9	ST72521(M/R/AR)7	ST72(F)521(R/AR)6
Program memory - bytes	60K	48K	32K
RAM (stack) - bytes	2048 (256)	1536 (256)	1024 (256)
Operating Voltage	3.8V to 5.5V		
Temp. Range (ROM)	0°C to 70°C / -10°C to +85 °C / -40°C to +85 °C / -40°C to +105°C / -40°C to +125°C		
Temp. Range (Flash)	-40°C to +85 °C / -40°C to +125°C	N/A	-40°C to +125 °C
Package	TQFP80 14x14 (M), TQFP64 14x14 (R), TQFP64 10x10 (AR)		TQFP64 14x14 (R), TQFP64 10x10 (AR)

Rev. 1.5

1 INTRODUCTION

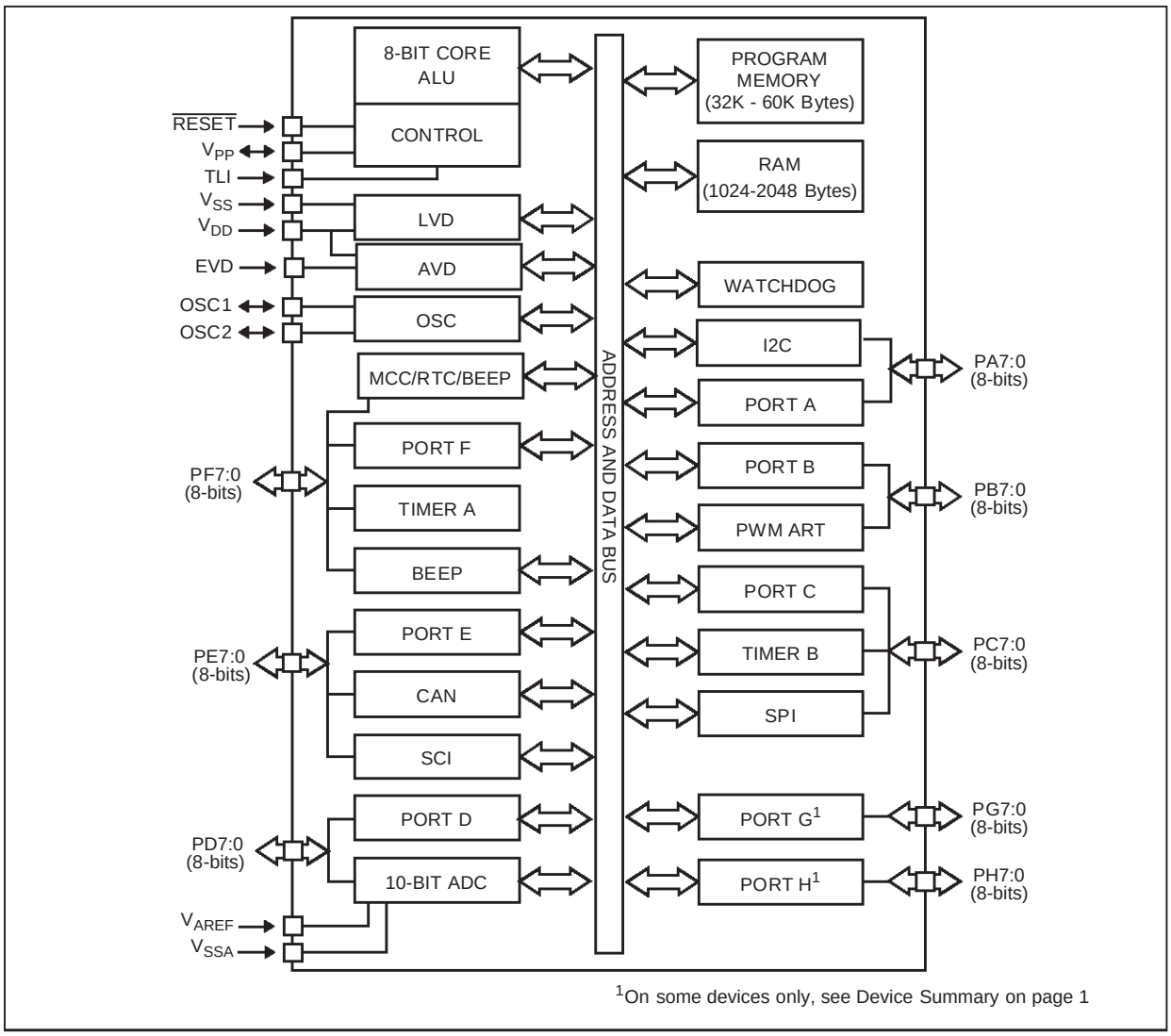
The ST72521(A)R and ST72521M devices are members of the ST7 microcontroller family designed for mid-range applications with a CAN bus interface (Controller Area Network).

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with FLASH or ROM program memory.

Under software control, all devices can be placed in WAIT, SLOW, ACTIVE-HALT or HALT mode, reducing power consumption when the application is in idle or stand-by state.

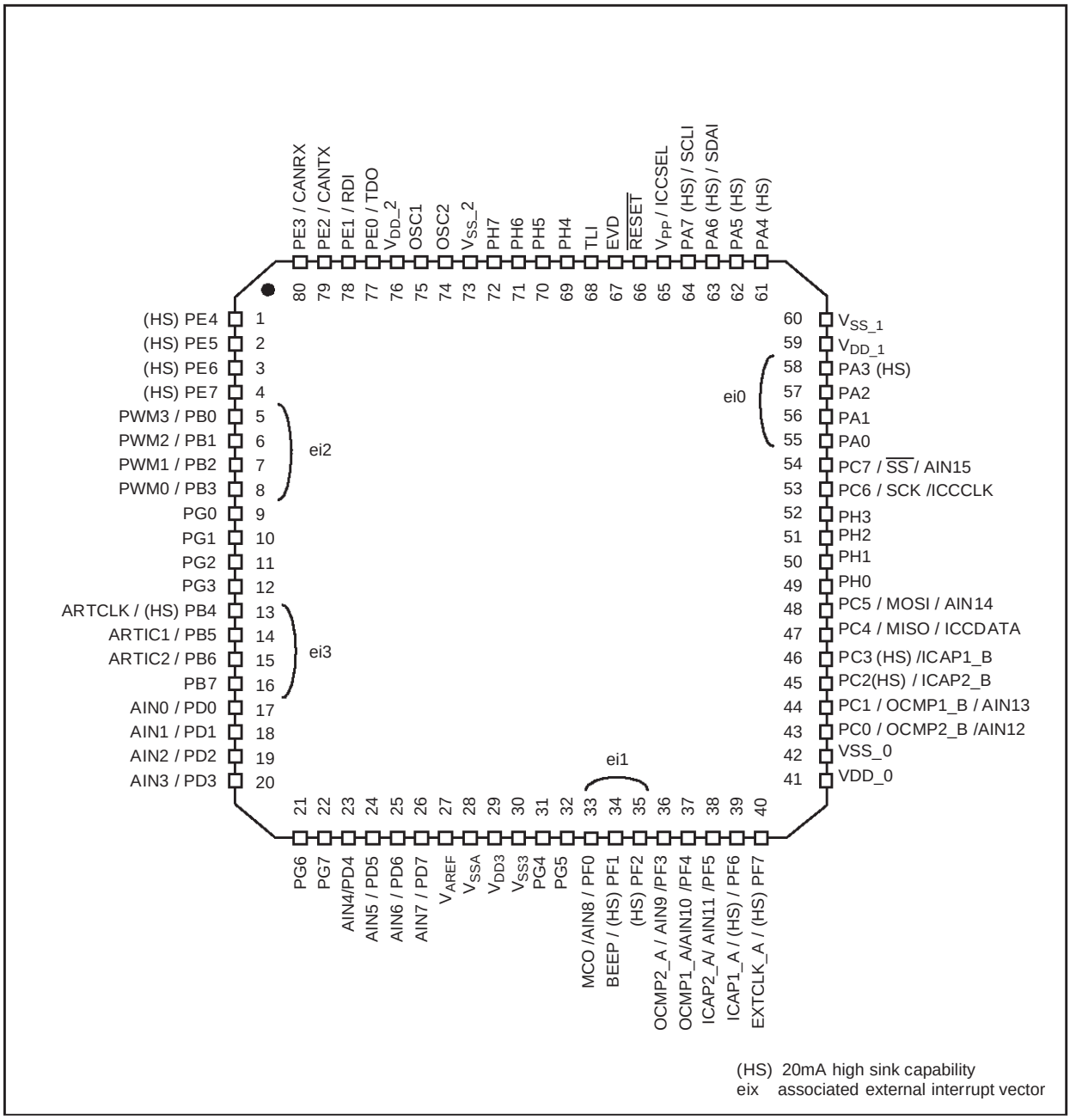
The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Figure 1. Device Block Diagram



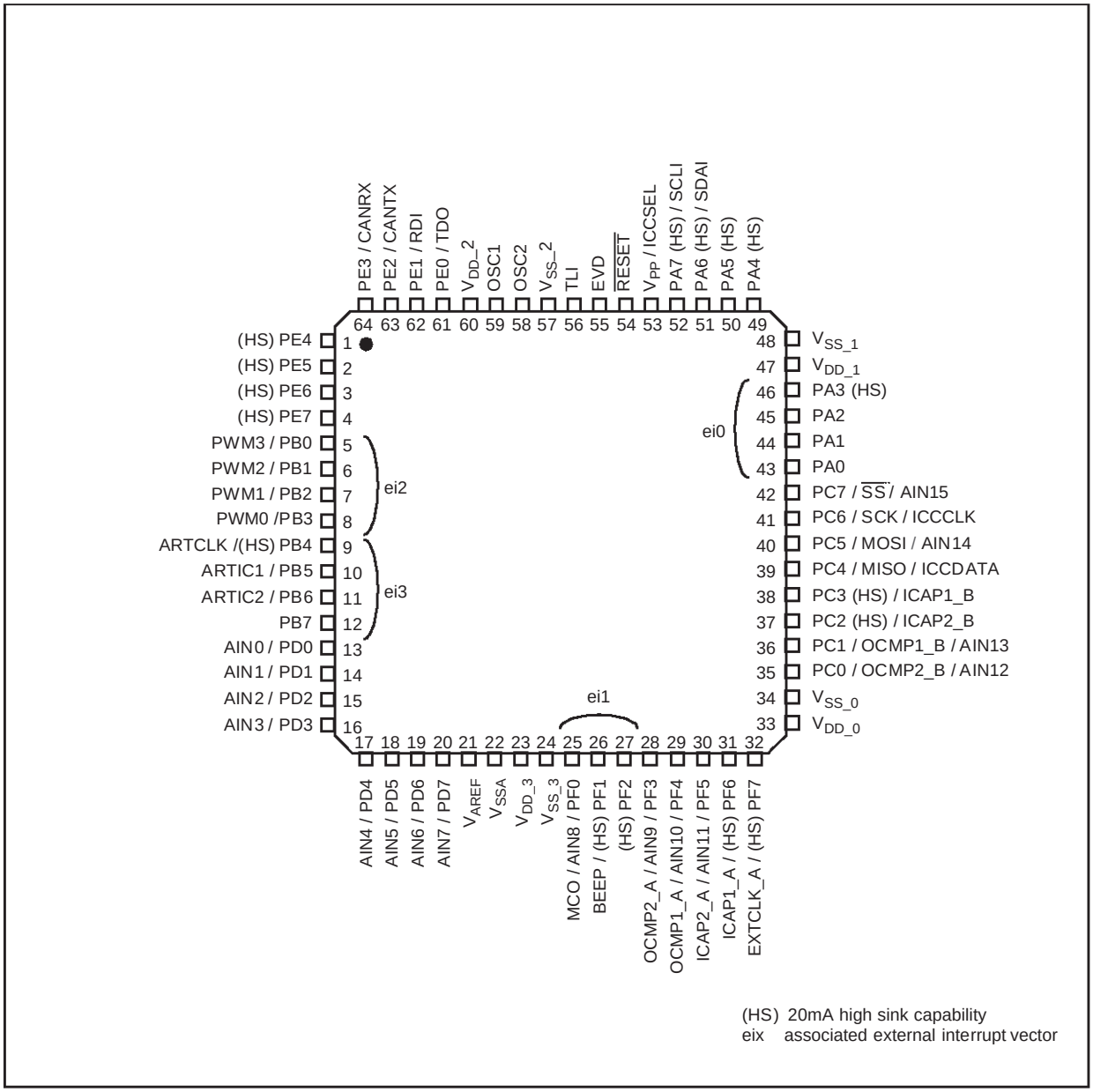
2 PIN DESCRIPTION

Figure 2. 80-Pin TQFP 14x14 Package Pinout



PIN DESCRIPTION (Cont'd)

Figure 3. 64-Pin TQFP 14x14 and 10x10 Package Pinout



PIN DESCRIPTION (Cont'd)

Legend / Abbreviations for Table 1**:**

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C = CMOS $0.3V_{DD}/0.7V_{DD}$
C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger
T_T= TTL 0.8V / 2V with Schmitt trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog

– Output: OD = open drain [2], PP = push-pull

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin n°		Pin Name	Type	Level		Port						Main function (after reset)	Alternate function
						Input				Output			
TQFP80	TQFP64			Input	Output	float	wpu	int	ana	OD	PP		
1	1	PE4 (HS)	I/O	C_T	HS	**X**	X			X	X	Port E4	
2	2	PE5 (HS)	I/O	C_T	HS	**X**	X			X	X	Port E5	
3	3	PE6 (HS)	I/O	C_T	HS	**X**	X			X	X	Port E6	
4	4	PE7 (HS)	I/O	C_T	HS	**X**	X			X	X	Port E7	
5	5	PB0/PWM3	I/O	C_T		**X**	ei2			X	X	Port B0	PWM Output 3
6	6	PB1/PWM2	I/O	C_T		**X**	ei2			X	X	Port B1	PWM Output 2
7	7	PB2/PWM1	I/O	C_T		**X**	ei2			X	X	Port B2	PWM Output 1
8	8	PB3/PWM0	I/O	C_T		**X**		ei2		X	X	Port B3	PWM Output 0
9	-	PG0	I/O	T_T		**X**	X			X	X	Port G0	
10	-	PG1	I/O	T_T		**X**	X			X	X	Port G1	
11	-	PG2	I/O	T_T		**X**	X			X	X	Port G2	
12	-	PG3	I/O	T_T		**X**	X			X	X	Port G3	
13	9	PB4 (HS)/ARTCLK	I/O	C_T	HS	**X**	ei3			X	X	Port B4	PWM-ART External Clock
14	10	PB5/ARTIC1	I/O	C_T		**X**	ei3			X	X	Port B5	PWM-ART Input Capture 1
15	11	PB6/ARTIC2	I/O	C_T		**X**	ei3			X	X	Port B6	PWM-ART Input Capture 2
16	12	PB7	I/O	C_T		**X**		ei3		X	X	Port B7	
17	13	PD0 /AIN0	I/O	C_T		**X**	X		X	X	X	Port D0	ADC Analog Input 0
18	14	PD1/AIN1	I/O	C_T		**X**	X		X	X	X	Port D1	ADC Analog Input 1
19	15	PD2/AIN2	I/O	C_T		**X**	X		X	X	X	Port D2	ADC Analog Input 2
20	16	PD3/AIN3	I/O	C_T		**X**	X		X	X	X	Port D3	ADC Analog Input 3
21	-	PG6	I/O	T_T		**X**	X			X	X	Port G6	
22	-	PG7	I/O	T_T		**X**	X			X	X	Port G7	
23	17	PD4/AIN4	I/O	C_T		**X**	X		X	X	X	Port D4	ADC Analog Input 4
24	18	PD5/AIN5	I/O	C_T		**X**	X		X	X	X	Port D5	ADC Analog Input 5
25	19	PD6/AIN6	I/O	C_T		**X**	X		X	X	X	Port D6	ADC Analog Input 6
26	20	PD7/AIN7	I/O	C_T		**X**	X		X	X	X	Port D7	ADC Analog Input 7

Pin n°		Pin Name	Type	Level		Port						Main function (after reset)	Alternate function	
						Input				Output				
TQFP80	TQFP64			Input	Output	float	wpu	int	ana	OD	PP			
27	21	V_{AREF}	I									Analog Reference Voltage for ADC		
28	22	V_{SSA}	S									Analog Ground Voltage		
29	23	V_{DD_3}	S									Digital Main Supply Voltage		
30	24	V_{SS_3}	S									Digital Ground Voltage		
31	-	PG4	I/O	T_T		**X**	X			X	X	Port G4		
32	-	PG5	I/O	T_T		**X**	X			X	X	Port G5		
33	25	PF0/MCO/AIN8	I/O	C_T		**X**	ei1			X	X	Port F0	Main clock out (f_{OSC}/2)	ADC Analog Input 8
34	26	PF1 (HS)/BEEP	I/O	C_T	HS	**X**	ei1			X	X	Port F1	Beep signal output	
35	27	PF2 (HS)	I/O	C_T	HS	**X**		ei1		X	X	Port F2		
36	28	PF3/OCMP2_A/AIN9	I/O	C_T		**X**	X			X	X	Port F3	Timer A Output Compare 2	ADC Analog Input 9
37	29	PF4/OCMP1_A/AIN10	I/O	C_T		**X**	X			X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
38	30	PF5/ICAP2_A/AIN11	I/O	C_T		**X**	X			X	X	Port F5	Timer A Input Capture 2	ADC Analog Input 11
39	31	PF6 (HS)/ICAP1_A	I/O	C_T	HS	**X**	X			X	X	Port F6	Timer A Input Capture 1	
40	32	PF7 (HS)/EXTCLK_A	I/O	C_T	HS	**X**	X			X	X	Port F7	Timer A External Clock Source	
41	33	V_{DD_0}	S									Digital Main Supply Voltage		
42	34	V_{SS_0}	S									Digital Ground Voltage		
43	35	PC0/OCMP2_B/AIN12	I/O	C_T		**X**	X			X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
44	36	PC1/OCMP1_B/AIN13	I/O	C_T		**X**	X			X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13
45	37	PC2 (HS)/ICAP2_B	I/O	C_T	HS	**X**	X			X	X	Port C2	Timer B Input Capture 2	
46	38	PC3 (HS)/ICAP1_B	I/O	C_T	HS	**X**	X			X	X	Port C3	Timer B Input Capture 1	
47	39	PC4/MISO/ICCDATA	I/O	C_T		**X**	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
48	40	PC5/MOSI/AIN14	I/O	C_T		**X**	X			X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14
49	-	PH0	I/O	T_T		**X**	X			X	X	Port H0		
50	-	PH1	I/O	T_T		**X**	X			X	X	Port H1		
51	-	PH2	I/O	T_T		**X**	X			X	X	Port H2		
52	-	PH3	I/O	T_T		**X**	X			X	X	Port H3		
53	41	PC6/SCK/ICCCLK	I/O	C_T		**X**	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output

Pin n°		Pin Name	Type	Level		Port						Main function (after reset)	Alternate function	
						Input				Output				
TQFP80	TQFP64			Input	Output	float	wpu	int	ana	OD	PP			
54	42	PC7/$\overline{SS}$/AIN15	I/O	C_T		**X**	X			X	X	Port C7	SPI Slave Select (active low)	ADC Analog Input 15
55	43	PA0	I/O	C_T		**X**	ei0			X	X	Port A0		
56	44	PA1	I/O	C_T		**X**	ei0			X	X	Port A1		
57	45	PA2	I/O	C_T		**X**	ei0			X	X	Port A2		
58	46	PA3 (HS)	I/O	C_T	HS	**X**		ei0		X	X	Port A3		
59	47	V_{DD_1}	S									Digital Main Supply Voltage		
60	48	V_{SS_1}	S									Digital Ground Voltage		
61	49	PA4 (HS)	I/O	C_T	HS	**X**	X			X	X	Port A4		
62	50	PA5 (HS)	I/O	C_T	HS	**X**	X			X	X	Port A5		
63	51	PA6 (HS)/SDAI	I/O	C_T	HS	**X**				T		Port A6	I^2C Data [1]	
64	52	PA7 (HS)/SCLI	I/O	C_T	HS	**X**				T		Port A7	I^2C Clock [1]	
65	53	V_{PP}/ ICCSEL	I									Must be tied low. In flash programming mode, this pin acts as the programming voltage input V_{PP}. High voltage must not be applied to ROM devices		
66	54	$\overline{RESET}$	I/O	C_T								Top priority non maskable interrupt.		
67	55	EVD										External voltage detector		
68	56	TLI	I	C_T		**X**		X				Top level interrupt input pin		
69	-	PH4	I/O	T_T		**X**	X			X	X	Port H4		
70	-	PH5	I/O	T_T		**X**	X			X	X	Port H5		
71	-	PH6	I/O	T_T		**X**	X			X	X	Port H6		
72	-	PH7	I/O	T_T		**X**	X			X	X	Port H7		
73	57	V_{SS_2}	S									Digital Ground Voltage		
74	58	OSC2[3]	I/O									Resonator oscillator inverter output or capacitor input for RC oscillator		
75	59	OSC1[3]	I									External clock input or Resonator oscillator inverter input or resistor input for RC oscillator		
76	60	V_{DD_2}	S									Digital Main Supply Voltage		
77	61	PE0/TDO	I/O	C_T		**X**	X			X	X	Port E0	SCI Transmit Data Out	
78	62	PE1/RDI	I/O	C_T		**X**	X			X	X	Port E1	SCI Receive Data In	
79	63	PE2/CANTX	I/O	C_T			**X**					Port E2	CAN Transmit Data Output	
80	64	PE3/CANRX	I/O	C_T		**X**	X			X	X	Port E3	CAN Receive Data Input	

Notes:

1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

2. In the open drain output column, “T” defines a true open drain I/O (P-Buffer and protection diode to V_{DD}

are not implemented).

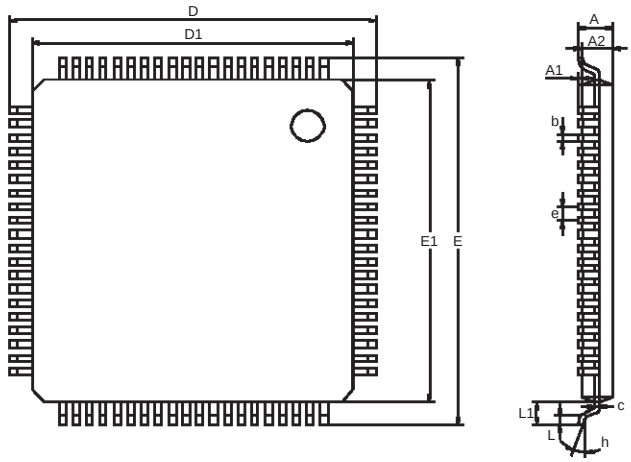
3. OSC1 and OSC2 pins connect a crystal/ceramic resonator, an RC oscillator, or an external source to the on-chip oscillator;

4. On the chip, each I/O port has 8 pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption.

3 PACKAGE CHARACTERISTICS

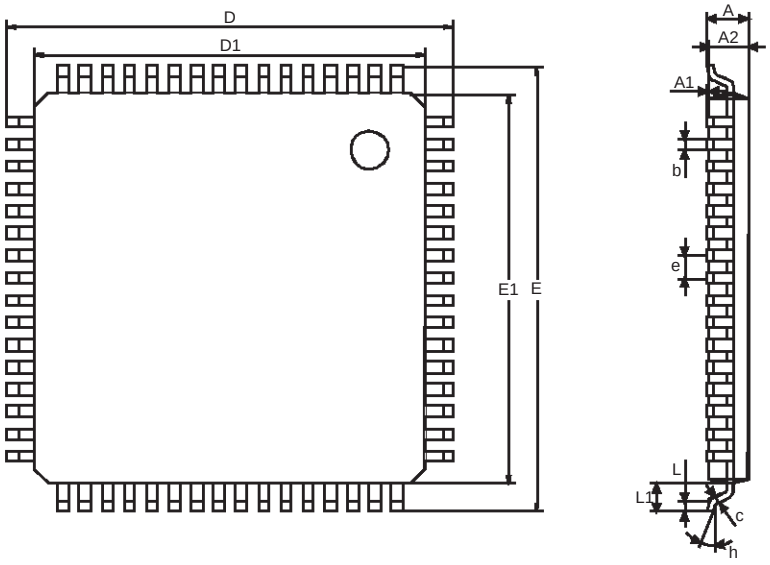
3.1 PACKAGE MECHANICAL DATA

Figure 4. 80-Pin Thin Quad Flat Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.65			0.026	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	80					

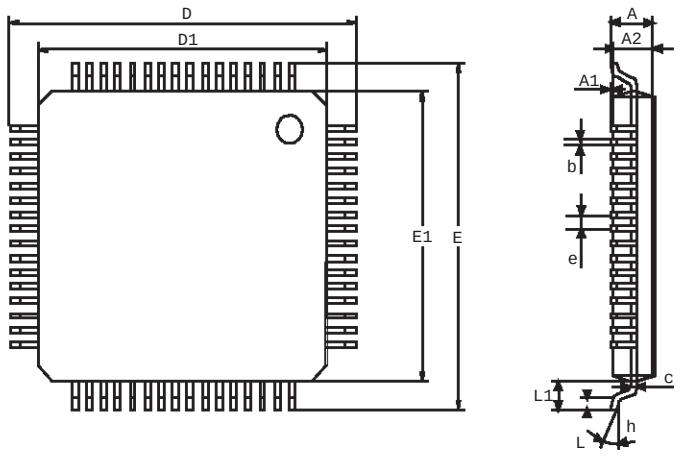
Figure 5. 64-Pin Thin Quad Flat Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.012	0.015	0.018
c	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.80			0.031	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64					

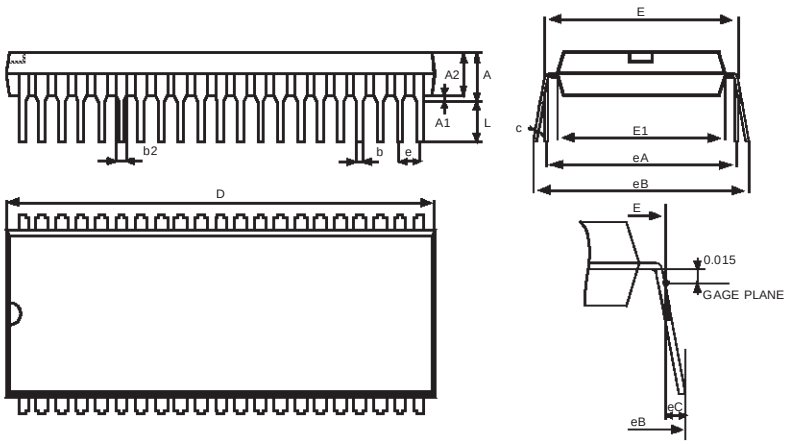
PACKAGE MECHANICAL DATA (Cont'd)

Figure 6. 64-Pin Thin Quad Flat Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64					

Figure 7. 42-Pin Plastic Dual In-Line Package, Shrink 600-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
b	0.38	0.46	0.56	0.015	0.018	0.022
b2	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.009	0.010	0.015
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.600		0.630
E1	12.70	13.72	14.48	0.500	0.540	0.570
e		1.78			0.070	
eA		15.24			0.600	
eB			18.54			0.730
eC			1.52	0.000		0.060
L	2.54	3.30	3.56	0.100	0.130	0.140
	Number of Pins					
N	42					

Notes: