QL58x2 Enhanced QuickPCI Family Data Sheet

33/66 MHz/32-bit PCI Master/Target with Embedded Programmable Logic, Embedded Computational Units, and Dual Port SRAM

Device Highlights

High Performance PCI Controller

- 33/66 MHz 32-bit PCI Master/Target
- Zero-wait state PCI Master provides up to 264 MBps transfer rates
- Zero-wait-state PCI Target Write/One-wait-state PCI Target Read interface
- Supports all PCI commands, including configuration and MWI
- Supports fully-customizable byte enable for master channels
- Target interface supports retry, disconnect with/without data transfer, and target abort
- Fully programmable back-end interface
- Independent PCI bus (33/66 MHz) and local bus (up to 160 MHz) clocks
- Fully customizable PCI Configuration Space
- Configurable FIFOs with depths up to 256 words
- Reference design with driver code (Win 95/98/2000/NT 4.0) available
- PCI v2.3 compliant
- Supports Type 0 Configuration Cycles in Target mode
- 3.3 V PCI signaling
- 1.8 V supply voltage
- 484-ball PBGA, 280-ball LFBGA, 208-pin PQFP, 196-ball TFBGA, and 144-pin TQFP packages
- Supports Extendable PCI functionality
- Unlimited/Continuous Burst Transfers supported

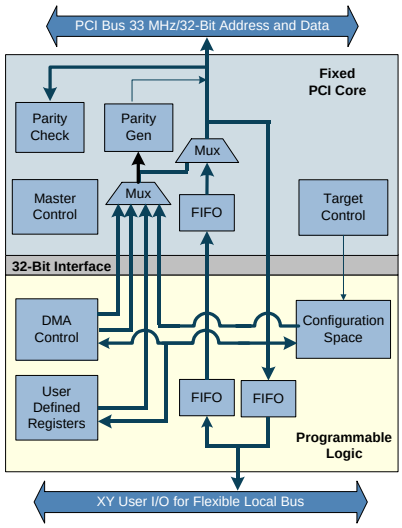
Extendable PCI Functionality

- Support for Configuration Space from 0 × 40 to 0 × 3FF
- PCI v2.3 Power Management Spec. compatible
- Multi-function, expanded capabilities, and expansion ROM capable
- PCI v2.3 Vital Product Data (VPD) configuration support

Flexible Programmable Logic

- Up to 1,348 logic cells
- Up to 50,688 RAM bits
- Up to 262 I/O pins
- All back-end interface and glue-logic can be implemented on chip
- Six 32-bit busses interface between the PCI Controller and the Programmable Logic
- Up to twenty-two 2,304 bit dual-port high performance SRAM blocks
- Up to 3,482 flip-flops available

Figure 1: QL58x2 Block Diagram



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Architecture Overview

The QL58x2 device family of QuickPCI Embedded Standard Products (ESPs) provides a complete and customizable PCI interface solution combined with programmable logic. Since the QL58x2 devices provide optimized pre-verified PCI cores, the burden of PCI timing closure and PCI protocol compliance has been eliminated and allows for the maximum 32-bit PCI bus bandwidth (264 MBps).

The programmable logic portion of this family contains up to 1,348 QuickLogic Logic Cells and up to 22 QuickLogic Dual-Port RAM Blocks. These configurable RAM blocks can be configured in many width/depth combinations. They can also be combined with logic cells to form FIFOs, or be initialized via Serial EEPROM on power-up and used as ROMs.

The QL58x2 device meets PCI 2.3 electrical and timing specifications and has been fully hardware-tested. The QL58x2 device features 1.8 V operation with multi-volt compatible I/Os. The device can easily operate in 3 V embedded systems and is fully compatible with 3.3 V applications.

PCI Controller

The PCI Controller is a 33/66 MHz 32-bit PCI 2.3 compliant Master/Target Controller capable of infinite length Master Write and Read transactions at zero wait states (264 MBps).

The Master will never insert wait states during transfers, so data is supplied or received by FIFOs that can be configured in the programmable region of the device. The Master is capable of initiating any type of PCI commands, including configuration cycles and Memory Write and Invalidate (MWI). This enables the QL58x2 device family to act as a PCI host. The Master Controller will most often be operated by a DMA Controller in the programmable region of the device. DMA Controller reference design is available and is included in the Quick*Works*® design software.

The Target interface offers full PCI Configuration Space and flexible target addressing. It supports zero-wait-state target Write and one-wait-state target Read operations. It also supports retry, disconnect with/without data transfer, and target abort requested by the back end. Any number of 32-bit BARs may be configured as either memory or I/O space. All required and optional PCI 2.3 Configuration Space registers can be implemented within the programmable region of the device. A reference design of a Target Configuration and Addressing module is available and is included in the Quick*Works* design software.

The interface ports are divided into a set of ports for master transactions and a set for target transactions. The Master DMA controller and Target Configuration Space and Address Decoding are done in the programmable logic region of the device. These functions are not timing critical, so leaving these elements in the programmable region allows the greatest degree of flexibility to the designer. Reference DMA controller, Configuration Space, and Address Decoding blocks are readily available so that the design cycle can be minimized.

Table 1 shows several commonly implemented IP cores in the programmable logic portion of the Master/Target Controller device. Their respective logic cell utilization and performance information are shown clearly for easy reference. Notice that the Configuration Space/Address Decoding and DMA Controller IP cores are labelled as essential IP cores. These IP blocks are necessary for the Master/Target Controller to be fully functional. The optional IP cores are common interface IP cores made available so that designers may implement according to their design requirements. These optional IP cores do not affect the functionality of the Master/Target Controller.

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Table 1: IP Implemented in Programmable Logic

Essential PCI IP Cores	Logic Cells	RAM	Performance
Configuration Space/Address Decoding	110	N/A	33/66 MHz
Optional IP Cores	**Logic Cells**	**RAM**	**Performance**
Async 32x32 FIFO	64	2	210 MHz
Async 128x32 FIFO	88	2	190 MHz
SDRAM Controller	149	N/A	160 MHz
DDR SDRAM Controller	216	N/A	100 MHz
Pulse Width Modulation	20	N/A	303 MHz

Configuration Space and Address Decode

The configuration space is completely customizable in the programmable region of the device.

PCI address and command decoding is performed by logic in the programmable section of the device. This allows support for any size of memory or I/O space for back end logic. It also allows the user to implement any subset of the PCI commands supported by the QL58x2. QuickLogic provides a reference Address Register/Counter and Command Decode block.

DMA Master Target Controller

The customizable DMA controller included with the QuickWorks design software contains the following features:

- Configurable DMA count size for Reads and Writes (up to 30-bits)
- Configurable DMA burst size for PCI (including unlimited/continuous burst)
- Customizable PCI command to use by core
- Customizable Byte Enable signal
- Programmable Arbitration between DMA Read & Write transactions
- DMA Registers may be mapped to any area of Target Memory Space, including:
  - Read Address (32-bit register)
  - Write Address (32-bit register)
  - Read Length (16-bit register) / Write Length (16-bit register)
  - Control and Status (32-bit register, includes 8 bit Burst Length)
- DMA Registers are available to the local design or the PCI bus
- Programmable Interrupt Control to signal end of transfer or other event

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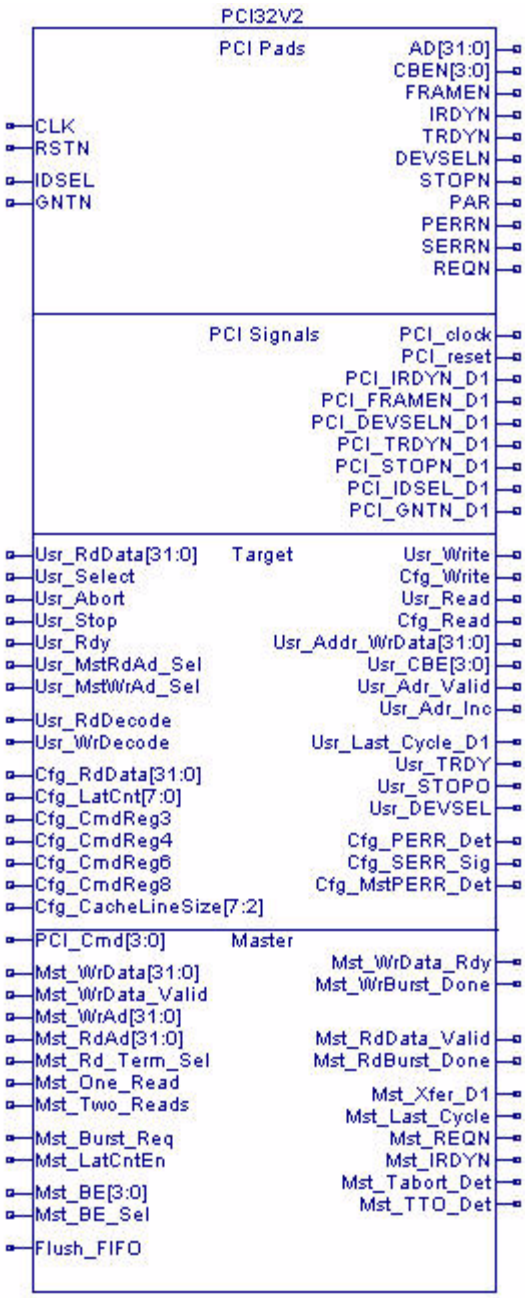
PCI Interface Symbol

Figure 2 shows the graphical interface symbol numbers you have to use in your schematic design in order to attach the local interface programmable logic design to the PCI core. If you are designing with a top-level Verilog or VHDL file you must use a structural instantiation of this PCI32V2 block instead of a graphical symbol.

Figure 2: PCI Interface Symbol



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PCI Master Interface

The internal signals used to interface with the PCI controller in the QL58x2 are listed in **Table 2** along with a description of each signal. The direction of the signal indicates if the signal is an input provided by the local interface (I) or an output provided by the PCI controller (O).

NOTE: Signals that end with the character 'N' should be considered active-low (for example, Mst_IRDYN).

Table 2: PCI Master Interface

Signal	I/O	Description
PCI_cmd[3:0]	I	**PCI command to be used for the master transaction.** This signal must remain unchanged throughout the period when Mst_Burst_Req is active. PCI commands considered as Reads include Interrupt Acknowledge, I/O Read, Memory Read, Configuration Read, Memory Read Multiple, and Memory Read Line. PCI commands considered as Writes include Special Cycle, I/O Write, Memory Write, Configuration Write, Memory Write, and Invalidate.Users should make sure that only valid PCI commands are supplied.
Mst_Burst_Req	I	**Request use of the PCI bus.** When it is active, the core requests the PCI bus and then generates a Master transaction. This signal should be held active until all requested data is transferred on the PCI bus and deactivated in the 2nd clock cycle following the last data transfer on PCI (to avoid being considered as requesting a new transaction).
Mst_WrAd[31:0]	I	**Address for master DMA writes.** This address must be treated as valid from the beginning of a DMA Write until the DMA Write operation is complete. It should be incremented by four bytes each time data is transferred on the PCI bus.
Mst_RdAd[31:0]	I	**Address for master DMA reads.** This address must be treated as valid from the beginning of a DMA read until the DMA Read operation is complete. It should be incremented by four bytes each time data is transferred on the PCI bus.
Mst_WrData[31:0]	I	**Data for master DMA Writes (to PCI bus).**
Mst_BE[3:0]	I	**Byte enables for master DMA Reads and writes.** Active-low.
Mst_WrData_Valid	I	**Data and byte enable valid on Mst_WrData[31:0] (for master Write only) and Mst_BE[3:0] (for both master Read and Write).**
Mst_WrData_Rdy	O	**Data receive acknowledge for Mst_WrData[31:0] (for master Write only) and Mst_BE[3:0] (for both)**.This serves as the PUSH control for the internal FIFO and the POP control for the external FIFO (in FPGA region) which provides data and byte enables to the PCI32 core.
Mst_BE_Sel	I	**Byte enable select for master transactions.** When low, Mst_BE[3:0] should remain constant throughout the entire transfer (when Mst_Burst_Req is active) and it is used for every data phase of the master transaction. When high, Mst_BE[3:0] pushed into internal FIFO (along with data in case of master Write) is used. Should be held constant throughout the transaction.
Mst_WrBurst_Done	O	**Master Write transaction is completed.** Active for only one clock cycle.
Mst_Rd_Term_Sel	I	**Master Read termination mode select when Mst_BE_Sel is high.** When both Mst_BE_Sel and Mst_Rd_Term_Sel are high, Master Read termination happens when the internal FIFO is empty, and Mst_Two_Reads and Mst_One_Read are ignored. When either signal is low, Mst_Two_Reads and Mst_One_Read are used to signal the end of Master Read. Should be held constant throughout the transaction.
Mst_One_Read	I	Signals to the PCI32 core that only one data transfer remains to be read in the burst Read.
Mst_Two_Reads	I	**Two data transfers remain to be read in the burst Read** It is not used for single-data-phase Master Read transactions.
Mst_RdData_Valid	O	**Master Read data valid on Usr_Addr_WrData[31:0].** This serves as the PUSH control for the external FIFO (in FPGA region) that receives data from the PCI32 core.

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Table 2: PCI Master Interface (Continued)

Signal	I/O	Description
Mst_RdBurst_Done	O	**Master Read transaction is completed.** Active for only one clock cycle.
Flush_FIFO	I	**Internal FIFO flush.** FIFO flushed immediately after it is active (synchronized with PCI clock).
Mst_LatCntEn	I	**Enable Latency Counter.** Set to 0 to ignore the Latency Timer in the PCI configuration space (offset 0Ch). For full PCI compliance, this port should be always set to 1.
Mst_Xfer_D1	O	**Data was transferred on the previous PCI clock.** Useful for updating DMA transfer counts on DMA Read operations.
Mst_Last_Cycle	O	**Active during the last data transfer of a master transaction**
Mst_REQN	O	**Copy of the PCI REQN signal generated by QL58x2 as PCI master.** Not usually used in the back-end design.
Mst_IRDYN	O	**Copy of the PCI IRDYN signal generated by QL58x2 as PCI master.** Valid only when QL58x2 is the PCI master. Kept low otherwise. Not usually used in the back-end design.
Mst_Tabort_Det	O	**Target abort detected during master transaction.** This is normally an error condition handled in the DMA controller.
Mst_TTO_Det	O	**Target timeout detected (no response from target).** This is normally an error condition handled in the DMA controller.

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PCI Target Interface

Table 3: PCI Target Interface

Signal	I/O	Description
Usr_Addr_WrData[31:0]	O	**Target address, and target Write data.** During all target accesses, the address is presented on Usr_Addr_WrData[31:0]; at the same time, Usr_Adr_Valid is active. During target Write transactions, this port also presents valid Write data to the PCI configuration space or user logic when Usr_Adr_Inc is active.
Usr_CBE[3:0]	O	**PCI command and byte enables.** During target accesses, the PCI command is presented on Usr_CBE[3:0]; at the same time, Usr_Adr_Valid is active. This port also presents active-low byte enables to the PCI configuration space or user logic.
Usr_Adr_Valid	O	Indicates the beginning of a PCI transaction, and that a target address is valid on Usr_Addr_WrData[31:0] and the PCI command is valid on Usr_CBE[3:0]. When this signal is active, the target address must be latched and decoded to determine if this address belongs to the device's memory or I/O space. Also, the PCI command must be decoded to determine the type of PCI transaction. On subsequent clocks of a target access, this signal is low, indicating that address is NOT present on Usr_Addr_WrData[31:0].
Usr_Adr_Inc	O	Indicates that the target address should be incremented, because the previous data transfer has completed. During burst target accesses, the target address is only presented to the back-end logic at the beginning of the transaction (when Usr_Adr_Valid is active), and must therefore be latched and incremented by four for subsequent data transfers. Note that during target Write transactions, Usr_Adr_Inc indicates valid data on Usr_Addr_WrData[31:0] that must be accepted by the backend logic (regardless of the state of Usr_Rdy). During Read transactions, Usr_Adr_Inc signals to the backend that the PCI core has presented the read data on the PCI bus (TRDYN asserted).
Usr_RdDecode	I	This signal should be the combinatorial decode of the “user read” command from Usr_CBE[3:0]. This command may be mapped from any of the PCI Read commands, such as Memory Read, Memory Read Line, Memory Read Multiple, I/O Read, etc. It is internally gated with Usr_Adr_Valid.
Usr_WrDecode	I	This signal should be the combinatorial decode of the “user write” command from Usr_CBE[3:0]. This command may be mapped from any of the PCI Write commands, such as Memory Write or I/O Write. It is internally gated with Usr_Adr_Valid.
Usr_Select	I	This signal should be driven active when the address on Usr_Addr_WrData[31:0] has been decoded and determined to be within the address space of the device. Usr_Addr_WrData[31:0] must be compared to each of the valid Base Address Registers in the PCI configuration space. Also, this signal must be gated by the Memory Access Enable or I/O Access Enable registers in the PCI configuration space (Command Register bits 1 or 0 at offset 04h). Internally gated with Usr_Adr_Valid.
Usr_Write	O	This signal is active throughout a “user write” transaction, which has been decoded by Usr_WrDecode at the beginning of the transaction. The Write strobe for individual DWORDs of data (on Usr_Addr_WrData[31:0]) during a user Write transaction should be generated by logically ANDing this signal with Usr_Adr_Inc.
Cfg_Write	O	This signal is active throughout a “configuration write” transaction. The Write strobe for individual DWORDs of data (on Usr_Addr_WrData[31:0]) during a configuration Write transaction should be generated by logically ANDing this signal with Usr_Adr_Inc.
Usr_Read	O	This signal is active throughout a “user read” transaction, which has been decoded by Usr_RdDecode at the beginning of the transaction.
Cfg_Read	O	This signal is active throughout a “configuration read” transaction.

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Table 3: PCI Target Interface (Continued)

Signal	I/O	Description
Cfg_RdData[31:0]	I	Data from the PCI configuration registers, required to be presented during PCI configuration reads.
Usr_RdData[31:0]	I	Data from the back-end user logic required to be presented during PCI user reads.
Cfg_CmdReg3	I	Bit 3 from the Command Register in the PCI configuration space (offset 04h). Enable Special Cycle monitoring. If high, the core reports data parity error in Special Cycles through SERRN if Cfg_CmdReg8 is active.
Cfg_CmdReg4	I	Bit 4 from the Command Register in the PCI configuration space (offset 04h). Memory Write and Invalidate (MWI) Enable. If high, the core generates MWI transactions as requested by the backend. Otherwise it uses Memory Write instead even if MWI is requested.
Cfg_CmdReg6	I	Bit 6 from the Command Register in the PCI configuration space (offset 04h). Parity Error Response. If high, the core uses PERRN to report data parity errors. Otherwise it never drives it.
Cfg_CmdReg8	I	Bit 8 from the Command Register in the PCI configuration space (offset 04h). SERRN Enable. If high, the cores uses SERRN to report address parity errors if Cfg_CmdReg6 is high.
Cfg_LatCnt[7:0]	I	8-bit value of the Latency Timer in the PCI configuration space (offset 0Ch).
Usr_MstRdAd_Sel	I	Used when a target Read operation should return the value set on the Mst_RdAd[31:0] pins. This select pin saves on logic which would otherwise need to be used to multiplex Mst_RdAd[31:0] into the Usr_RdData[31:0] bus. When this signal is asserted, the data on Usr_RdData[31:0] is ignored.
Usr_MstWrAd_Sel	I	Used when a target read operation should return the value set on the Mst_WrAd[31:0] pins. This select pin saves on logic which would otherwise need to be used to multiplex Mst_WrAd[31:0] into the Usr_RdData[31:0] bus. When this signal is asserted, the data on Usr_RdData[31:0] is ignored.
Cfg_PERR_Det	O	Parity error detected on the PCI bus. When this signal is active, bit 15 of the Status Register must be set in the PCI configuration space (offset 04h).
Cfg_SERR_Sig	O	System error asserted on the PCI bus. When this signal is active, the Signalled System Error bit, bit 14 of the Status Register, must be set in the PCI configuration space (offset 04h).
Cfg_MstPERR_Det	O	Data parity error detected on the PCI bus by the master. When this signal is active, bit 8 of the Status Register must be set in the PCI configuration space (offset 04h).
Usr_TRDY	O	Inverted copy of the TRDYN signal as driven by the PCI target interface. Valid only within a target access.
Usr_STOPO	O	Inverted copy of the STOPN signal as driven by the PCI target interface. Valid only within a target access.
Usr_DEVSEL	O	Inverted copy of the DEVSELN signal as driven by the PCI target interface. Valid only within a target access.
Usr_Last_Cycle_D1	O	Active one clock cycle after the last data phase (may not with data transfer) occurs on PCI and inactive one clock cycle afterwards.
Usr_Rdy	I	Used to delay (add wait states to) a target PCI transaction when the backend needs additional time to provide data (read) or accept data (write). Subject to PCI latency restrictions.
Usr_Stop	I	Used to prematurely stop a PCI target access on the next PCI clock.
Usr_Abort	I	Used to signal Target Abort on PCI when the backend has fatal errors and is unable to complete a transaction. Rarely used.

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PCI Internal Signals

Table 4: PCI Internal Signals

Signal	I/O	Description
PCI_clock	O	PCI clock.
PCI_reset	O	PCI reset signal.
PCI_IRDYN_D1	O	Copy of the IRDYN signal from the PCI bus, delayed by one clock.
PCI_FRAMEN_D1	O	Copy of the FRAMEN signal from the PCI bus, delayed by one clock.
PCI_DEVSELN_D1	O	Copy of the DEVSELN signal from the PCI bus, delayed by one clock.
PCI_TRDYN_D1	O	Copy of the TRDYN signal from the PCI bus, delayed by one clock.
PCI_STOPN_D1	O	Copy of the STOPN signal from the PCI bus, delayed by one clock.
PCI_IDSEL_D1	O	Copy of the IDSEL signal from the PCI bus, delayed by one clock.

Table 5: QL58x2 Master QuickPCI Family Members

		QL5822	QL5842
Max Gates		188,946	320,640
Logic Cells		450	1,348
Max Flip-Flops		1,172	3,482
Max I/O		95	262
RAM Modules		14	22
RAM Bits		32,256	46,080
PLLs		-	4
ECUs		-	12
Packages	TQFP	144	-
	TFBGA (0.8 mm)	196	-
	PQFP	208	208
	LFBGA (0.8 mm)	280	280
	PBGA (1.0 mm)	-	484

Table 6: Max I/O per Device/Package Combination

Device	144 TQFP	196 TFBGA	208 PQFP	280 LFBGA	484 PBGA
QL5822	52	76	95	115	-
QL5842	-	-	67	115	262

QuickWorks Design Software

The QuickWorks® package provides the most complete ESP and FPGA software solution from design entry to logic synthesis, to place and route, to power calculation, and simulation. The package provides a solution for designers who use third-party tools from Cadence, Mentor, OrCAD, Synopsys, Viewlogic, and other third-party tools for design entry, synthesis, or simulation.

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Process Data

The QL58x2 device family is fabricated on a 0.18 µ, six layer metal CMOS process. The core voltage is 1.8 V and the I/Os are up to 3.3 V drive/tolerant. The QL58x2 device family product line is available in commercial, industrial, and military temperature grades.

Programmable Logic Architectural Overview

The QL58x2 device family logic cell structure is presented in **Figure 3**. This architectural feature addresses today's register-intensive designs.

Table 7: Performance Standard[a]s

Function	Description	Slowest Speed Grade	Fastest Speed Grade
Multiplexer	16:1	2.8 ns	2.4 ns
Parity Tree	24	3.4 ns	2.9 ns
	36	4.6 ns	3.9 ns
Counter	16 bit	275 MHz	328 MHz
	32 bit	250 MHz	300 MHz
Synchronous FIFO	128 x 32	197 MHz	235 MHz
	128 x 64	188 MHz	266 MHz
	256 x 16	208 MHz	248 MHz
Clock-to-Out		6.5 ns	6 ns
System clock		200 MHz	300 MHz

a. Performance standards for worst-case commercial conditions.

The QL58x2 device family logic cell structure presented in **Figure 3** is a dual register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. Both registers share CLK, SET, and RESET inputs. The second register has a two-to-one multiplexer controlling its input. The register can be loaded from the NZ output or directly from a dedicated input.

NOTE: The input PP is not an “input” in the classical sense. It is a static input to the logic cell and selects which path (NZ or PS) is used as an input to the Q2Z register. All other inputs are dynamic and can be connected to multiple routing channels.

The complete logic cell consists of two six-input AND gates, four two-input AND gates, seven two-to-one multiplexers, and two D flip-flops with asynchronous SET and RESET controls. The cell has a fan-in of 30 (including register control lines), fits a wide range of functions with up to 17 simultaneous inputs, and has six outputs (four combinatorial and two registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay while other architectures require two or more levels of delay.

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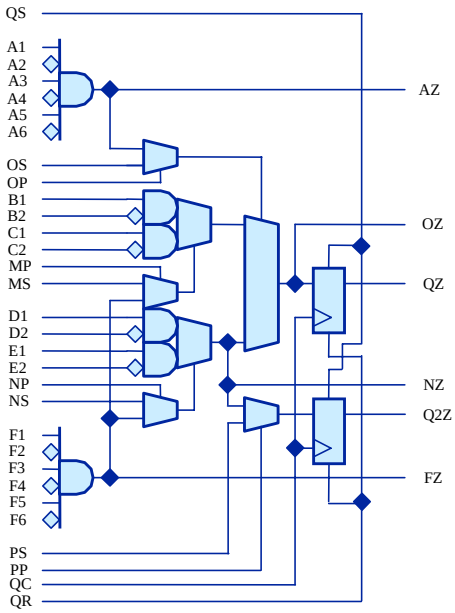
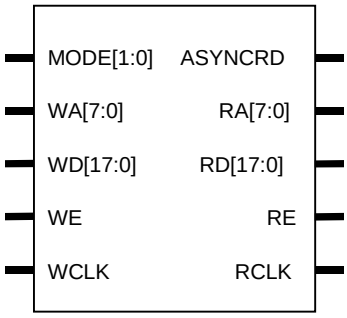
Figure 3: QL58x2 Device Family Logic Cell



RAM Modules

The QL58x2 device family includes up to 24 dual-port 2,304-bit RAM modules for implementing RAM, ROM, and FIFO functions. Each module is user-configurable into two different block organizations and can be cascaded horizontally to increase their effective width, or vertically to increase their effective depth as shown in **Figure 5**.

Figure 4: 2,304-bit RAM Module



The number of RAM modules varies from 4 to 24 blocks for a total of 9.2 K to 55.3 K bits of RAM. Using the two “mode” pins, designers can configure each module into 128 x 18 and 256 x 9. The blocks are also easily cascadable to increase their effective width and/or depth (see **Figure 5**).

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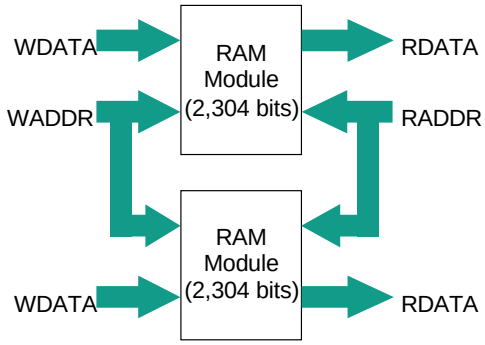
Figure 5: Cascaded RAM Modules



The RAM modules are dual-port, with completely independent READ and WRITE ports and separate READ and WRITE clocks. The READ ports support asynchronous and synchronous operation, while the WRITE ports support synchronous operation. Each port has 18 data lines and 8 address lines, allowing word lengths of up to 18 bits and address spaces of up to 256 words. Depending on the mode selected, however, some higher order data or address lines may not be used.

The Write Enable (WE) line acts as a clock enable for synchronous write operation. The Read Enable (RE) acts as a clock enable for synchronous READ operation (ASYNCRD input low), or as a flow-through enable for asynchronous READ operation (ASYNCRD input high).

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules.

A similar technique can be used to create depths greater than 256 words. In this case address signals higher than the MSB are encoded onto the write enable (WE) input for WRITE operations. The READ data outputs are multiplexed together using encoded higher READ address bits for the multiplexer SELECT signals.

The RAM blocks can be loaded with data generated internally (typically for RAM or FIFO functions) or with data from an external PROM (typically for ROM functions).

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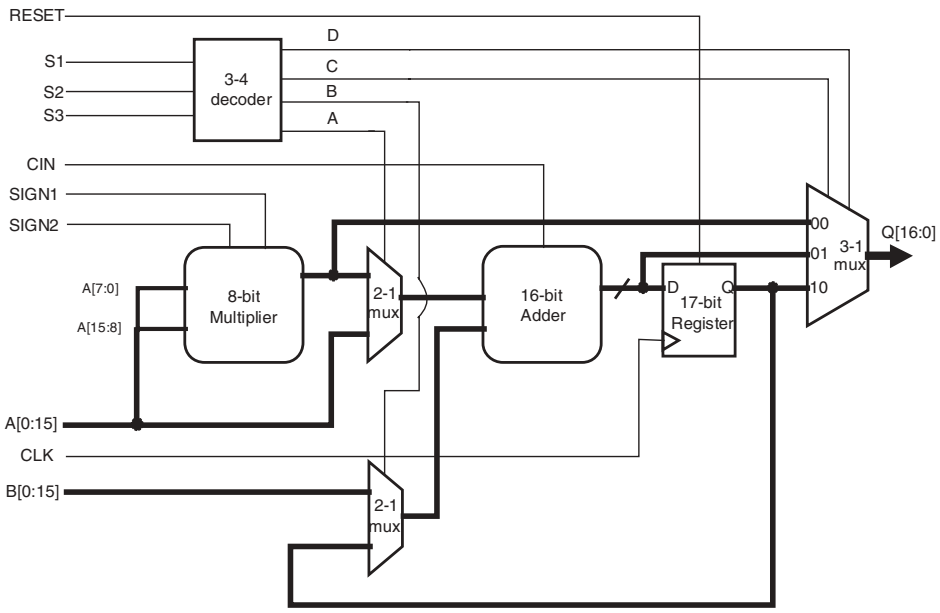
Embedded Computational Unit (ECU)

Traditional Programmable Logic architectures do not implement arithmetic functions efficiently or effectively—these functions require high logic cell usage while garnering only moderate performance results.

The QL58x2 device family architecture allows for functionality above and beyond that achievable using programmable logic devices. By embedding a dynamically reconfigurable computational unit, the QL58x2 device family can address various arithmetic functions efficiently. This approach offers greater performance and utilization than traditional programmable logic implementations. The embedded block is implemented at the transistor level as shown in **Figure 6**.

Figure 6: ECU Block Diagram



The QL58x2 device family ECU blocks (**Table 8**) are placed next to the SRAM circuitry for efficient memory/instruction fetch and addressing for DSP algorithmic implementations.

Table 8: QL58x2 Device Family ECU Blocks

Device	ECUs
QL5842	12
QL5822	0

Up to twelve 8-bit MAC functions can be implemented per cycle for a total of 1 billion MACs/s when clocked at 100 MHz. Additional multiply-accumulate functions can be implemented in the programmable logic.

The modes for the ECU block are dynamically re-programmable through the programmable logic.

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Table 9: ECU Mode Select Criteria

Instruction			Operation	ECU Performance[a], -8 WCC		
S1	S2	S3		t_{PD}	t_{SU}	t_{CO}
0	0	0	Multiply	6.6 ns max		
0	0	1	Multiply-Add	8.8 ns max		
0	1	0	Accumulate[b]		3.9 ns min	1.2 ns max
0	1	1	Add	3.1 ns max		
1	0	0	Multiply (registered)[c]		9.6 ns min	1.2 ns max
1	0	1	Multiply- Add (registered)		9.6 ns min	1.2 ns max
1	1	0	Multiply - Accumulate		9.6 ns min	1.2 ns max
1	1	1	Add (registered)		3.9 ns min	1.2 ns max

a. t_{PD}, t_{SU} and t_{CO} do not include routing paths in/out of the ECU block.
b. Internal feedback path in ECU restricts max clk frequency to 238 MHz.
c. B [15:0] set to zero.

NOTE: Timing numbers in **Table 9** represent -8 Worst Case Commercial conditions.

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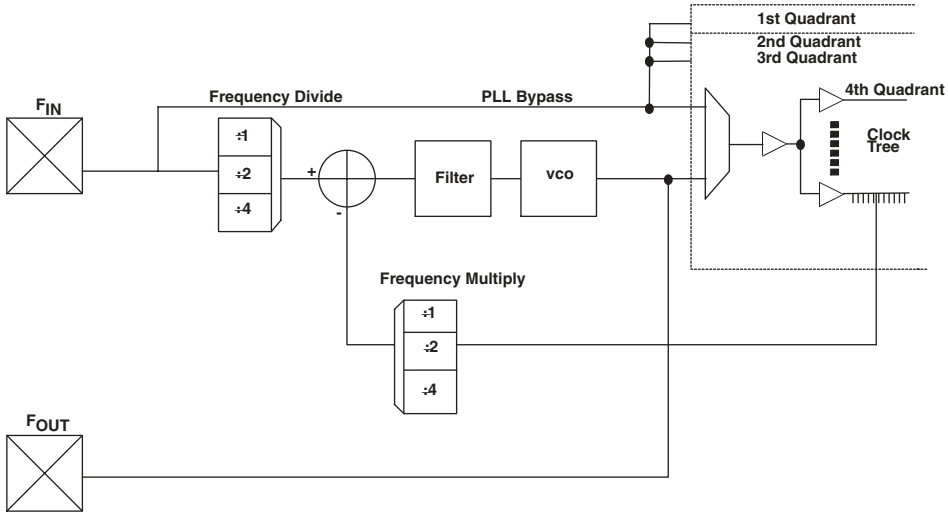
Phase Locked Loop (PLL) Information

Instead of requiring extra components, designers simply need to instantiate one of the pre-configured models (described in this section). The QuickLogic built-in PLLs support a wider range of frequencies than many other PLLs. These PLLs also have the ability to support different ranges of frequency multiplications or divisions, driving the device at a faster or slower rate than the incoming clock frequency. When PLLs are cascaded, the clock signal must be routed off-chip through the PLLPAD_OUT pin prior to routing into another PLL; internal routing cannot be used for cascading PLLs.

Figure 7 illustrates a QuickLogic PLL.

Figure 7: PLL Block Diagram



F_{in} represents a very stable high-frequency input clock and produces an accurate signal reference. This signal can either bypass the PLL entirely, thus entering the clock tree directly, or it can pass through the PLL itself.

Within the PLL, a voltage-controlled oscillator (VCO) is added to the circuit. The external F_{in} signal and the local VCO form a control loop. The VCO is multiplied or divided down to the reference frequency, so that a phase detector (the crossed circle in **Figure 7**) can compare the two signals. If the phases of the external and local signals are not within the tolerance required, the phase detector sends a signal through the charge pump and loop filter (**Figure 7**). The charge pump generates an error voltage to bring the VCO back into alignment, and the loop filter removes any high frequency noise before the error voltage enters the VCO. This new VCO signal enters the clock tree to drive the chip's circuitry.

F_{out} represents the clock signal emerging from the output pad (the output signal PLLPAD_OUT is explained in **Table 11**). The PLL always drives the PLLPAD_OUT signal, regardless of whether the PLL is configured for on-chip use. The PLLPAD_OUT will not oscillate if PLL_RESET is asserted, or if the PLL is powered down.

Most QuickLogic products contain four PLLs. The PLL presented in **Figure 7** controls the clock tree in the fourth quadrant of its FPGA. QuickLogic PLLs compensate for the additional delay created by the clock tree itself, as previously noted, by subtracting the clock tree delay through the feedback path.

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PLL Modes of Operation

QuickLogic PLLs have eight modes of operation, based on the input frequency and desired output frequency—**Table 10** indicates the features of each mode.

NOTE: "HF" stands for "high frequency" and "LF" stands for "low frequency."

Table 10: PLL Mode Frequencies

PLL Model	Output Frequency	Input Frequency Range	Output Frequency Range
PLL_HF	Same as input	66 MHz–220 MHz	66 MHz–220 MHz
PLL_LF	Same as input	25 MHz–66 MHz	25 MHz–66 MHz
PLL_MULT2HF	2x	33 MHz–110 MHz	66 MHz–220 MHz
PLL_MULT2LF	2x	12.5 MHz–33 MHz	25 MHz–66 MHz
PLL_DIV2HF	1/2x	220 MHz–440 MHz	110 MHz–220 MHz
PLL_DIV2LF	1/2x	50 MHz–220 MHz	25 MHz–110 MHz
PLL_MULT4	4x	12.5 MHz–50 MHz	50 MHz–200 MHz
PLL_DIV4	1/4x	100 MHz–440 MHz	25 MHz–110 MHz

The input frequency can range from 12.5 MHz to 440 MHz, while output frequency ranges from 25 MHz to 220 MHz. When adding PLLs to the top-level design, be sure that the PLL mode matches the desired input and output frequencies.

PLL Signals

Table 11 summarizes the key signals in QuickLogic PLLs.

Table 11: QuickLogic PLL Signals

Signal Name	Description
PLLCLK_IN	**Input clock signal**
PLL_RESET	**Active High Reset** If PLL_RESET is asserted, then CLKNET_OUT and PLLPAD_OUT are reset to 0. This signal must be asserted and then released in order for the LOCK_DETECT to work.
ONn_OFFCHIP	This is a reserved signal. It can be connected to VCC or GND.
CLKNET_OUT	**Out to internal gates** This signal bypasses the PLL logic before driving the internal gates. Note that this signal cannot be used in the same quadrant where the PLL signal is used (PLLCLK_OUT).
PLLCLK_OUT	**Out from PLL to internal gates** This signal can drive the internal gates after going through the PLL.
PLLPAD_OUT	**Out to off-chip** This outgoing signal is used off-chip. The PLLPAD_OUT is always active, driving the PLL-derived clock signal out through the pad. The PLLPAD_OUT will not oscillate if PLL_RESET is asserted, or if the PLL is powered down.
LOCK_DETECT	**Active High Lock detection signal** NOTE: For simulation purposes, this signal gets asserted after 10 clock cycles. However, it can take a maximum of 200 clock cycles to sync with the input clock upon release of the PLL_RESET signal.

NOTE: Because PLLCLK_IN and PLL_RESET signals have PLL_INPAD, and PLLPAD_OUT has OUTPAD, you do not need to add additional pads to your design.

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I/O Cell Structure

The QL58x2 device family features a variety of distinct I/O pins to maximize performance, functionality, and flexibility with bi-directional I/O pins and input-only pins. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single ended I/O standards, VCCIO specifies the input tolerance and the output drive. For voltage referenced I/O standards (e.g SSTL), the voltage supplied to the INREF pins in each bank specifies the input switch point. For example, the VCCIO pins must be tied to a 3.3 V supply to provide 3.3 V compliance. The QL58x2 device family can also support the LVDS and LVPECL I/O standards with the use of external resistors (see **Table 12**).

Table 12: I/O Standards and Applications

I/O Standard	Reference Voltage	Output Voltage	Application
LVTTL	n/a	3.3 V	General Purpose
LVCMOS25	n/a	2.5 V	General Purpose
LVCMOS18	n/a	1.8 V	General Purpose
PCI	n/a	3.3 V	PCI Bus Applications
GTL+	1	n/a	Backplane
SSTL3	1.5	3.3 V	SDRAM
SSTL2	1.25	2.5 V	SDRAM

As designs become more complex and requirements more stringent, several application-specific I/O standards have emerged for specific applications. I/O standards for processors, memories, and a variety of bus applications have become commonplace and a requirement for many systems. In addition, I/O timing has become a greater issue with specific requirements for setup, hold, clock to out, and switching times. The QL58x2 device family has addressed these new system requirements and now includes a completely new I/O cell which consists of programmable I/Os as well as a new cell structure consisting of three registers—Input, Output, and OE.

The QL58x2 device family offers banks of programmable I/Os that address many of the bus standards that are popular today. As shown in **Figure 8** each bi-directional I/O pin is associated with an I/O cell which features an input register, an input buffer, an output register, a three-state output buffer, an output enable register, and 2 two-to-one output multiplexers.

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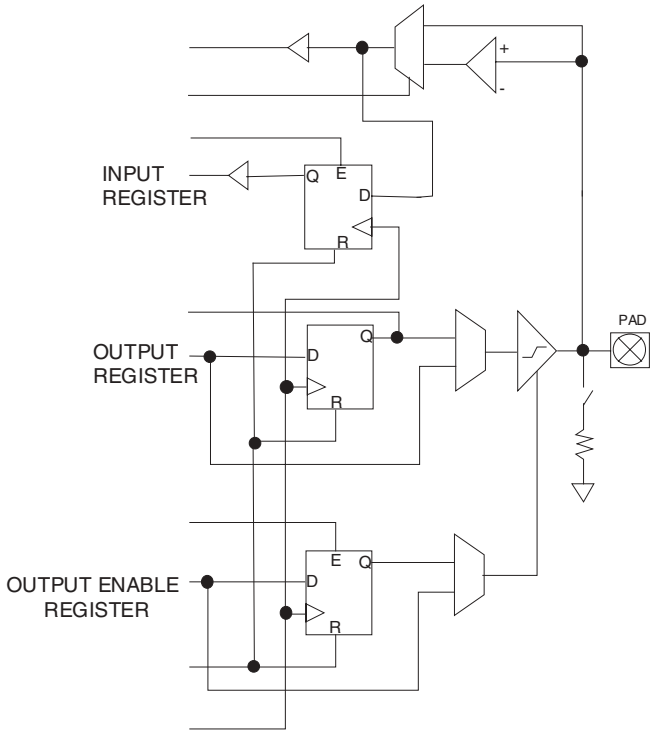
Figure 8: QL58x2 Device Family I/O Cell



The bi-directional I/O pin options can be programmed for input, output, or bi-directional operation. As shown in **Figure 8**, each bi-directional I/O pin is associated with an I/O cell which features an input register, an input buffer, an output register, a three-state output buffer, an output enable register, and 2 two-to-one multiplexers. The select lines of the two-to-one multiplexers are static and must be connected to either VCC or GND.

For input functions, I/O pins can provide combinatorial, registered data, or both options simultaneously to the logic array. For combinatorial input operation, data is routed from I/O pins through the input buffer to the array logic. For registered input operation, I/O pins drive the D input of input cell registers, allowing data to be captured with fast, predictable set-up times without consuming internal logic cell resources. The comparator and multiplexer in the input path allows for native support of I/O standards with reference points offset from traditional ground.

For output functions, I/O pins can receive combinatorial or registered data from the logic array. For combinatorial output operation, data is routed from the logic array through a multiplexer to the I/O pin. For registered output operation, the array logic drives the D input of the output cell register which in turn drives the I/O pin through a multiplexer. The multiplexer allows either a combinatorial or a registered signal to be driven to the I/O pin. The addition of an output register will also decrease the Tco. Since the output register does not need to drive the routing the length of the output path is also reduced, and static timing analysis becomes very predictable.

The three-state output buffer controls the flow of data from the array logic to the I/O pin and allows the I/O pin to act as an input and/or output. The buffer's output enable can be individually controlled by the logic cell array or any pin (through the regular routing resources), or it can be bank-controlled through one of the global networks. The signal can also be either combinatorial or registered. This is identical to that of the flow for the output cell. For combinatorial control operation, data is routed from the logic array through a multiplexer to the three-state control. The IOCTRL pins can directly drive the OE and CLK signals for all I/O cells within the same bank.

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For registered control operation, the array logic drives the D input of the OE cell register which in turn drives the three-state control through a multiplexer. The multiplexer allows either a combinatorial or a registered signal to be driven to the three-state control.

When I/O pins are unused, the OE controls can be permanently disabled, allowing the output cell register to be used for registered feedback into the logic array.

I/O cell registers are controlled by clock, clock enable, and reset signals, which can come from the regular routing resources, from one of the global networks, or from two IOCTRL input pins per bank of I/O's. The CLK and RESET signals share common lines, while the clock enables for each register can be independently controlled. I/O interface support is programmable on a per bank basis.

The larger QL58x2 (QL5842) device contains eight I/O banks. **Figure 9** illustrates the I/O bank configurations for QL5842. The smaller QL58x2 (QL5822) device contains two I/O banks per device. **Figure 10** illustrates the I/O bank configurations for QL5822.

Each I/O bank is independent of other I/O banks and each I/O bank has its own VCCIO and INREF supply inputs. A mixture of different I/O standards can be used on the device; however, there is a limitation as to which I/O standards can be supported within a given bank. Only standards that share a common VCCIO and INREF can be shared within the same bank (e.g., PCI and LVTTL). In the case of the QL5822, only one voltage-referenced standard can be used. The two I/O banks, A and B, share the INREF pin.

Figure 9: Multiple I/O Banks on QL5842

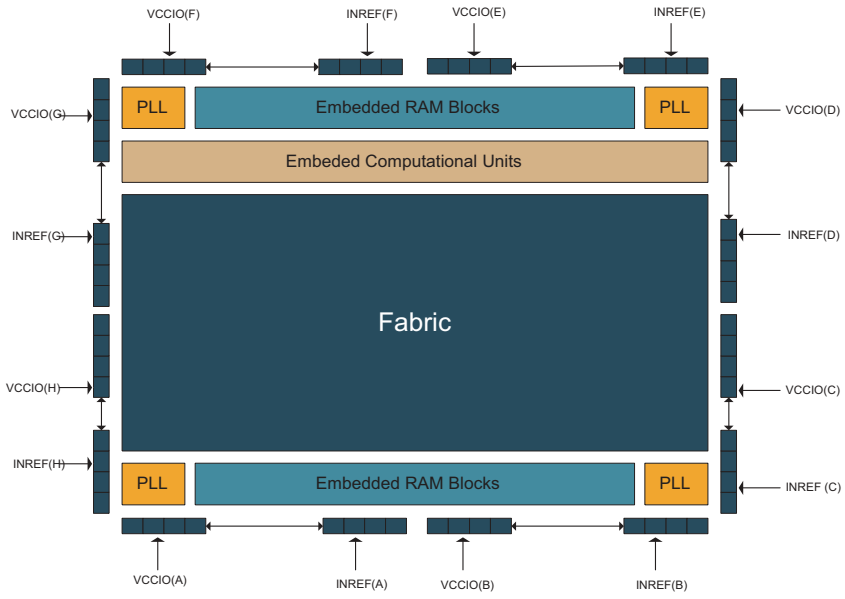
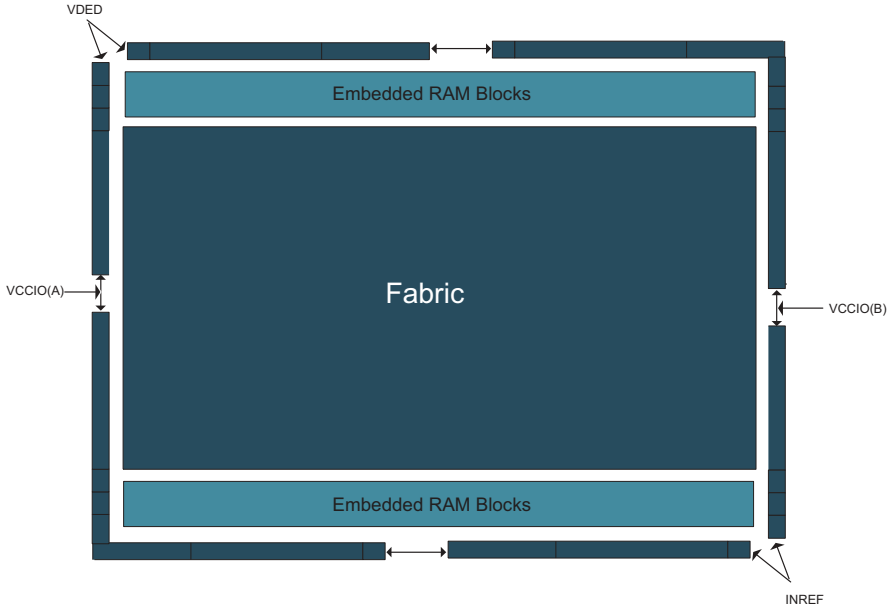


Figure 10: Multiple I/O Banks on QL5822



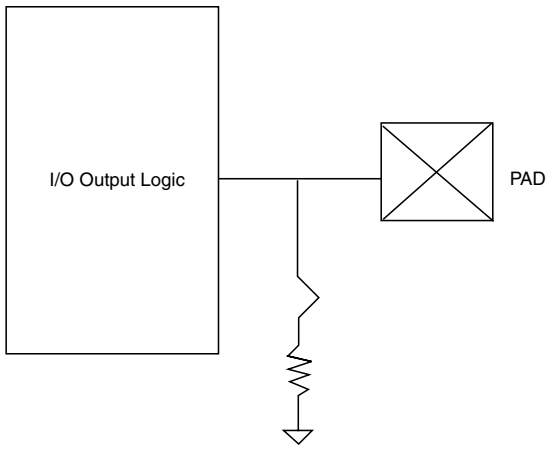
Programmable Slew Rate

Each I/O has programmable slew rate capability—the slew rate can be either fast or slow. The slower rate can be used to reduce the switching times of each I/O.

Programmable Weak Pull-Down

A programmable Weak Pull-Down resistor is available on each I/O. The I/O Weak Pull-Down eliminates the need for external pull down resistors for used I/Os as shown in **Figure 11**. The spec for pull-down current is maximum of 150 µA under worst case condition.

Figure 11: Programmable I/O Weak Pull-Down



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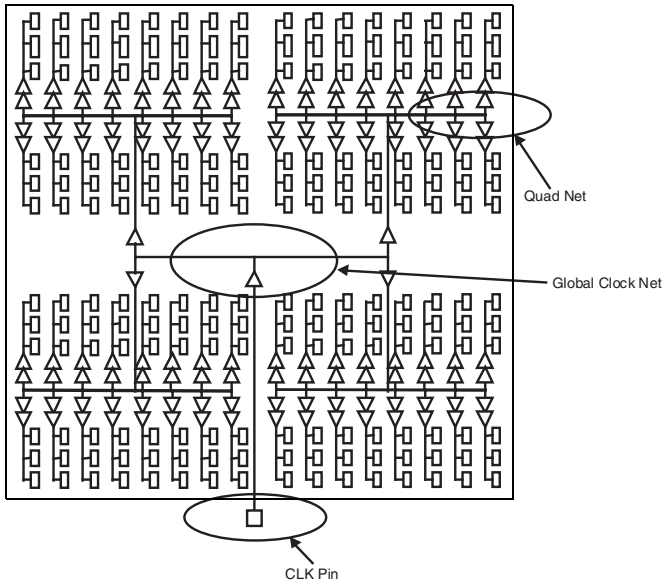
Clock Networks

Global Clocks

There are a maximum of seven global clock networks in each QL58x2 device. Global clocks can drive logic cells and I/O registers, ECUs, and RAM blocks in the device. All global clocks have access to a Quad Net (local clock network) connection with a programmable connection to the logic cell's register clock input.

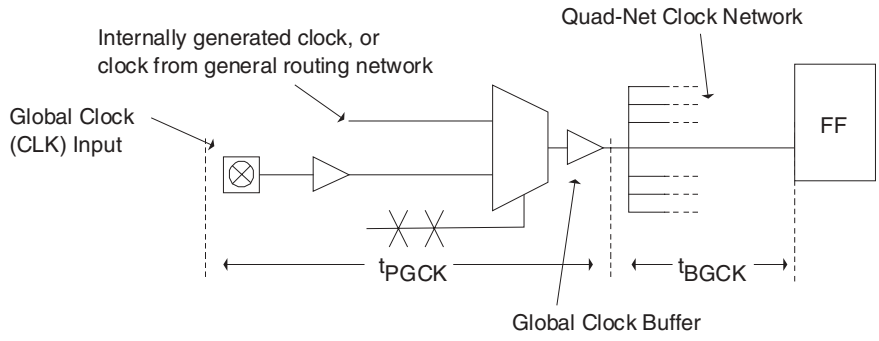
Figure 12: Global Clock Architecture



Quad-Net Network

There are five Quad-Net local clock networks in each quadrant for a total of 20 in a device. Each Quad-Net is local to a quadrant. Before driving the column clock buffers, the quad-net is driven by the output of a mux which selects between the CLK pin input and an internally generated clock source (see **Figure 13**).

Figure 13: Global Clock Structure



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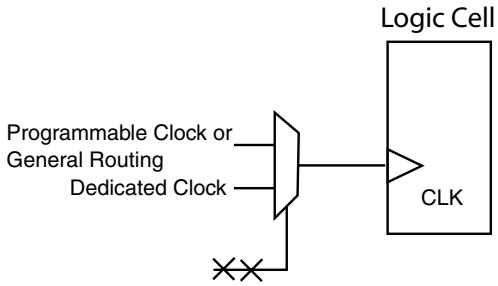
Dedicated Clock

There is one dedicated clock in the larger device of the QL58x2 family (QL5842). This clock connects to the clock input of the Logic Cell and I/O registers, and RAM blocks through a hardwired connection and is multiplexed with the programmable clock input. The dedicated clock provides a fast global network with low skew. Users have the ability to select either the dedicated clock or the programmable clock (**Figure 14**).

Figure 14: Dedicated Clock Circuitry within Logic Cell



NOTE: For more information on the clocking capabilities of the QL58x2 Enhanced QuickPCI Family, see QuickLogic Application Note 68 at http://www.quicklogic.com/images/appnote68.pdf.

I/O Control and Local Hi-Drives

Each bank of I/Os has two input-only pins that can be programmed to drive the RST, CLK, and EN inputs of I/Os in that bank. These input-only pins also serve as high drive inputs to a quadrant. These buffers can be driven by the internal logic both as an I/O control or high drive. For I/O constrained designs, these pins can be used for general purpose inputs. To provide more general purpose I/Os in the 208 PQFP package, the I/O controls pins are not bonded out. The performance of these resources is presented in **Table 13**.

Table 13: I/O Control Network/Local High-Drive

Destination TT, 25 C, 2.5 V	From Pad	From Array
I/O (far)	1.00 ns	1.14 ns
I/O (near)	0.63 ns	0.78 ns
Skew	0.37 ns	0.36 ns

Table 14 shows the total number of I/O control pins per device/package combination. These pins are not bonded out in the smaller devices and packages. This increases the number of bi-directional user I/Os available.

Table 14: I/O Control Pins per Device/Package Combination

Device	144 TQFP	196 TFBGA	208 PQFP	280 LFBGA	484 BGA
QL5822	-	-	-	-	-
QL5842	-	-	-	16	16

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Programmable Logic Routing

QL58x2 devices are engineered with six types of routing resources as follows: short (sometimes called segmented) wires, dual wires, quad wires, express wires, distributed networks, and default wires. Short wires span the length of one logic cell, always in the vertical direction. Dual wires run horizontally and span the length of two logic cells. Short and dual wires are predominantly used for local connections. Default wires supply VCC and GND (Logic '1' and Logic '0') to each column of logic cells.

Quad wires have passive link interconnect elements every fourth logic cell. As a result, these wires are typically used to implement intermediate length or medium fan-out nets.

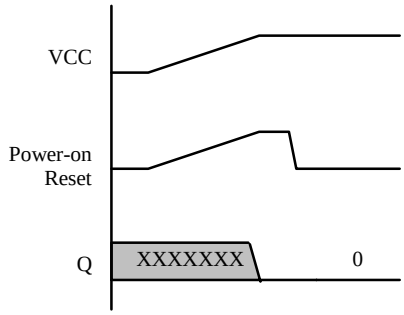
Express lines run the length of the device uninterrupted. Each of these lines has a higher capacitance than a quad, dual, or short wire, but less capacitance than shorter wires connected to run the length of the device. The resistance will also be lower because the express wires don't require the use of pass links. Express wires provide higher performance for long routes or high fan-out nets.

Distributed networks are described in **Clock Networks** on page 21. These wires span the programmable logic and are driven by quad-net buffers.

Global Power-On Reset (POR)

The QL58x2 device family features a global power-on reset. This reset is hardwired to all registers and resets them to Logic '0' upon power-up of the device. In QuickLogic devices, the asynchronous Reset input to flip-flops has priority over the Set input; therefore, the Global POR will reset all flip-flops during power-up. If you want to set the flip-flops to Logic '1', you must assert the "Set" signal after the Global POR signal has been deasserted.

Figure 15: Power-On Reset



Low Power Mode

Quiescent power consumption of all QL58x2 family devices can be reduced significantly by de-activating the charge pumps inside the architecture. By applying 3.3 V to the VPUMP pin, the internal charge pump is de-activated—this effectively reduces the static and dynamic power consumption of the device. The QL58x2 device family is fully functional and operational in the Low Power mode. Users who have a 3.3 V supply available in their system should take advantage of this low power feature by tying the VPUMP pin to 3.3 V. Otherwise, if a 3.3 V supply is not available, this pin should be tied to ground.

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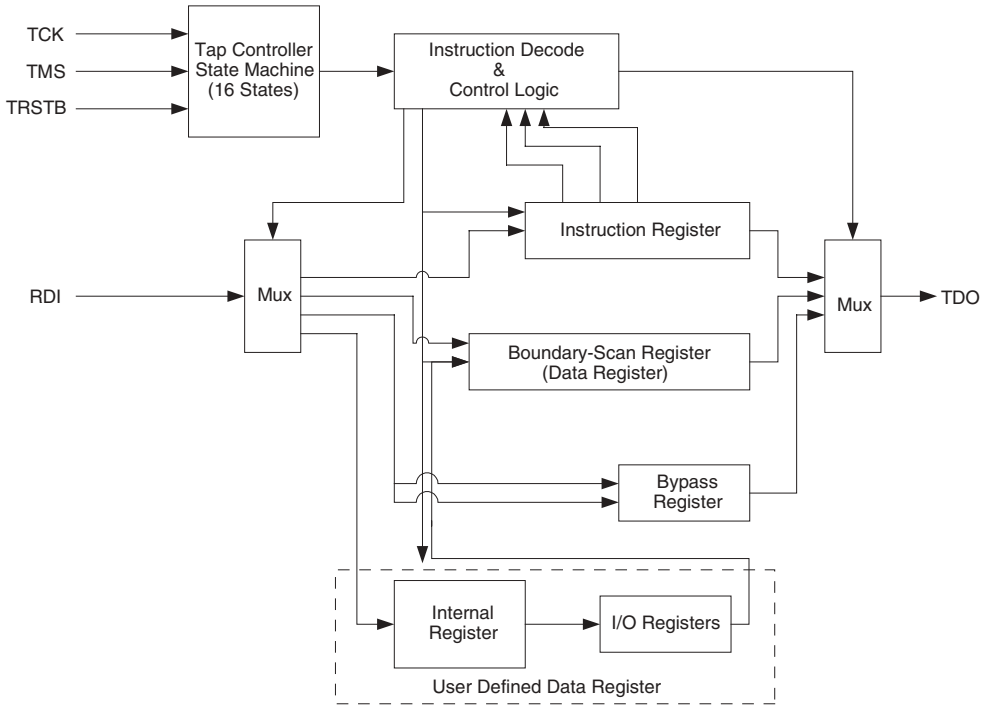
Joint Test Access Group (JTAG) Information

Figure 16: JTAG Block Diagram



Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, one problem being the accessibility of test points. JTAG formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (through the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed through a data scan operation, allowing users to sample the functional data entering and leaving the device.

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- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

JTAG BSDL Support

- BSDL-Boundary Scan Description Language
- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/package combinations from QuickLogic
- Extensive industry support available and ATVG (Automatic Test Vector Generation)

Security Links

There are several security links to disable reading logic from the array, and to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs. The option to program these links is selectable through QuickWorks in the Tools/Options/Device Programming window in SpDE.

Power-Up Loading Link

The flexibility link enables Power-Up Loading of the Embedded RAM blocks. If the link is programmed, the Power-Up Loading state machine is activated during power-up of the device. The state machine communicates with an external EPROM via the JTAG pins to download memory contents into the on-chip RAM. If the link is not programmed, Power-Up Loading is not enabled and the JTAG pins function as they normally would. The option to program this link is selectable through QuickWorks in the Tools/Options/Device Programming window in SpDE. For more information on Power-Up Loading, see QuickLogic Application Note 55 at http://www.quicklogic.com/images/appnote55.pdf. See the power-up loading power-up sequencing requirement for proper functionality in **Figure 17**.

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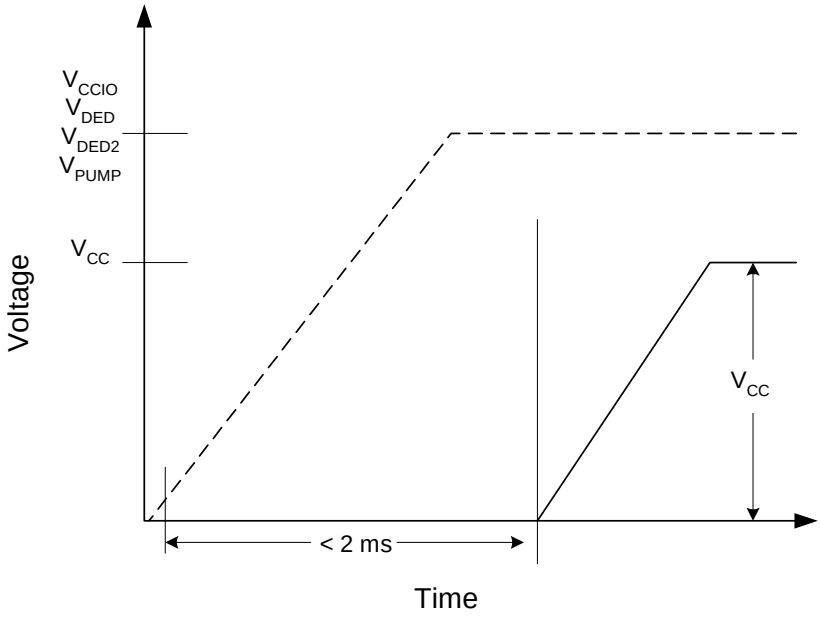
Figure 17: Required Power-Up Sequence When Using Power-Up Loading



To use the power-up loading function in QL58x2 designers must ensure that V_{CC} begins to ramp within a maximum of 2 ms of V_{CCIO}, V_{DED}, V_{DED2}, and V_{PUMP}.

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Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 15** through **Table 19**.

Table 15: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 2.0 V	Latch-up Immunity	±100 mA
VCCIO Voltage	-0.5 V to 4.0 V	DC Input Current	±20 mA
INREF Voltage	0.5 V to VCCIO	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to VCCIO + 0.5 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C

Table 16: Recommended Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		1.71	1.89	1.71	1.89	1.71	1.89	V
VCCIO	I/O Input Tolerance Voltage		1.71	3.60	1.71	3.60	1.71	3.60	V
TJ	Junction Temperature		-55	125	-40	100	0	85	°C
K	Delay Factor	-33A Speed Grade	0.49	1.57	0.50	1.51	0.54	1.47	n/a
		-33B Speed Grade	0.48	1.40	0.50	1.34	0.53	1.31	n/a
		-66C Speed Grade	0.45	1.32	0.47	1.26	0.50	1.23	n/a

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Table 17: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-1	1	µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	1	µA
C_I	I/O Input Capacitance	-	-	8	pF
C_{CLOCK}	Clock Input Capacitance	-	-	8	pF
I_{OS}	Output Short Circuit Current[a]	VO = GND VO = VCC	-15 40	-180 210	mA mA
I_{REF}	Quiescent Current on INREF	-	-10	10	µA
I_{PD}	Current on programmable pull-down	VCC = 1.8 V	-	50	µA
I_{PUMP}	Quiescent Current on VPUMP	VPUMP= 3.3 V	-	10	µA
I_{PLL}	Quiescent Current on each VCCPLL	2.5 V 3.3 V	-	3	mA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.6 V VCCIO = 2.5 V VCCIO = 1.8 V	-	20 10 10	µA

a. Only one output at a time. Duration should not exceed 30 seconds.

Table 18: Quiescent ICC Characteristics

Device	VPUMP = 0 V	VPUMP = 3.3 V
QL5822	-	-
QL5842[a, b]	2 mA	-

a. For -33B/-66C commercial grade devices only. Maximum Quiescent ICC is 3 mA for all industrial grade devices and 5 mA for all military devices.
b. Quiescent ICC is for current drawn by VCC and VDED. If any PLLs are used, see **Table 16** for current drawn by each PLL.

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Table 19: DC Input and Output Levels[a]

Symbol	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	VCCIO + 0.3	0.7	1.7	2.0	-2.0
LVCMOS18	n/a	n/a	-0.3	0.63	1.2	VCCIO + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x VCCIO	0.6 x V_{CCIO}	VCCIO + 0.5	0.1 x VCCIO	0.9 x VCCIO	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	VCCIO + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	1.10	1.90	8	-8

a. The data provided in **Table 19** represents the JEDEC and PCI specification. QuickLogic devices either meet or exceed these requirements. For data specific to QuickLogic I/Os, see preceding **Table 24** through **Table 29**, **Figure 8** and **Figure 11**, and **Figure 39** through **Figure 42**.

NOTE: All CLK, IOCTRL, and PLLIN pins are clamped to the VDED rail. Therefore, these pins can be driven up to VDED. All JTAG inputs are clamped to the VDED2 rail. These JTAG input pins can only be driven up to VDED2.

Figure 18 through **Figure 21** show the VIL and VIH characteristics for I/O and clock pins.

Figure 18: VIL Maximum for I/O

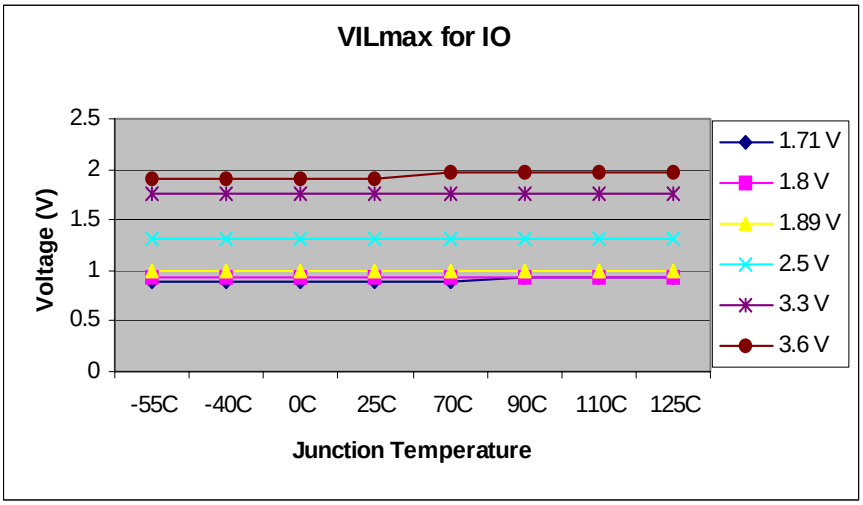

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Figure 19: VIH Minimum for I/O

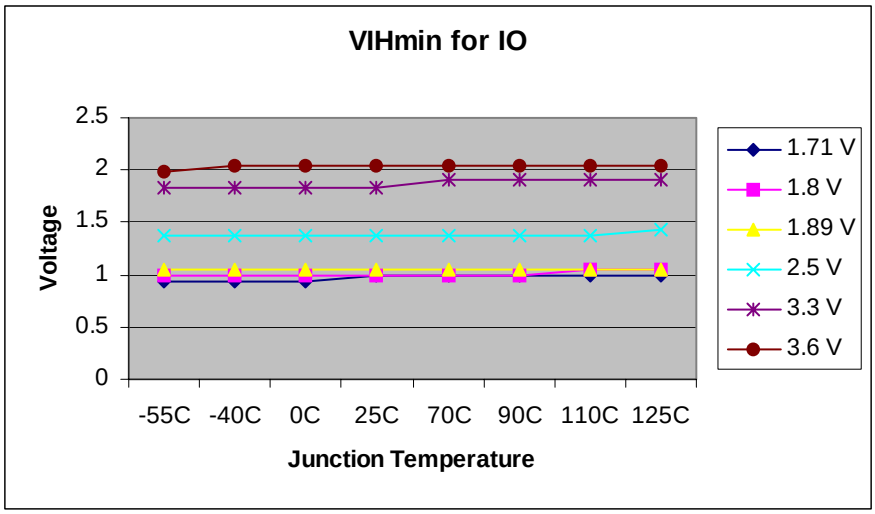

Figure 20: VIL Maximum for CLOCK Pins

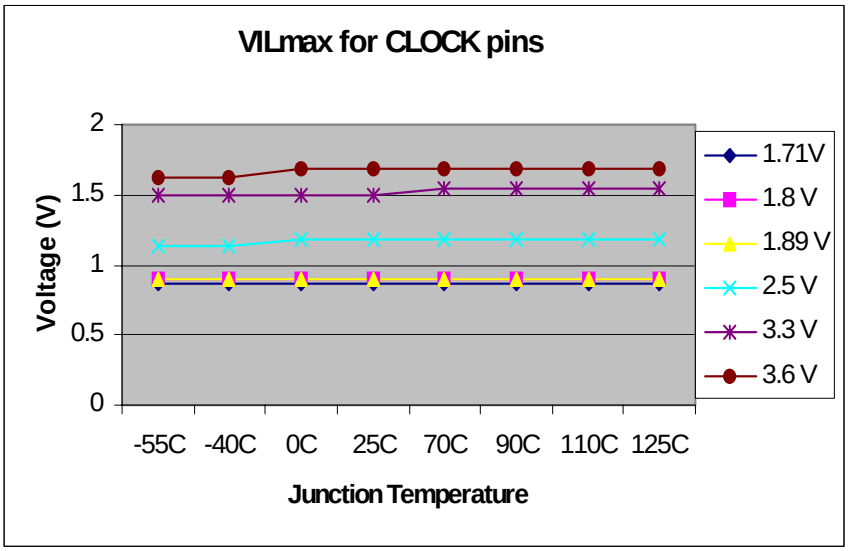

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Figure 21: VIH Minimum for CLOCK Pins

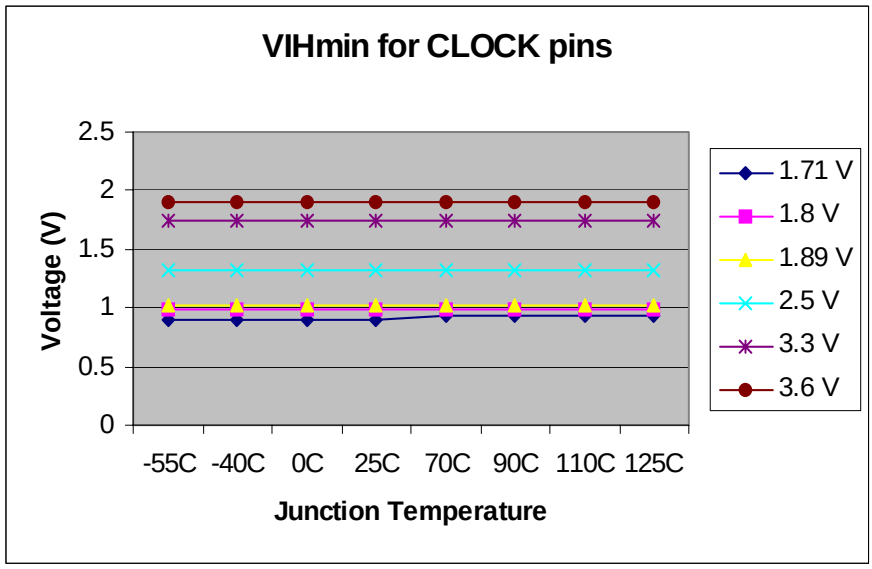

Figure 22 through **Figure 26** show the output drive characteristics for the I/Os across various voltages and temperatures.

Figure 22: Drive Current at VCCIO = 1.71 V

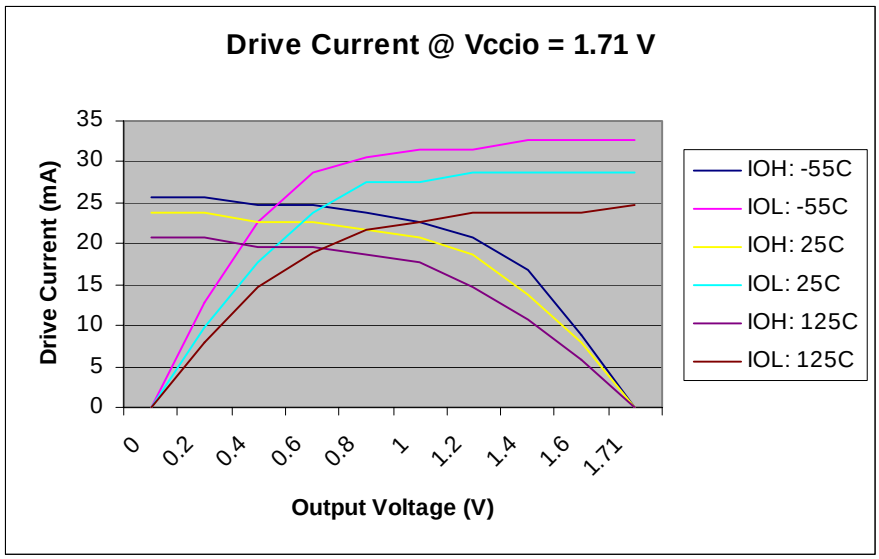

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Figure 23: Drive Current at VCCIO = 1.8 V

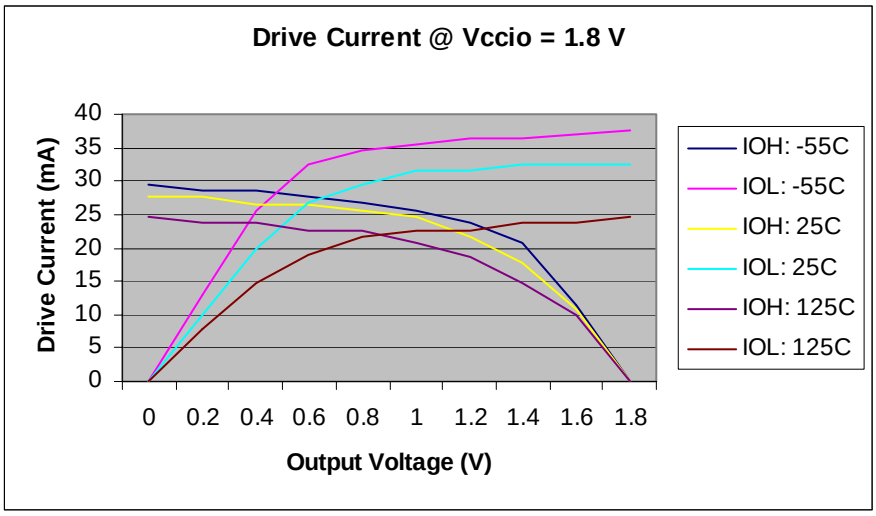

Figure 24: Drive Current at VCCIO = 2.5 V

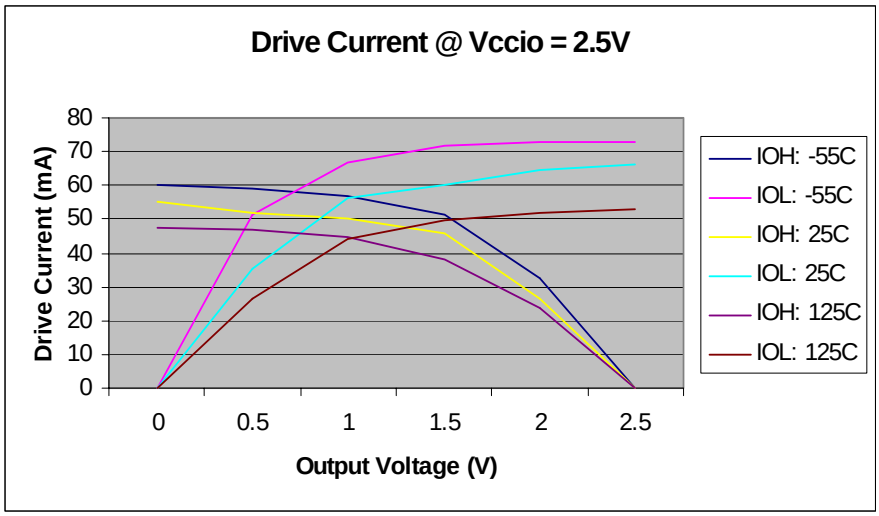

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Figure 25: Drive Current at VCCIO = 3.3 V

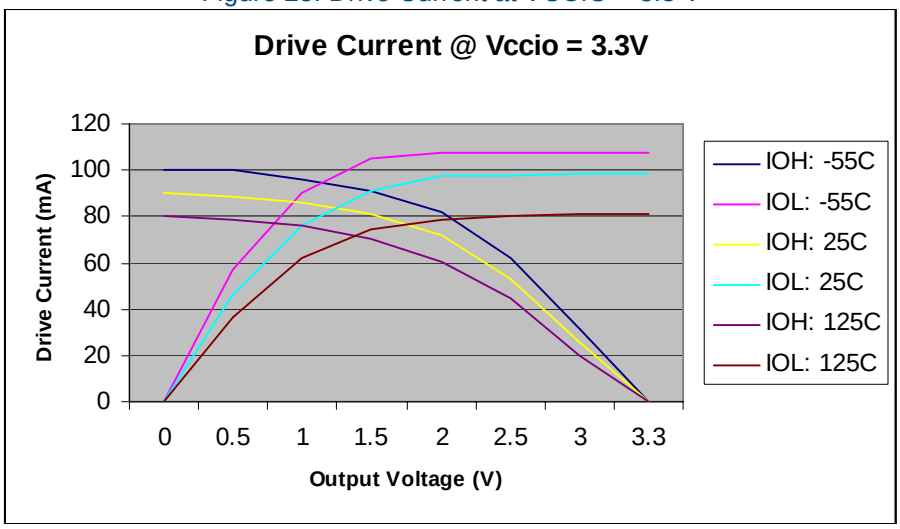

Figure 26: Drive Current at VCCIO = 3.6 V

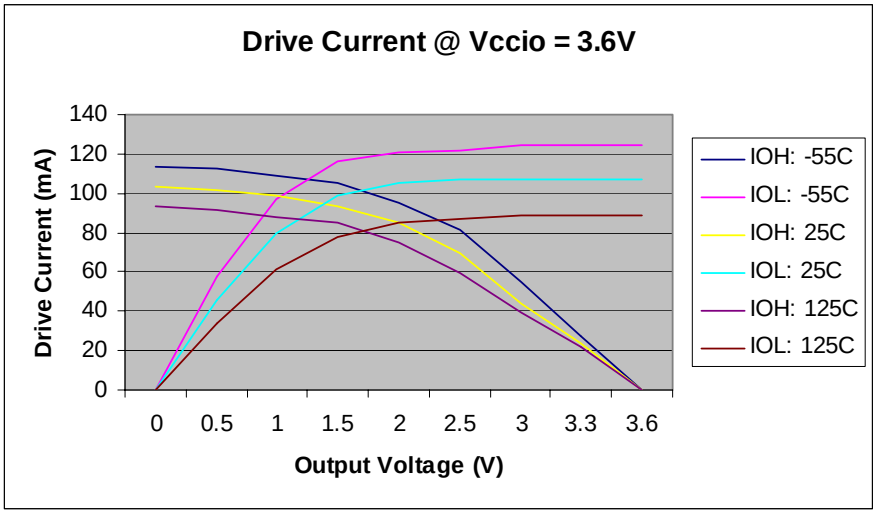

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Figure 27 through **Figure 30** show the quiescent current for the QL5842 for each of the voltage supplies, across voltage and temperature. Quiescent current on V_{CC} is a function of device utilization. The numbers in the following graphs were taken from 100% utilized designs.

Figure 27: Quiescent Current on V_{CC} for QL5842

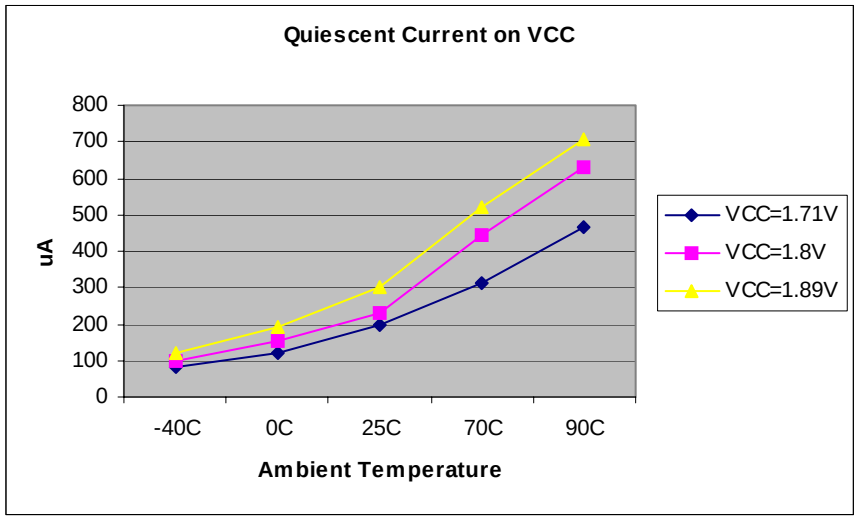

Figure 28: Quiescent Current for QL5842 at V_{DED} = 1.8 V

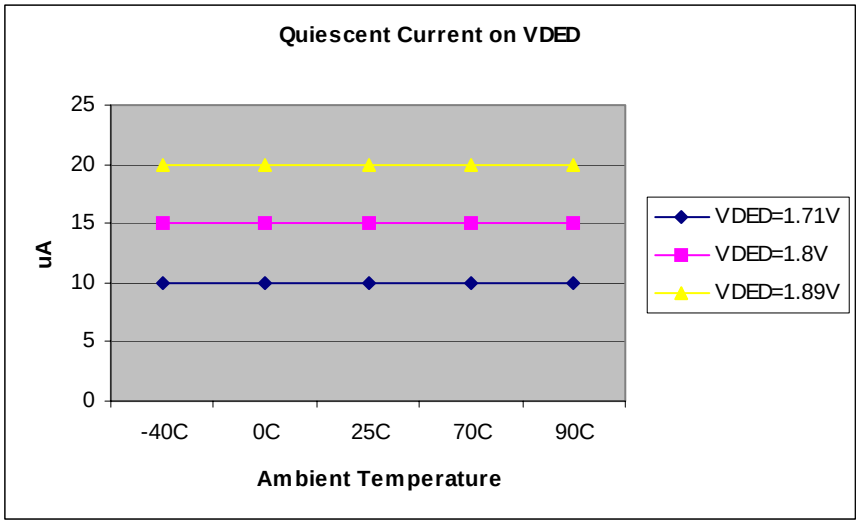

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Figure 29: Quiescent Current for QL5842 at V_{DED} = 3.3 V

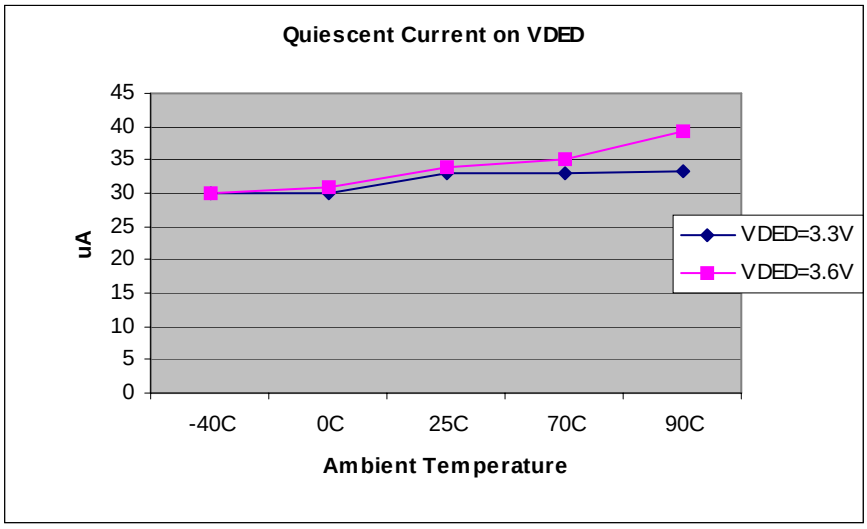
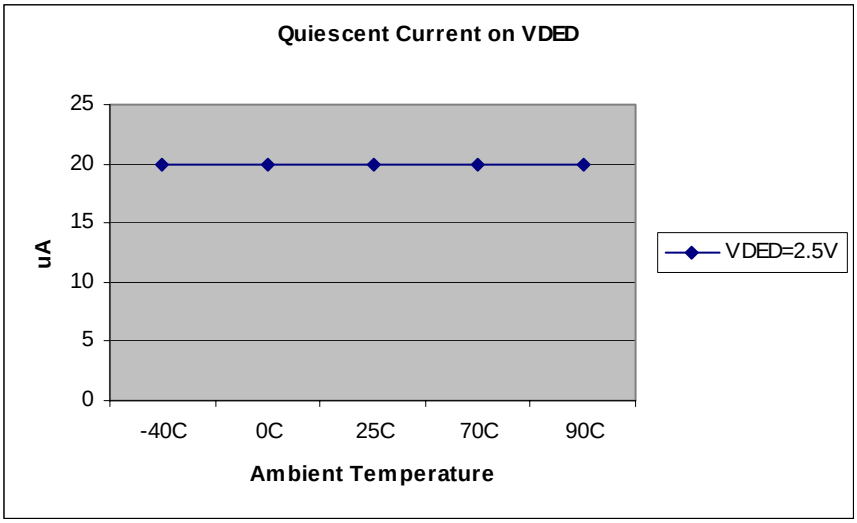


Figure 30: Quiescent Current for QL5842 at V_{DED} = 2.5 V



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AC Characteristics

The AC Specifications (at VCC = 1.8 V, TA = 25° C, Worst Case Corner, Speed Grade = -8 (K = 1.01)) are provided from **Table 20** through **Table 29**. Logic Cell diagrams and waveforms are provided from **Figure 31** through **Figure 42**.

Figure 31: QL58x2 Device Family Logic Cell

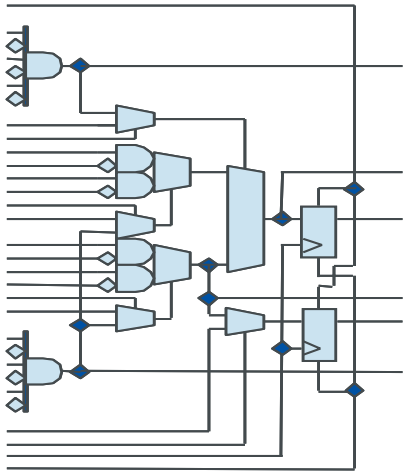

Table 20: Logic Cells

Symbol	Parameter	Value	
		Min	Max
t_{PD}	Combinatorial Delay of the longest path: time taken by the combinatorial circuit to output	0.28 ns	0.98 ns
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	0.10 ns	0.25 ns
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0 ns
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge.	0.22 ns	0.52 ns
t_{CWHI}	Clock High Time: required minimum time the clock stays high	0.46 ns	0.46 ns
t_{CWLO}	Clock Low Time: required minimum time that the clock stays low	0.46 ns	0.46 ns
t_{SET}	Set Delay: time between when the flip-flop is ”set” (high) and when the output is consequently “set” (high)	0.69 ns	0.69 ns
t_{RESET}	Reset Delay: time between when the flip-flop is ”reset” (low) and when the output is consequently “reset” (low)	1.09 ns	1.09 ns
t_{SW}	Set Width: time that the SET signal must remain high/low	0.3 ns	0.3 ns
t_{RW}	Reset Width: time that the RESET signal must remain high/low	0.3 ns	0.3 ns

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Figure 32: Logic Cell Flip-Flop

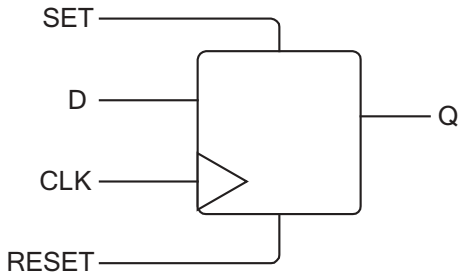

Figure 33: Logic Cell Flip-Flop Timings—First Waveform

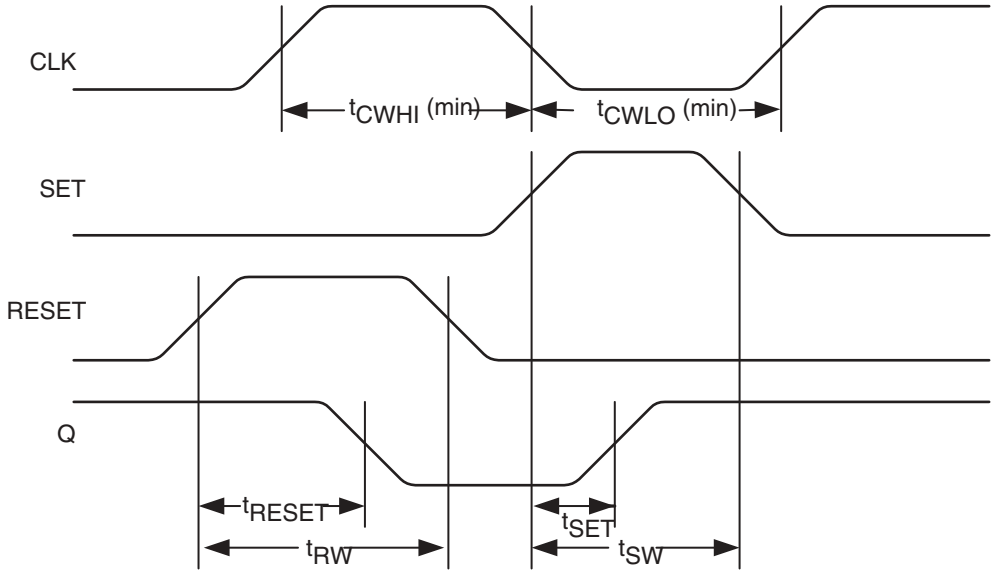

Figure 34: Logic Cell Flip-Flop Timings—Second Waveform

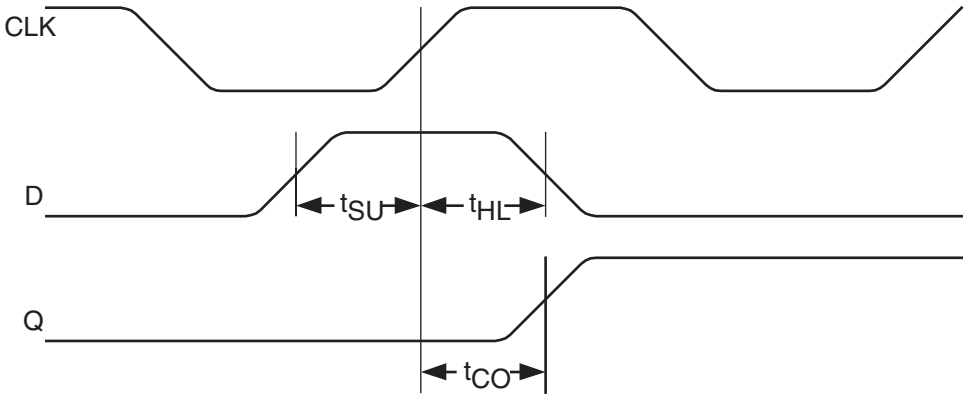

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Table 21: QL58x2 Device Family Global Clock Delay

Clock Segment	Parameter	Value	
		Min	Max
t_{PGCK}	Global clock pin delay to quad net	-	1.92 ns
t_{BGCK}	Global clock tree delay (quad net to flip-flop)	-	0.28 ns

NOTE: When using a PLL, t_{PGCK} and t_{BGCK} are effectively zero due to delay adjustment by Phase Locked Loop feedback path.

Figure 35: Global Clock Structure Timing Elements

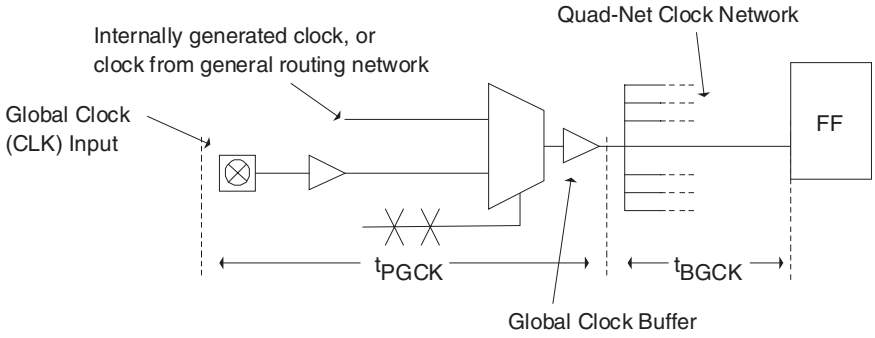

Figure 36: Dual-Port SRAM Cell

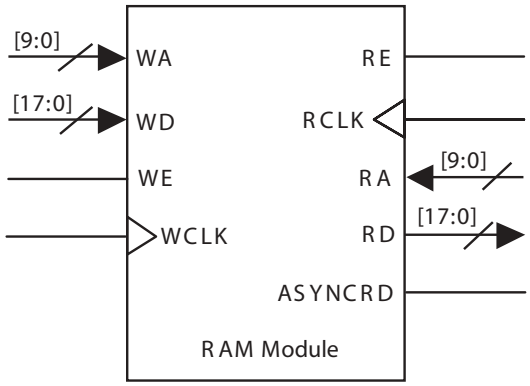

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Table 22: RAM Cell Synchronous Write Timing

Symbol	Parameter	Value	
		Min	Max
RAM Cell Synchronous Write Timing			
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.47 ns	-
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.48 ns	-
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWE}	WE setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0 ns	-
t_{HWE}	WE hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{WCRD}	WCLK to RD (WA = RA): time between the active WRITE CLOCK edge and the time when the data is available at RD	-	3.79 ns

Figure 37: RAM Cell Synchronous Write Timing

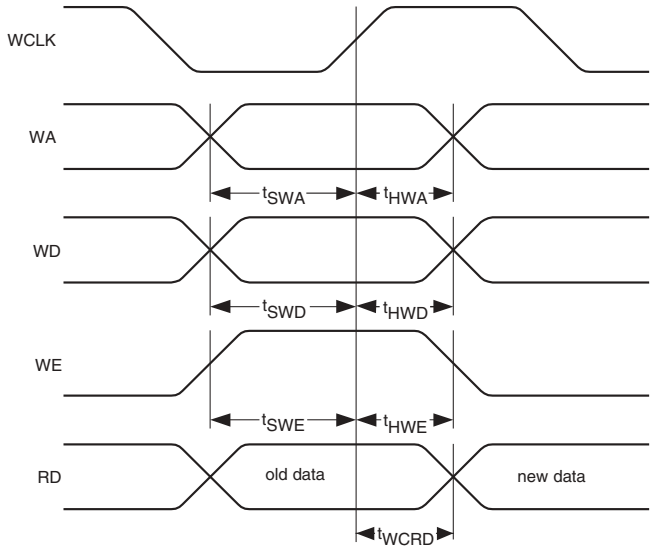

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Table 23: RAM Cell Synchronous and Asynchronous Read Timing

Symbol	Parameter	Value	
		Min	Max
RAM Cell Synchronous Read Timing			
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.43 ns	-
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0 ns	-
t_{SRE}	RE setup time to WCLK: time the READ ENABLE must be stable before the active edge of the READ CLOCK	0.21 ns	-
t_{HRE}	RE hold time to WCLK: time the READ ENABLE must be stable after the active edge of the READ CLOCK	0 ns	-
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD	-	2.25 ns
RAM Cell Asynchronous Read Timing			
r_{PDRD}	RA to RD: time between when the READ ADDRESS is input and when the DATA is output	-	1.99 ns

Figure 38: RAM Cell Synchronous and Asynchronous Read Timing

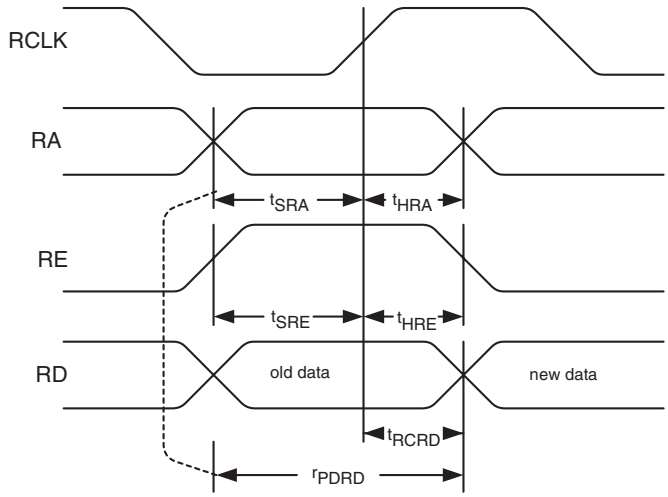

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Figure 39: QL58x2 Device Family I/O Cell Output Path

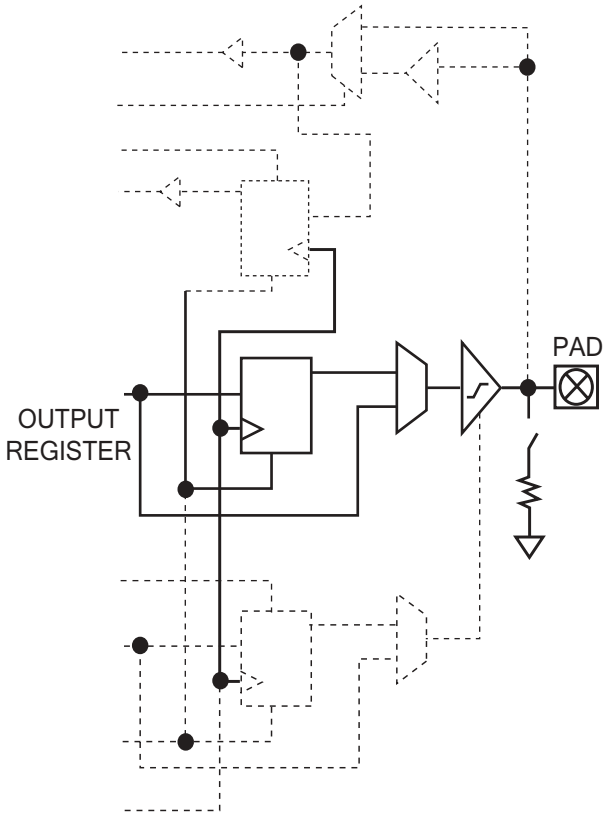

Figure 40: QL58x2 Device Family I/O Cell Output Enable Timing

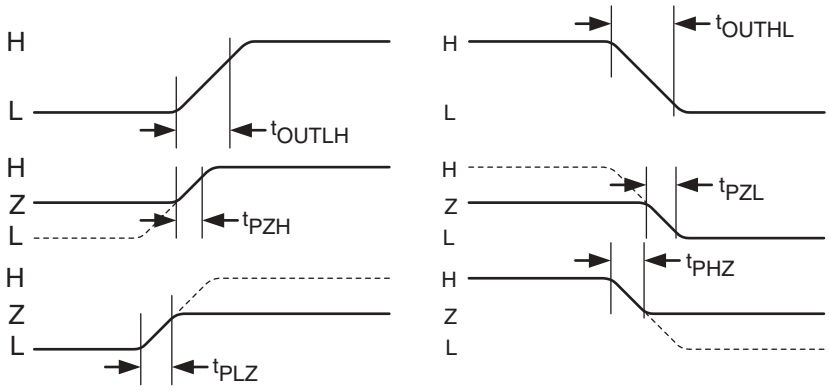

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Table 24: QL58x2 Device Family I/O Cell Output Timing

Symbol	Parameter	Value (ns)	
Output Register Cell Only		**Min**	**Max**
t_{OUTLH}	Output Delay low to high (90% of H)	-	2.95
t_{OUTHL}	Output Delay high to low (10% of L)	-	2.49
t_{PZH}	Output Delay tri-state to high (90% of H)	-	3.93
t_{PZL}	Output Delay tri-state to low (10% of L)	-	2.84
t_{PHZ}	Output Delay high to tri-State	-	3.62
t_{PLZ}	Output Delay low to tri-State	-	3.4
t_{COP}	Clock-to-out delay (does not include clock tree delays)	-	3.3 (fast slew) 5.49 (slow slew)

Table 25: Output Slew Rates @ VCCIO = 3.3 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	2.8 V/ns	1.0 V/ns
Falling Edge	2.86 V/ns	1.0 V/ns

Table 26: Output Slew Rates @ VCCIO = 2.5 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	1.7 V/ns	0.6 V/ns
Falling Edge	1.9 V/ns	0.6 V/ns

Table 27: Output Slew Rates @ VCCIO = 1.8 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	-	-
Falling Edge	-	-

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Figure 41: QL58x2 Device Family I/O Cell Input Path

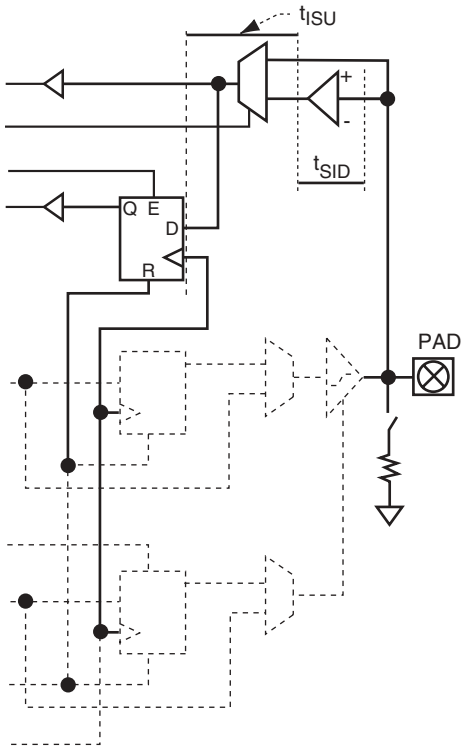

Figure 42: QL58x2 Device Family Input Register Cell Timing

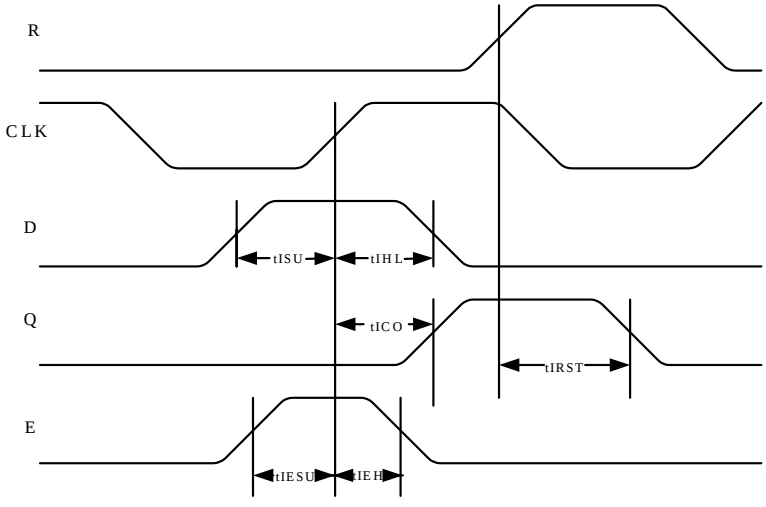

Table 28: I/O Input Register Cell Timing

Symbol	Parameter	Value	
		Min	Max
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.15 ns	-
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	-
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output after the active clock edge	-	0.3 ns
t_{IRST}	Input register reset delay: time between when the flip-flop is “reset”(low) and when the output is consequently “reset” (low)	-	0.82 ns
t_{IESU}	Input register clock enable setup time: time “enable” must be stable before the active clock edge	0.4 ns	-
t_{IEH}	Input register clock enable hold time: time “enable” must be stable after the active clock edge	0 ns	-

Table 29: I/O Input Buffer Delays

Symbol	Parameter	Value	
	To get the total input delay add this delay to t_{ISU}	Min	Max
t_{SID} (LVTTL)	LVTTL input delay: Low Voltage TTL for 3.3 V applications	-	0.82 ns
t_{SID} (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5 V and lower applications	-	0.82 ns
t_{SID} (LVCMOS18)	LVCMOS18 input delay: Low Voltage CMOS for 1.8 V applications	-	-
t_{SID} (GTL+)	GTL+ input delay: Gunning Transceiver Logic	-	0.94 ns
t_{SID} (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3 V	-	0.94 ns
t_{SID} (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5 V	-	0.94 ns

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Package Thermal Characteristics

Thermal Resistance Equations:

$\theta_{JC} = (T_J - T_C)/P$
$\theta_{JA} = (T_J - T_A)/P$
$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JC}: Junction-to-case thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 125°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 30**, pick an appropriate T_{AMAX} and use:

$P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA}$

Table 30: Package Thermal Characteristics

Device	Package Description			θ_{JA} (°C/W)		
	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM
QL5842	PS	PBGA	484	26.6	24.1	21.8
	PT	LFBGA	280	34	31.6	29.9
	PQ	PQFP	208	32	28	26.5
QL5822	PT	TFBGA	196	40	38	35.2
	PQ	PQFP	208	43.6	41	39
	PF	TQFP	144	41	39	37
	PT	LFBGA	280	34	31.6	29.9

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Kv and Kt Graphs

Figure 43: Voltage Factor vs. Supply Voltage

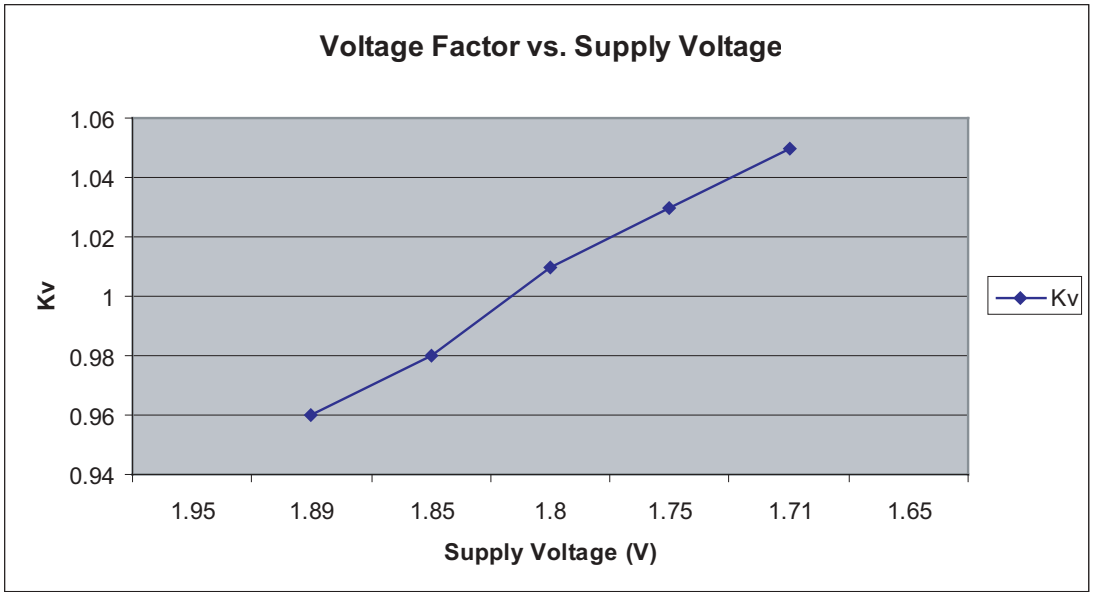
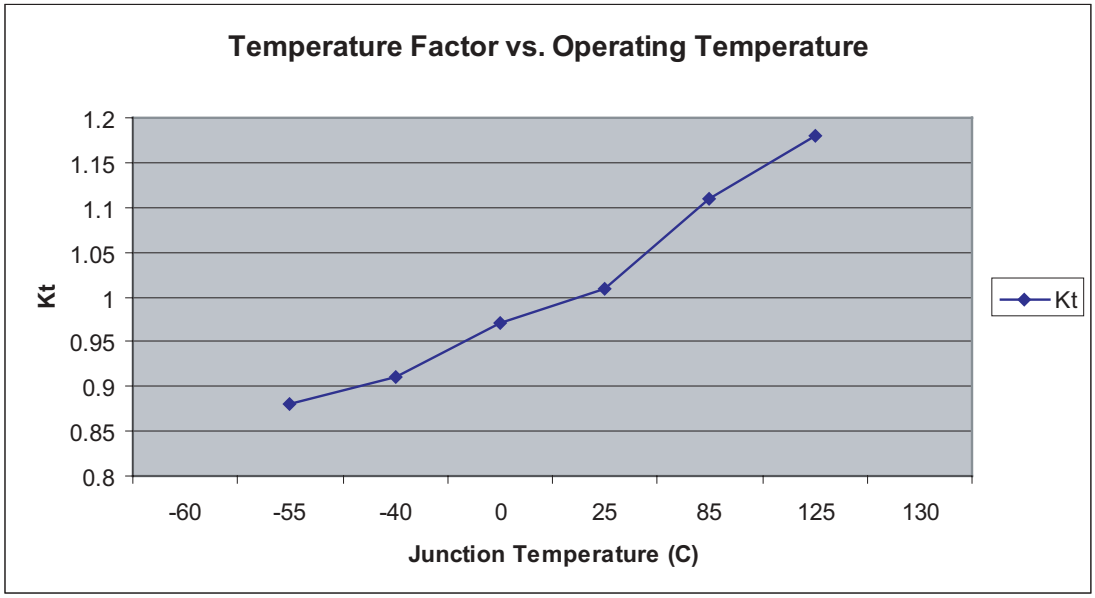


Figure 44: Temperature Factor vs. Operating Temperature



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Power vs. Operating Frequency

The basic power equation which best models power consumption is given below:

$$P_{TOTAL} = 0.350 + f[0.0031\ \eta_{LC} + 0.0948\ \eta_{CKBF} + 0.01\ \eta_{CLBF} + 0.0263\ \eta_{CKLD} + 0.543\ \eta_{RAM} + 0.20\ \eta_{PLL} + 0.0035\ \eta_{INP} + 0.0257\ \eta_{OUTP}]\ (mW)$$

Where:

η_{LC} is the total number of logic cells in the design

η_{CKBF} = # of clock buffers

η_{CLBF} = # of column clock buffers

η_{CKLD} = # of loads connected to the column clock buffers

η_{RAM} = # of RAM blocks

η_{PLL} = # of PLLs

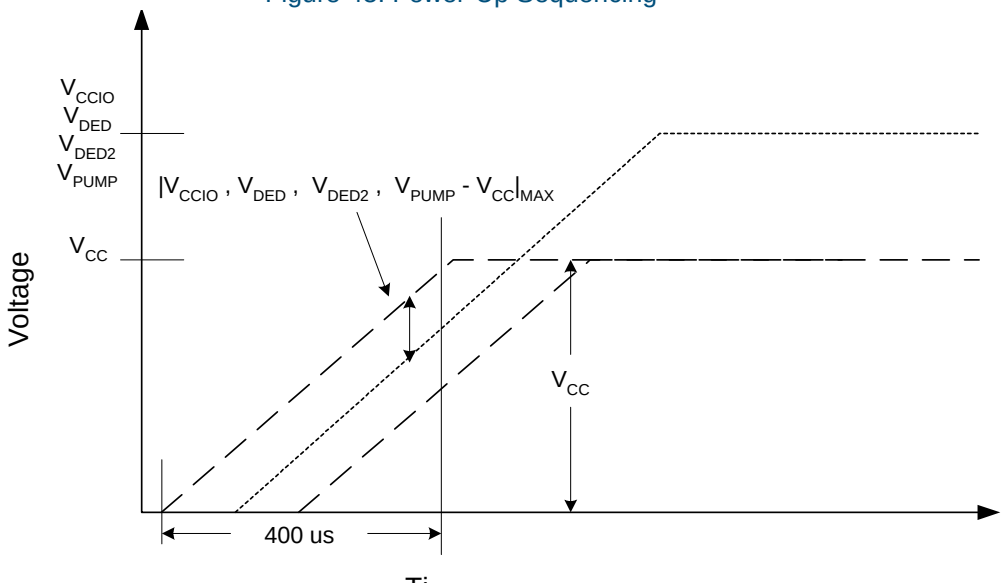
η_{INP} is the number of input pins

η_{OUTP} is the number of output pins

NOTE: To learn more about power consumption, see QuickLogic Application Note 60 at http://www.quicklogic.com/images/appnote60.pdf.

Power-up Sequencing

Figure 45: Power-Up Sequencing



When powering up a device, the $V_{CC}/V_{CCIO}/V_{DED}/V_{DED2}$ rails must take 400 µs or longer to reach the maximum value (refer to **Figure 45**).

NOTE: Ramping V_{CC}, V_{CCIO}, V_{PUMP}, V_{DED}, or V_{DED2} faster than 400 µs can cause the device to behave improperly.

For users with a limited power budget, ensure V_{CCIO}, V_{DED}, V_{DED2}, and V_{PUMP} are within 500 mV of V_{CC} when ramping up the power supplies.

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Pin Descriptions

Table 31: Pin Descriptions

Pin	Direction	Function	Description
JTAG Pin Descriptions			
TDI/RSI	I	Test Data In for JTAG/RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VDED2 if unused
TRSTB/RRO	I/0	Active low Reset for JTAG/RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused
TMS	I	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VDED2 if not used for JTAG
TCK	I	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VDED2 or GND if not used for JTAG
TDO/RCO	O	Test data out for JTAG/RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization. The output voltage drive is specified by VDED.
Dedicated Pin Descriptions			
CLK	I	Global clock network pin	Low skew global clock. This pin provides access to a dedicated, distributed network capable of driving the CLOCK, SET, RESET, F1, and A2 inputs to the Logic Cell, READ, and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, CLOCK of the ECUs, and Output Enables of the I/Os. The voltage tolerance of this pin is specified by VDED.
I/O(A)	I/O	Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The A inside the parenthesis means that the I/O is located in Bank A. If an I/O is not used, SpDE (Quick*Works* Tool) provides the option of tying that pin to GND, VCC, or TriState.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The A inside the parenthesis means that VCCIO is located in BANK A. Every I/O pin in Bank A will be tolerant of VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V. VCCIO powers the the PLLOUT pins.
GND	I	Ground pin	Connect to ground.
PLLIN	I	PLL clock input	Clock input for PLL. The voltage tolerance of this pin is specified by VDED.
DEDCLK	I	Dedicated clock pin	Very low skew global clock. This pin provides access to a dedicated, distributed clock network capable of driving the CLOCK inputs of all sequential elements of the device (e.g., RAM, Flip Flops). The voltage tolerance of this pin is specified by VDED.
GNDPLL	I	Ground pin for PLL	Connect to GND.

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Table 31: Pin Descriptions (Continued)

Pin	Direction	Function	Description
INREF(A)	I	Differential reference voltage	The INREF is the reference voltage pin for GTL+, SSTL2, and STTL3 standards. Follow the recommendations provided in **Table 19** for the appropriate standard. The A inside the parenthesis means that INREF is located in BANK A. This pin should be tied to GND if voltage referenced standards are not used.
PLLOUT	O	PLL output pin	Dedicated PLL output pin. Must be left unconnected if PLL is powered up and not held in reset, since PLLOUT will be driving the PLL-derived clock. May be left unconnected if PLL is held in reset or not powered up. PLLOUT pin is driven by VCCIO. For a list of each PLLOUT pin and the VCCIO pin that powers it see **Table 32**.
IOCTRL(A)	I	Highdrive input	This pin provides fast RESET, SET, CLOCK, and ENABLE access to the I/O cell flip-flops, providing fast clock-to-out and fast I/O response times. This pin can also double as a high-drive pin to the internal logic cells. The A inside the parenthesis means that IOCTRL is located in Bank A. There is an internal pulldown resistor to GND on this pin. This pin should be tied to GND if it is not used. For backwards compatibility with QL5632/QL5732, it can be tied to VDED or GND. If tied to VDED, it will draw no more than 20 µA per IOCTRL pin due to current through the pulldown resistor. The voltage tolerance of this pin is specified by VDED. Note that the 208 PQFP package has no I/O control pins.
VPUMP	I	Charge Pump Disable	This pin disables the internal charge pump for lower static power consumption. To disable the charge pump, connect VPUMP to 3.3 V. If the Disable Charge Pump feature is not used, connect VPUMP to GND. For backwards compatibility with QL5632/QL5732 devices, connect VPUMP to GND.
VDED	I	Voltage tolerance for clocks, TDO JTAG output, and IOCTRL	This pin specifies the input voltage tolerance for CLK, DEDCLK, PLLIN, and IOCTRL dedicated input pins, as well as the output voltage drive TDO JTAG pins. If the PLLs are used, VDED must be the same as VCCPLL. The legal range for VDED is between 1.71 V and 3.6 V. For backwards compatibility with QL5632/QL5732 devices, connect VDED to 2.5 V.

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Table 31: Pin Descriptions (Continued)

Pin	Direction	Function	Description
VDED2	I	Voltage tolerance for JTAG pins (TDI, TMS, TCK, and TRSTB)	These pins specify the input voltage tolerance for the JTAG input pins. The legal range for VDED2 is between 1.71 V and 3.6 V. These do not specify output voltage of the JTAG output, TDO. Refer to the VDED pin section for specifying the JTAG output voltage.
VCCPLL	I	Power Supply pin for PLL	Connect to 2.5 V or 3.3 V supply. For backwards compatibility with QL5632/QL5732 devices, connect to 2.5 V. To minimize static power consumption when designs do not utilize the PLLs, you may connect VCCPLL to GND. If VCCPLL is grounded, the PLL is disabled.
PLL_RESET	I	PLL reset pin	If PLL_RESET is asserted, then CLKNET_OUT and PLLPAD_OUT are reset to 0. This signal must be asserted and then released in order for the LOCK_DETECT to work. If a PLL module is not used, then the associated PLLRST<x> must be connected to VDED.

Table 32: PLLOUT Pin Supply Voltage

PLLOUT	VCCIO
PLLOUT(0)	VCCIO(E)
PLLOUT(1)	VCCIO(B)
PLLOUT(2)	VCCIO(A)
PLLOUT(3)	VCCIO(F)

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Figure 46: QL5842 I/O Banks with Relevant Pins

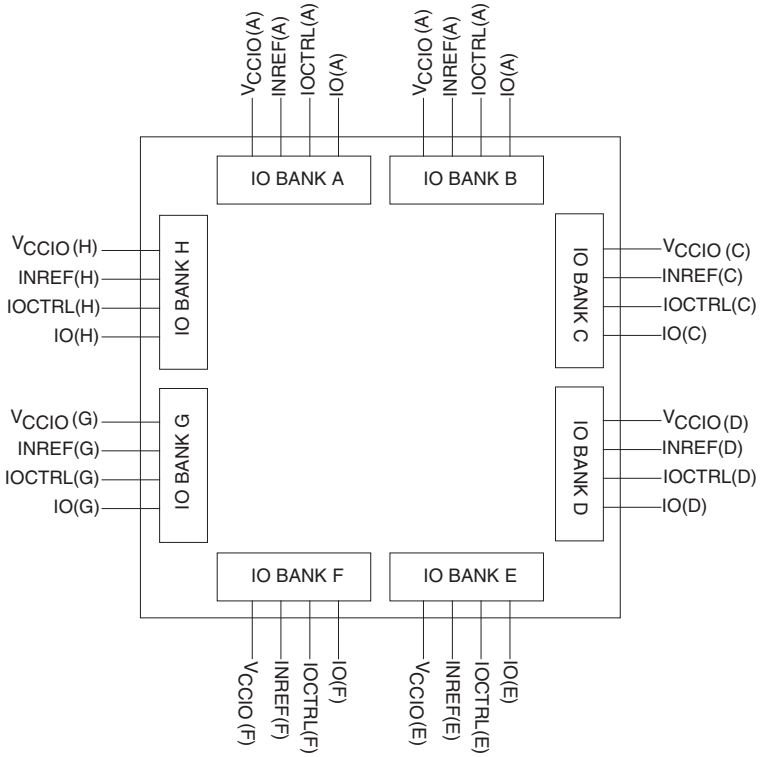
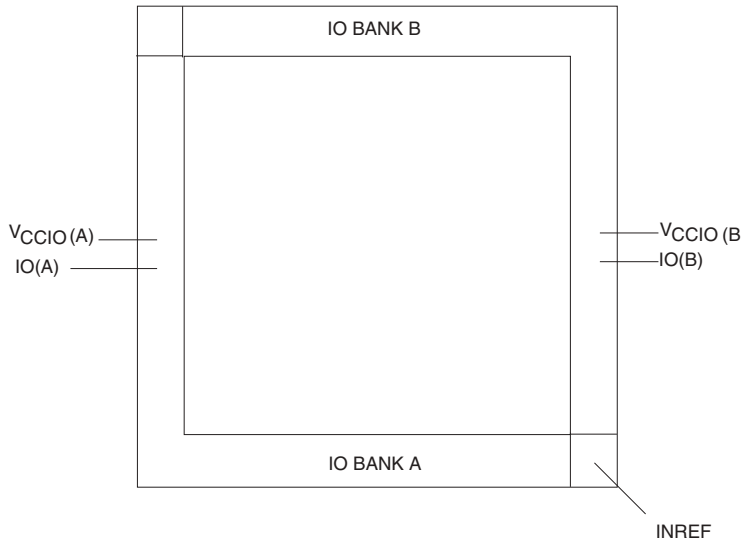


Figure 1: QL5822 I/O Banks with Relevant Pins



Recommended Unused Pin Terminations for QL58x2 Device Family

All unused, general purpose I/O pins can be tied to VCC, GND, or HIZ (high impedance) internally using the Configuration Editor. This option is given in the bottom-right corner of the placement window. To use the Placement Editor, choose **Constraint > Fix Placement** in the **Option** pull-down menu of SpDE.

The rest of the pins should be terminated at the board level in the manner presented in **Table 33**.

Table 33: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
PLLOUT<x>[a]	In earlier versions, the recommendation for unused PLLOUT pins was that they be connected to VCC or GND. This was acceptable for Rev. D (and earlier) silicon, including all 0.25 µm devices. For Rev. G (and later) silicon this is not correct. Unused PLLOUT pins should be left unconnected. Used PLLOUT pins will normally be connected to inputs, but can also be left unconnected. For the truth table of PLLOUT connections, refer to **Table 34**.
IOCTRL<y>[b]	There is an internal pulldown resistor to GND on this pin. This pin should be tied to GND if it is not used. For backwards compatibility with Eclipse, it can be tied to VDED or GND. If tied to VDED, it will draw no more than 20 µA per IOCTRL pin due to current through the pulldown resistor.
CLK/PLLIN<x>	Any unused clock pins should be connected to VDED or GND.
PLLRST<x>	If a PLL module is not used, then the associated PLLRST<x> must be connected to VDED or GND. If VCCPLL is grounded, then PLLRST must be grounded also. If VCCPLL is driven by 2.5 V or 3.3 V, PLLRST must be driven by the same voltage.
INREF<y>	If an I/O bank does not require the use of the INREF signal the pin should be connected to GND.

a. x represents a number.
b. y represents an alphabetical character.

Table 34: Recommended PLLOUT Terminations Truth Table

PLL_RESET	Recommended PLLOUT Termination
0	Must be left unconnected.
1	May be left unconnected, or connected to GND. Must not be connected to VCC.

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QL5822 - 144 TQFP Pinout Diagram

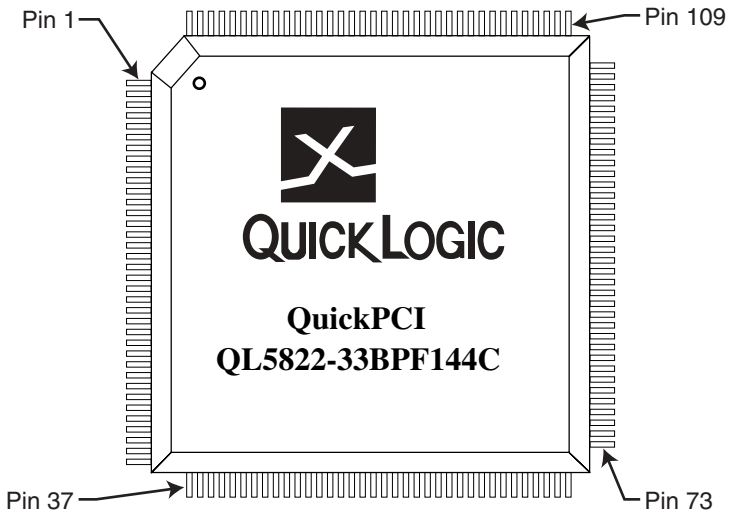

Figure 2: Top View of 144 Pin TQFP

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QL5822 - 144 TQFP Pinout Table

Table 35: QL5822 - 144 TQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GND	37	IO(A)	73	IO(A)	109	GND
2	GND	38	GND	74	IO(B)	110	CBEN(2)
3	IO(A)	39	IO(A)	75	GND	111	VCCIO(B)
4	IO(A)	40	VCCIO(A)	76	IO(B)	112	FRAMEN
5	IO(A)	41	IO(A)	77	RSTN	113	DEVSELN
6	IO(A)	42	IO(A)	78	GNTN	114	TRDYN
7	VCC	43	IO(A)	79	VCC	115	IRDYN
8	IO(A)	44	IO(A)	80	REQN	116	STOPN
9	IO(A)	45	IO(A)	81	AD(31)	117	PERRN
10	IO(A)	46	IO(A)	82	INREF	118	SERRN
11	IO(A)	47	IO(A)	83	AD(30)	119	PAR
12	IO(A)	48	IO(A)	84	AD(29)	120	VCC
13	VCCIO(A)	49	VCCIO(A)	85	AD(28)	121	CBEN(1)
14	IO(A)	50	IO(A)	86	VCCIO(B)	122	VCCIO(B)
15	TDI	51	IO(A)	87	AD(27)	123	AD(15)
16	CLK(0)	52	VCC	88	AD(26)	124	AD(14)
17	CLK(1)	53	TRSTB	89	AD(25)	125	VCC
18	VCC	54	VDED2	90	(PCI)CLK	126	TCK
19	IO(A)	55	IO(A)	91	CLK(3)	127	VDED2
20	VDED	56	IO(A)	92	VCC	128	AD(13)
21	IO(A)	57	IO(A)	93	CLK(4)	129	AD(12)
22	IO(A)	58	GND	94	TMS	130	GND
23	GND	59	IO(A)	95	AD(24)	131	AD(11)
24	VCCIO(A)	60	VCC	96	GND	132	AD(10)
25	IO(A)	61	IO(A)	97	VCCIO(B)	133	AD(9)
26	IO(A)	62	IO(A)	98	CBEN(3)	134	AD(8)
27	IO(A)	63	IO(A)	99	IDSEL	135	CBEN(0)
28	IO(A)	64	IO(A)	100	AD(23)	136	AD(7)
29	IO(A)	65	IO(A)	101	AD(22)	137	AD(6)
30	IO(A)	66	IO(A)	102	AD(21)	138	AD(5)
31	IO(A)	67	IO(A)	103	AD(20)	139	AD(4)
32	IO(A)	68	IO(A)	104	AD(19)	140	AD(3)
33	IO(A)	69	VCCIO(A)	105	AD(18)	141	VCCIO(B)
34	TDO	70	IO(A)	106	AD(17)	142	AD(2)
35	GND	71	VPUMP	107	GND	143	AD(1)
36	IO(A)	72	IO(A)	108	AD(16)	144	AD(0)

VCCIO(B) must be connected to VCCIO(PCI) 3.3 V.

Summary: 49 PCI pins, 52 user I/O, and 4 GCLK.

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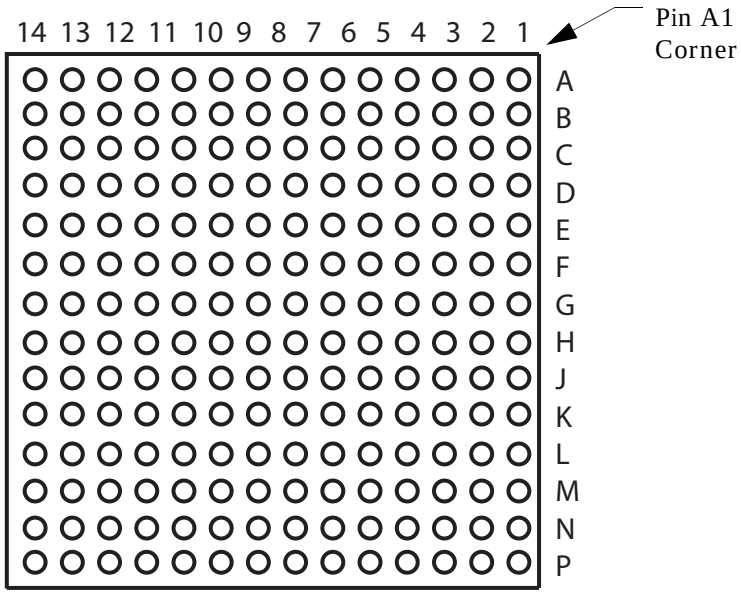
QL5822 - 196 TFBGA Pinout Diagram

Top

Bottom



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QL5822 - 196 TFBGA Pinout Table

Table 36: QL5822 - 196 TFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	AD(23)	C13	IO(A)	F11	IO(A)	J9	GND	M7	VCC
A2	CBEN(3)	C14	IO(A)	F12	IO(A)	J10	GND	M8	IO(A)
A3	AD(25)	D1	STOPN	F13	IO(A)	J11	IO(A)	M9	IO(A)
A4	AD(27)	D2	IRDYN	F14	IO(A)	J12	IO(A)	M10	IO(A)
A5	AD(24)	D3	AD(16)	G1	AD(14)	J13	IO(A)	M11	IO(A)
A6	AD(28)	D4	IDSEL	G2	TCK	J14	IO(A)	M12	IO(A)
A7	CLK(4)	D5	REQN	G3	CBEN(1)	K1	CBEN(0)	M13	IO(A)
A8	CLK(2)	D6	VCCIO(B)	G4	VCC	K2	AD(6)	M14	IO(A)
A9	AD(31)	D7	VCCIO(B)	G5	GND	K3	AD(7)	N1	IO(A)
A10	RSTN	D8	VDED	G6	GND	K4	IO(A)	N2	IO(A)
A11	INREF	D9	VCCIO(B)	G7	GND	K5	VCCIO(B)	N3	IO(A)
A12	IO(B)	D10	IO(B)	G8	GND	K6	VCCIO(A)	N4	IO(A)
A13	IO(B)	D11	IO(A)	G9	GND	K7	GND	N5	IO(A)
A14	IO(B)	D12	VPUMP	G10	GND	K8	GND	N6	IO(A)
B1	AD(19)	D13	IO(A)	G11	IO(A)	K9	VCCIO(A)	N7	IO(A)
B2	AD(21)	D14	IO(A)	G12	VCC	K10	VCCIO(A)	N8	IO(A)
B3	AD(20)	E1	SERRN	G13	IO(A)	K11	IO(A)	N9	IO(A)
B4	GNTN	E2	PERRN	G14	IO(A)	K12	IO(A)	N10	IO(A)
B5	AD(26)	E3	FRAMEN	H1	AD(11)	K13	IO(A)	N11	IO(A)
B6	TMS	E4	CBEN(2)	H2	AD(12)	K14	IO(A)	N12	TDO
B7	VCC	E5	VCCIO(B)	H3	VDED2	L1	AD(4)	N13	IO(A)
B8	AD(30)	E6	GND	H4	VCCIO(B)	L2	AD(3)	N14	IO(A)
B9	IO(B)	E7	GND	H5	GND	L3	AD(5)	P1	IO(A)
B10	IO(B)	E8	GND	H6	GND	L4	AD(0)	P2	IO(A)
B11	IO(B)	E9	GND	H7	GND	L5	IO(A)	P3	IO(A)
B12	IO(B)	E10	IO(B)	H8	GND	L6	IO(A)	P4	IO(A)
B13	IO(B)	E11	VCCIO(A)	H9	GND	L7	VCCIO(A)	P5	IO(A)
B14	IO(B)	E12	IO(A)	H10	GND	L8	VDED	P6	CLK(0)
C1	DEVSELN	E13	IO(A)	H11	VCCIO(A)	L9	VDED	P7	CLK(1)
C2	AD(17)	E14	VCC	H12	TRSTB	L10	VCCIO(A)	P8	IO(A)
C3	AD(18)	F1	AD(15)	H13	VDED2	L11	VCC	P9	IO(A)
C4	VCC	F2	VCC	H14	VCC	L12	IO(A)	P10	IO(A)
C5	AD(22)	F3	TRDYN	J1	AD(10)	L13	IO(A)	P11	IO(A)
C6	VCC	F4	PAR	J2	AD(9)	L14	IO(A)	P12	IO(A)
C7	AD(29)	F5	VCCIO(B)	J3	AD(8)	M1	AD(2)	P13	IO(A)
C8	(PCI)CLK	F6	GND	J4	VCC	M2	AD(1)	P14	IO(A)
C9	IO(B)	F7	GND	J5	AD(13)	M3	IO(B)		
C10	VCC	F8	GND	J6	GND	M4	GND		
C11	IO(B)	F9	GND	J7	GND	M5	VCC		
C12	IO(A)	F10	IO(A)	J8	GND	M6	TDI		

VCCIO(B) must be connected to VCCIO(PCI) 3.3 V.

Summary: 49 PCI pins, 76 user I/O, and 4 GCLK.

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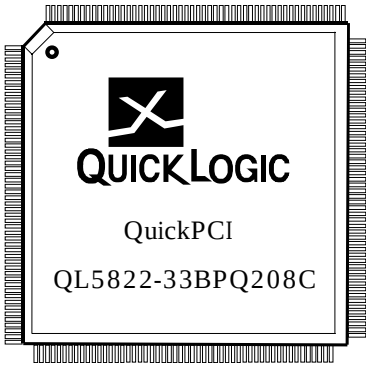
QL5822 - 208 PQFP Pinout Diagram

Top



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QL5822 - 208 PQFP Pinout Table

Table 37: QL5822 - 208 PQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O(A)	36	I/O(A)	71	I/O(A)	106	I/O(B)	141	AD(26)	176	PAR
2	I/O(A)	37	I/O(A)	72	VCCIO(A)	107	I/O(B)	142	AD(25)	177	VCCIO(B)
3	GND	38	I/O(A)	73	I/O(A)	108	GND	143	AD(24)	178	GND
4	GND	39	I/O(A)	74	I/O(A)	109	I/O(B)	144	CBEN(3)	179	CBEN(1)
5	I/O(A)	40	I/O(A)	75	GND	110	I/O(B)	145	I/O(B)	180	AD(15)
6	I/O(A)	41	I/O(A)	76	VCC	111	VCCIO(B)	146	VCC	181	AD(14)
7	I/O(A)	42	I/O(A)	77	I/O(A)	112	I/O(B)	147	IDSEL	182	VCC
8	VCCIO(A)	43	I/O(A)	78	TRSTB	113	VCC	148	AD(23)	183	TCK
9	I/O(A)	44	VCCIO(A)	79	VDED2	114	I/O(B)	149	AD(22)	184	VDED2
10	I/O(A)	45	I/O(A)	80	I/O(A)	115	I/O(B)	150	VCCIO(B)	185	AD(13)
11	I/O(A)	46	VCC	81	I/O(A)	116	I/O(B)	151	AD(21)	186	AD(12)
12	VCC	47	I/O(A)	82	I/O(A)	117	I/O(B)	152	AD(20)	187	AD(11)
13	I/O(A)	48	I/O(A)	83	GND	118	INREF	153	GND	188	GND
14	I/O(A)	49	GND	84	VCCIO(A)	119	I/O(B)	154	AD(19)	189	VCCIO(B)
15	I/O(A)	50	TDO	85	I/O(A)	120	I/O(B)	155	I/O(B)	190	AD(10)
16	I/O(A)	51	I/O(A)	86	VCC	121	I/O(B)	156	GND	191	AD(9)
17	I/O(A)	52	GND	87	I/O(A)	122	VCCIO(B)	157	I/O(B)	192	AD(8)
18	I/O(A)	53	I/O(A)	88	I/O(A)	123	GND	158	I/O(B)	193	CBEN(0)
19	VCCIO(A)	54	I/O(A)	89	VCC	124	RSTN	159	I/O(B)	194	I/O(B)
20	I/O(A)	55	I/O(A)	90	I/O(A)	125	GNTN	160	GND	195	VCC
21	GND	56	VDED	91	I/O(A)	126	REQN	161	AD(18)	196	AD(7)
22	I/O(A)	57	I/O(A)	92	I/O(A)	127	I/O(B)	162	VCCIO(B)	197	AD(6)
23	TDI	58	GND	93	I/O(A)	128	CLK(2)	163	AD(17)	198	AD(5)
24	CLK(0)	59	I/O(A)	94	I/O(A)	129	VDED	164	AD(16)	199	AD(4)
25	CLK(1)	60	VCCIO(A)	95	I/O(A)	130	CLK(3)	165	VCC	200	AD(3)
26	VCC	61	I/O(A)	96	I/O(A)	131	VCC	166	CBEN(2)	201	AD(2)
27	I/O(A)	62	I/O(A)	97	I/O(A)	132	(PCI)CLK	167	FRAMEN	202	AD(1)
28	I/O(A)	63	I/O(A)	98	VCCIO(A)	133	TMS	168	IRDYN	203	VCCIO(B)
29	VDED	64	I/O(A)	99	I/O(A)	134	AD(31)	169	TRDYN	204	GND
30	I/O(A)	65	I/O(A)	100	I/O(A)	135	AD(30)	170	I/O(B)	205	AD(0)
31	I/O(A)	66	I/O(A)	101	VPUMP	136	AD(29)	171	DEVSELN	206	I/O(B)
32	I/O(A)	67	I/O(A)	102	I/O(A)	137	GND	172	STOPN	207	I/O(B)
33	GND	68	I/O(A)	103	I/O(A)	138	VCCIO(B)	173	PERRN	208	I/O(B)
34	VCCIO(A)	69	I/O(A)	104	GND	139	AD(28)	174	SERRN		
35	I/O(A)	70	I/O(A)	105	I/O(B)	140	AD(27)	175	VCC		

VCCIO(B) must be connected to VCCIO(PCI) 3.3 V.

Summary: 49 PCI pins, 95 user I/O, and 4 GCLK.

NOTE: The pinout is compatible within the 58xx family, however, not with QL5632.

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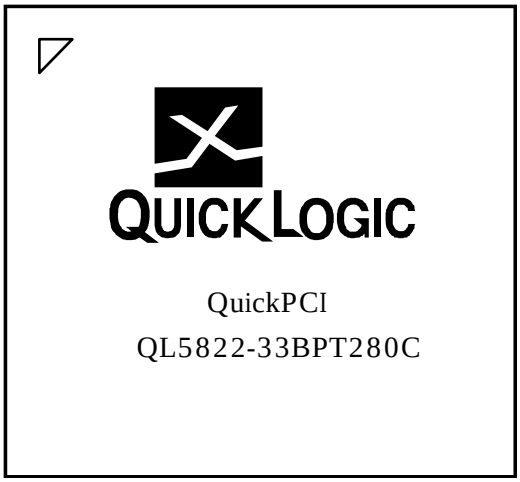
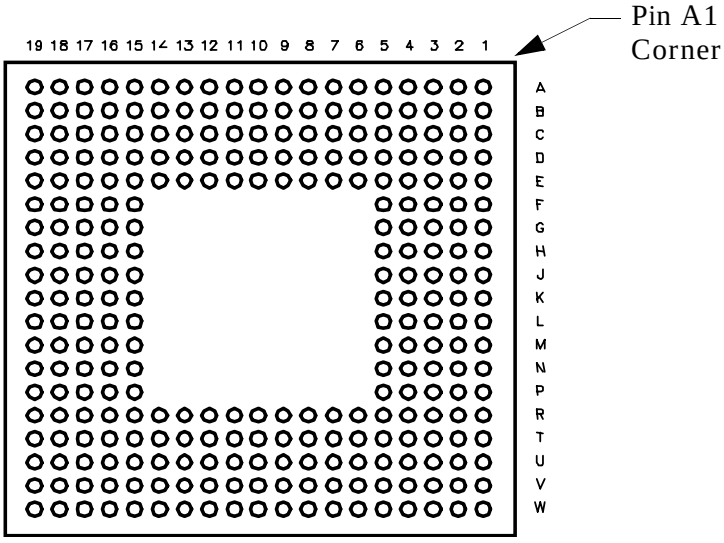
QL5822 - 280 LFBGA Pinout Diagram

Top



Bottom



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QL5822 - 280 LFBGA Pinout Table

Table 38: QL5822 - 280 LFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	NC	C10	I/O(B)	E19	NC	K16	I/O(A)	R4	I/O(B)	U13	I/O(A)
A2	GND	C11	VCCIO(B)	F1	NC	K17	I/O(A)	R5	GND	U14	NC
A3	AD(18)	C12	I/O(B)	F2	NC	K18	I/O(A)	R6	GND	U15	VCCIO(A)
A4	AD(20)	C13	I/O(B)	F3	SERRN	K19	TRSTB	R7	VCC	U16	I/O(A)
A5	IDSEL	C14	I/O(B)	F4	DEVSELN	L1	AD(4)	R8	VCC	U17	TDO
A6	NC	C15	VCCIO(B)	F5	GND	L2	AD(5)	R9	GND	U18	NC
A7	AD(26)	C16	I/O(B)	F15	VCC	L3	VCCIO(B)	R10	GND	U19	I/O(A)
A8	AD(30)	C17	I/O(B)	F16	NC	L4	AD(6)	R11	VCC	V1	NC
A9	RSTN	C18	I/O(B)	F17	I/O(A)	L5	VCC	R12	VCC	V2	GND
A10	CLK(3)	C19	I/O(B)	F18	I/O(A)	L15	GND	R13	VCC	V3	GND
A11	I/O(B)	D1	TRDYN	F19	I/O(A)	L16	I/O(A)	R14	VDED	V4	I/O(A)
A12	I/O(B)	D2	IRDYN	G1	AD(14)	L17	VCCIO(A)	R15	GND	V5	I/O(A)
A13	I/O(B)	D3	AD(16)	G2	AD(15)	L18	I/O(A)	R16	I/O(A)	V6	NC
A14	NC	D4	AD(23)	G3	NC	L19	I/O(A)	R17	VCCIO(A)	V7	I/O(A)
A15	I/O(B)	D5	AD(24)	G4	PAR	M1	AD(0)	R18	I/O(A)	V8	I/O(A)
A16	I/O(B)	D6	AD(25)	G5	VCC	M2	AD(1)	R19	I/O(A)	V9	I/O(A)
A17	I/O(B)	D7	AD(29)	G15	VCC	M3	AD(2)	T1	I/O(B)	V10	CLK(1)
A18	NC	D8	GNTN	G16	I/O(A)	M4	AD(3)	T2	I/O(B)	V11	NC
A19	NC	D9	(PCI) CLK	G17	I/O(A)	M5	VCC	T3	I/O(A)	V12	I/O(A)
B1	NC	D10	I/O(B)	G18	I/O(A)	M15	VDED	T4	I/O(A)	V13	I/O(A)
B2	NC	D11	I/O(B)	G19	I/O(A)	M16	NC	T5	I/O(A)	V14	NC
B3	AD(19)	D12	I/O(B)	H1	AD(11)	M17	I/O(A)	T6	NC	V15	I/O(A)
B4	AD(21)	D13	INREF	H2	AD(12)	M18	I/O(A)	T7	I/O(A)	V16	I/O(A)
B5	CBEN(3)	D14	I/O(B)	H3	AD(13)	M19	I/O(A)	T8	I/O(A)	V17	I/O(A)
B6	NC	D15	I/O(B)	H4	CBEN(1)	N1	NC	T9	I/O(A)	V18	GND
B7	AD(27)	D16	I/O(A)	H5	VCC	N2	I/O(B)	T10	I/O(A)	V19	NC
B8	AD(31)	D17	I/O(A)	H15	VCC	N3	I/O(B)	T11	NC	W1	NC
B9	TMS	D18	I/O(A)	H16	VDED2	N4	I/O(B)	T12	I/O(A)	W2	NC
B10	CLK(2)	D19	I/O(A)	H17	I/O(A)	N5	VCC	T13	I/O(A)	W3	I/O(A)
B11	I/O(B)	E1	PERRN	H18	I/O(A)	N15	VCC	T14	I/O(A)	W4	I/O(A)
B12	I/O(B)	E2	STOPN	H19	I/O(A)	N16	I/O(A)	T15	I/O(A)	W5	I/O(A)
B13	NC	E3	VCCIO(B)	J1	AD(8)	N17	I/O(A)	T16	I/O(A)	W6	I/O(A)
B14	I/O(B)	E4	FRAMEN	J2	AD(9)	N18	NC	T17	NC	W7	I/O(A)
B15	I/O(B)	E5	GND	J3	VCCIO(B)	N19	NC	T18	I/O(A)	W8	I/O(A)
B16	I/O(B)	E6	VCC	J4	AD(10)	P1	I/O(B)	T19	I/O(A)	W9	TDI
B17	NC	E7	VCC	J5	GND	P2	I/O(B)	U1	I/O(A)	W10	I/O(A)
B18	GND	E8	VDED	J15	VCC	P3	NC	U2	I/O(A)	W11	I/O(A)
B19	NC	E9	VCC	J16	I/O(A)	P4	NC	U3	NC	W12	I/O(A)
C1	CBEN(2)	E10	GND	J17	VCCIO(A)	P5	VCC	U4	I/O(A)	W13	I/O(A)
C2	NC	E11	GND	J18	I/O(A)	P15	GND	U5	VCCIO(A)	W14	NC
C3	AD(17)	E12	VCC	J19	I/O(A)	P16	I/O(A)	U6	NC	W15	I/O(A)
C4	AD(22)	E13	VCC	K1	VDED2	P17	I/O(A)	U7	I/O(A)	W16	I/O(A)
C5	VCCIO(B)	E14	GND	K2	TCK	P18	I/O(A)	U8	I/O(A)	W17	I/O(A)
C6	NC	E15	VPUMP	K3	AD(7)	P19	I/O(A)	U9	VCCIO(A)	W18	I/O(A)
C7	AD(28)	E16	I/O(A)	K4	CBEN(0)	R1	I/O(B)	U10	CLK(0)	W19	NC
C8	REQN	E17	VCCIO(A)	K5	GND	R2	I/O(B)	U11	VCCIO(A)		
C9	VCCIO(B)	E18	NC	K15	GND	R3	VCCIO(B)	U12	I/O(A)		

VCCIO(B) must be connected to VCCIO(PCI) (3.3 V).

Summary: 49 PCI pins, 116 User I/O and 5 GCLK.

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QL5842 - 208 PQFP Pinout Diagram

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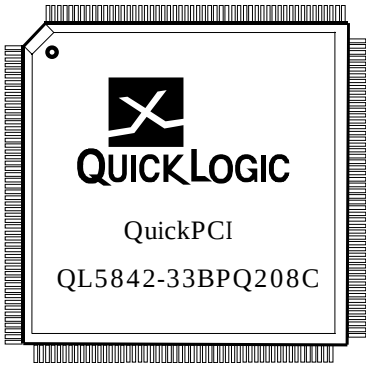

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QL5842 - 208 PQFP Pinout Table

Table 39: QL5842 - 208 PQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	PLLRST(3)	36	I/O(B)	71	I/O(C)	106	VCCPLL(1)	141	AD(26)	176	PAR
2	VCCPLL(3)	37	I/O(B)	72	VCCIO(C)	107	I/O(E)	142	AD(25)	177	VCCIO(G)
3	GND	38	I/O(B)	73	I/O(C)	108	GND	143	AD(24)	178	GND
4	GND	39	I/O(B)	74	I/O(C)	109	I/O(E)	144	CBEN(3)	179	CBEN(1)
5	I/O(A)	40	INREF(B)	75	GND	110	I/O(E)	145	INREF(F)	180	AD(15)
6	I/O(A)	41	I/O(B)	76	VCC	111	VCCIO(E)	146	VCC	181	AD(14)
7	I/O(A)	42	I/O(B)	77	I/O(C)	112	I/O(E)	147	IDSEL	182	VCC
8	VCCIO(A)	43	I/O(B)	78	TRSTB	113	VCC	148	AD(23)	183	TCK
9	I/O(A)	44	VCCIO(B)	79	VDED2	114	I/O(E)	149	AD(22)	184	VDED2
10	I/O(A)	45	I/O(B)	80	I/O(D)	115	I/O(E)	150	VCCIO(F)	185	AD(13)
11	I/O(A)	46	VCC	81	I/O(D)	116	I/O(E)	151	AD(21)	186	AD(12)
12	VCC	47	I/O(B)	82	I/O(D)	117	I/O(E)	152	AD(20)	187	AD(11)
13	INREF(A)	48	I/O(B)	83	GND	118	INREF(E)	153	GND	188	GND
14	I/O(A)	49	GND	84	VCCIO(D)	119	I/O(E)	154	AD(19)	189	VCCIO(H)
15	I/O(A)	50	TDO	85	I/O(D)	120	I/O(E)	155	PLLOUT(3)	190	AD(10)
16	I/O(A)	51	PLLOUT(1)	86	VCC	121	I/O(E)	156	GNDPLL(0)	191	AD(9)
17	I/O(A)	52	GNDPLL(2)	87	I/O(D)	122	VCCIO(E)	157	GND	192	AD(8)
18	I/O(A)	53	GND	88	I/O(D)	123	GND	158	VCCPLL(0)	193	CBEN(0)
19	VCCIO(A)	54	VCCPLL(2)	89	VCC	124	RSTN	159	PLLRST(0)	194	INREF(H)
20	I/O(A)	55	PLLRST(2)	90	I/O(D)	125	GNTN	160	GND	195	VCC
21	GND	56	VDED	91	I/O(D)	126	REQN	161	AD(18)	196	AD(7)
22	I/O(A)	57	I/O(C)	92	I/O(D)	127	CLK(5) PLLIN(3)	162	VCCIO(G)	197	AD(6)
23	TDI	58	GND	93	INREF(D)	128	CLK(6)	163	AD(17)	198	AD(5)
24	CLK(0)	59	I/O(C)	94	I/O(D)	129	VDED	164	AD(16)	199	AD(4)
25	CLK(1)	60	VCCIO(C)	95	I/O(D)	130	CLK(7)	165	VCC	200	AD(3)
26	VCC	61	I/O(C)	96	I/O(D)	131	VCC	166	CBEN(2)	201	AD(2)
27	CLK(2) PLLIN(2)	62	I/O(C)	97	I/O(D)	132	(PCI)CLK	167	FRAMEN	202	AD(1)
28	CLK(3) PLLIN(1)	63	I/O(C)	98	VCCIO(D)	133	TMS	168	IRDYN	203	VCCIO(H)
29	VDED	64	I/O(C)	99	I/O(D)	134	AD(31)	169	TRDYN	204	GND
30	CLK(4) PLLIN(0)	65	I/O(C)	100	I/O(D)	135	AD(30)	170	INREF(G)	205	AD(0)
31	I/O(B)	66	I/O(C)	101	VPUMP	136	AD(29)	171	DEVSELN	206	PLLOUT(2)
32	I/O(B)	67	I/O(C)	102	PLLOUT(0)	137	GND	172	STOPN	207	GND
33	GND	68	INREF(C)	103	GND	138	VCCIO(F)	173	PERRN	208	GNDPLL(3)
34	VCCIO(B)	69	I/O(C)	104	GNDPLL(1)	139	AD(28)	174	SERRN		
35	I/O(B)	70	I/O(C)	105	PLLRST(1)	140	AD(27)	175	VCC		

VCCIO(E), VCCIO(F), VCCIO(G), and VCCIO(H) must be connected to VCCIO(PCI) 3.3 V.

Summary: 49 PCI pins, 67 user I/O, and 8 GCLK.

NOTE: The pinout is compatible within the 58xx family, however, not with QL5632.

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QL5842 - 280 LFBGA Pinout Diagram

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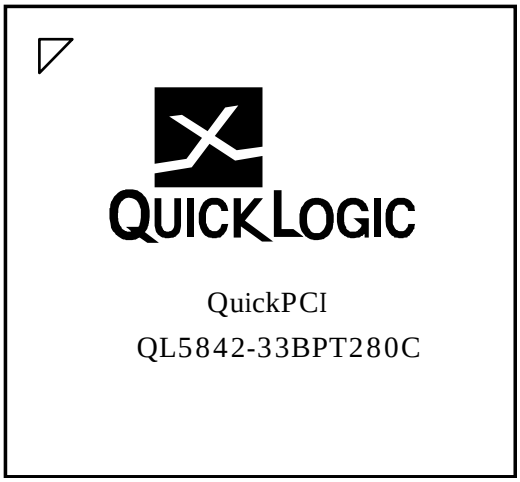
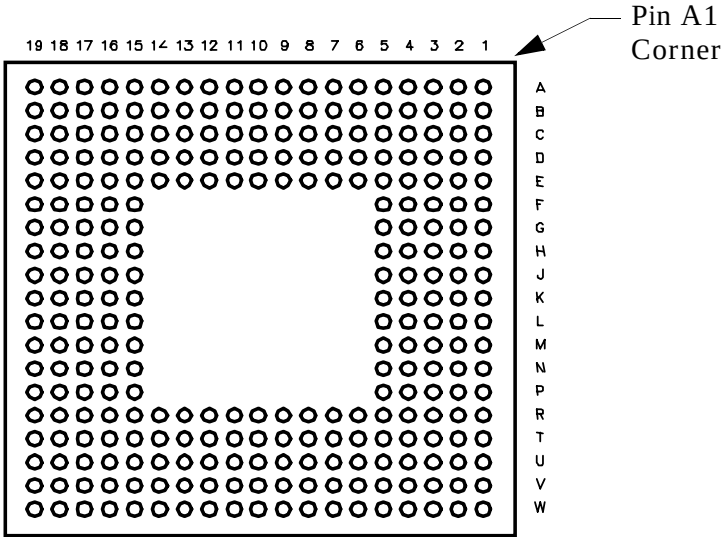


Bottom



QL5842 - 280 LFBGA Pinout Table

Table 40: QL5842 - 280 LFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	PLLOUT(3)	C10	CLK(5)/ PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	VCCIO(E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	AD(18)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	VCCIO(B)
A4	AD(20)	C13	I/O(E)	F3	SERRN	K19	TRSTB	R7	VCC	U16	I/O(B)
A5	IDSEL	C14	I/O(E)	F4	DEVSELN	L1	AD(4)	R8	VCC	U17	TDO
A6	IOCTRL(F)	C15	VCCIO(E)	F5	GND	L2	AD(5)	R9	GND	U18	PLLRST(2)
A7	AD(26)	C16	I/O(E)	F15	VCC	L3	VCCIO(H)	R10	GND	U19	I/O(B)
A8	AD(30)	C17	I/O(E)	F16	IOCTRL(D)	L4	AD(6)	R11	VCC	V1	PLLOUT(2)
A9	RSTN	C18	I/O(E)	F17	I/O(D)	L5	VCC	R12	VCC	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	VCC	V3	GND
A11	I/O(E)	D1	TRDYN	F19	I/O(D)	L16	I/O(C)	R14	VDED	V4	I/O(A)
A12	I/O(E)	D2	IRDYN	G1	AD(14)	L17	VCCIO(C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	AD(16)	G2	AD(15)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	AD(23)	G3	IOCTRL(G)	L19	I/O(C)	R17	VCCIO(C)	V7	I/O(A)
A15	I/O(E)	D5	AD(24)	G4	PAR	M1	AD(0)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	AD(25)	G5	VCC	M2	AD(1)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	AD(29)	G15	VCC	M3	AD(2)	T1	I/O(H)	V10	CLK(1)
A18	PLLRST(1)	D8	GNTN	G16	I/O(D)	M4	AD(3)	T2	I/O(H)	V11	CLK(4) DEDCLK/ PLLIN(0)
A19	GND	D9	(PCI) CLK	G17	I/O(D)	M5	VCC	T3	I/O(A)	V12	I/O(B)
B1	PLLRST(0)	D10	I/O(E)	G18	I/O(D)	M15	VDED	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	AD(19)	D12	I/O(E)	H1	AD(11)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	AD(21)	D13	INREF(E)	H2	AD(12)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	CBEN(3)	D14	I/O(E)	H3	AD(13)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	CBEN(1)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	AD(27)	D16	I/O(D)	H5	VCC	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	AD(31)	D17	I/O(D)	H15	VCC	N3	I/O(H)	T11	CLK(3/) PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	VDED2	N4	I/O(H)	T12	I/O(B)	W2	PLLRST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	VCC	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	PERRN	H18	I/O(D)	N15	VCC	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	STOPN	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	VCCIO(G)	J1	AD(8)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	FRAMEN	J2	AD(9)	N18	IOCTRL(C)	T17	VCCPLL(2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	VCCIO(G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	VCC	J4	AD(10)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	VCCPLL(1)	E7	VCC	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	VDED	J15	VCC	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	VCC	J16	I/O(C)	P4	INREF(H)	U3	VCCPLL(3)	W12	I/O(B)
C1	CBEN(2)	E10	GND	J17	VCCIO(D)	P5	VCC	U4	I/O(A)	W13	I/O(B)
C2	VCCPLL(0)	E11	GND	J18	I/O(D)	P15	GND	U5	VCCIO(A)	W14	IOCTRL(B)
C3	AD(17)	E12	VCC	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	AD(22)	E13	VCC	K1	VDED2	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	VCCIO(F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	VPUMP	K3	AD(7)	P19	I/O(C)	U9	VCCIO(A)	W18	I/O(B)
C7	AD(28)	E16	I/O(D)	K4	CBEN(0)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	REQN	E17	VCCIO(D)	K5	GND	R2	I/O(H)	U11	VCCIO(B)		
C9	VCCIO(F)	E18	INREF(D)	K15	GND	R3	VCCIO(H)	U12	I/O(B)		

VCCIO(F), VCCIO(G) and VCCIO(H) must be connected to VCCIO(PCI) (3.3 V).

Summary: 49 PCI pins, 115 User I/O and 8 GCLK.

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QL5842 - 484 PBGA Pinout Diagrams

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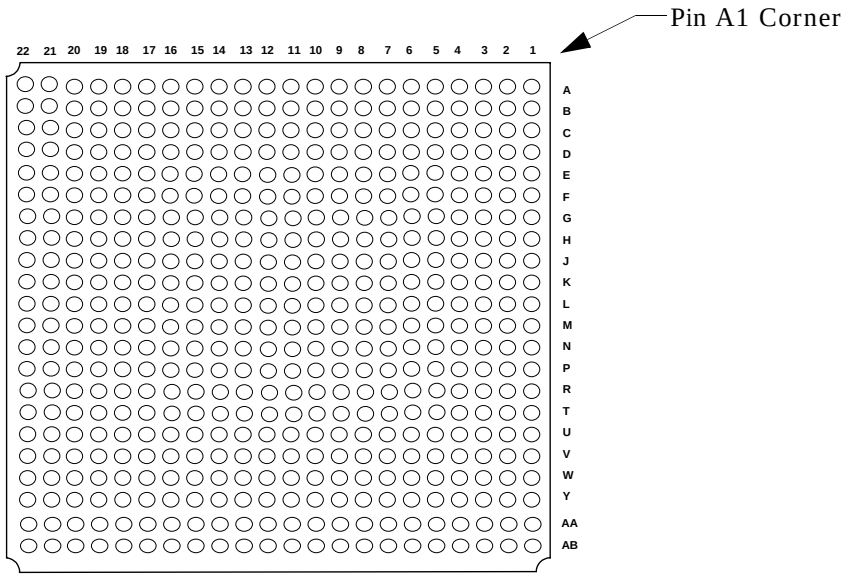

QL5842 - 484 PBGA Pinout Table

Table 41: QL5842 - 484 PBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	I/O(A)	C17	I/O(G)	F11	VCCIO(H)	J5	I/O(A)	L21	I/O(F)	P15	VDED
A2	PLLRST(3)	C18	AD(18)	F12	VCCIO(G)	J6	I/O(A)	L22	I/O(F)	P16	I/O(E)
A3	I/O(A)	C19	AD(23)	F13	AD(12)	J7	I/O(A)	M1	I/O(B)	P17	I/O(E)
A4	I/O(A)	C20	GNDPLL(0)	F14	VCCIO(PCI)	J8	VCC	M2	I/O(B)	P18	I/O(E)
A5	I/O(A)	C21	AD(27)	F15	N/C	J9	GND	M3	I/O(B)	P19	I/O(E)
A6	I/O(H)	C22	AD(30)	F16	VCCIO(G)	J10	VCC	M4	CLK(3)/ PLLIN(1)	P20	I/O(E)
A7	I/O(H)	D1	I/O(A)	F17	N/C	J11	VCC	M5	I/O(B)	P21	I/O(E)
A8	IOCTRL(H)	D2	I/O(A)	F18	GNTN	J12	GND	M6	VCCIO(B)	P22	I/O(E)
A9	AD(0)	D3	I/O(A)	F19	REQN	J13	VCC	M7	CLK(1)	R1	I/O(B)
A10	N/C	D4	I/O(A)	F20	IOCTRL(F)	J14	GND	M8	VCC	R2	INREF(B)
A11	N/C	D5	I/O(A)	F21	I/O(F)	J15	VCC	M9	VCC	R3	I/O(B)
A12	TCK	D6	I/O(H)	F22	IOCTRL(F)	J16	AD(29)	M10	GND	R4	I/O(B)
A13	AD(10)	D7	I/O(H)	G1	I/O(A)	J17	VCCIO(F)	M11	GND	R5	I/O(B)
A14	AD(13)	D8	I/O(H)	G2	I/O(A)	J18	I/O(F)	M12	GND	R6	I/O(B)
A15	SERRN	D9	I/O(H)	G3	I/O(A)	J19	I/O(F)	M13	GND	R7	I/O(B)
A16	I/O(G)	D10	AD(4)	G4	I/O(A)	J20	I/O(F)	M14	GND	R8	GND
A17	IRDYN	D11	AD(7)	G5	I/O(A)	J21	I/O(F)	M15	GND	R9	VCC
A18	AD(17)	D12	AD(8)	G6	I/O(A)	J22	I/O(F)	M16	GND	R10	VCC
A19	AD(20)	D13	AD(14)	G7	GND	K1	TDI	M17	I/O(E)	R11	GND
A20	GND	D14	CBEN(1)	G8	I/O(H)	K2	I/O(A)	M18	I/O(E)	R12	VDED
A21	PLLOUT(3)	D15	IOCTRL(G)	G9	I/O(H)	K3	I/O(A)	M19	I/O(E)	R13	VCC
A22	IDSEL	D16	CBEN(2)	G10	I/O(H)	K4	I/O(A)	M20	CLK(7)	R14	VCC
B1	I/O(A)	D17	AD(16)	G11	CBEN(0)	K5	I/O(A)	M21	CLK(5)/ PLLIN(3)	R15	GND
B2	GND	D18	AD(22)	G12	GND	K6	VCCIO(A)	M22	TMS	R16	I/O(D)
B3	GNDPLL(3)	D19	VCCPLL(0)	G13	I/O(G)	K7	I/O(A)	N1	I/O(B)	R17	VCCIO(E)
B4	GND	D20	AD(26)	G14	I/O(G)	K8	VCC	N2	I/O(B)	R18	I/O(E)
B5	I/O(A)	D21	AD(31)	G15	PAR	K9	VCC	N3	I/O(B)	R19	I/O(E)
B6	I/O(H)	D22	RSTN	G16	VPUMP	K10	GND	N4	I/O(B)	R20	I/O(E)
B7	I/O(H)	E1	IOCTRL(A)	G17	VCCIO(F)	K11	GND	N5	I/O(B)	R21	I/O(E)
B8	INREF(H)	E2	I/O(A)	G18	I/O(F)	K12	GND	N6	I/O(B)	R22	I/O(E)
B9	I/O(H)	E3	I/O(A)	G19	I/O(F)	K13	GND	N7	I/O(B)	T1	I/O(B)
B10	AD(3)	E4	I/O(A)	G20	I/O(F)	K14	VCC	N8	VCC	T2	I/O(B)
B11	AD(6)	E5	I/O(A)	G21	INREF(F)	K15	VCC	N9	VCC	T3	I/O(B)
B12	N/C	E6	I/O(H)	G22	I/O(F)	K16	I/O(F)	N10	GND	T4	I/O(B)
B13	N/C	E7	N/C	H1	I/O(A)	K17	I/O(F)	N11	GND	T5	I/O(B)
B14	N/C	E8	I/O(H)	H2	I/O(A)	K18	I/O(F)	N12	GND	T6	VCCIO(B)
B15	I/O(G))	E9	I/O(H)	H3	I/O(A)	K19	I/O(F)	N13	GND	T7	GND
B16	DEVSELN	E10	AD(5)	H4	I/O(A)	K20	I/O(F)	N14	VCC	T8	I/O(C)
B17	FRAMEN	E11	VDED2	H5	IOCTRL(A)	K21	I/O(F)	N15	VCC	T9	N/C
B18	AD(19)	E12	AD(9)	H6	VCCIO(A)	K22	I/O(F)	N16	I/O(E)	T10	TRSTB
B19	PLLRST(0)	E13	AD(15)	H7	I/O(H)	L1	CLK(4) DEDCLK/ PLLIN(0)	N17	VCCIO(E)	T11	GND
B20	CBEN(3)	E14	I/O(G)	H8	GND	L2	CLK(0)	N18	I/O(E)	T12	N/C
B21	AD(24)	E15	IOCTRL(G)	H9	VCC	L3	CLK(2)/ PLLIN(2)	N19	I/O(E)	T13	I/O(D)
B22	AD(28)	E16	STOPN	H10	VCC	L4	I/O(A)	N20	I/O(E)	T14	N/C
C1	I/O(A)	E17	INREF(G)	H11	VDED	L5	I/O(A)	N21	I/O(E)	T15	I/O(D)
C2	I/O(A)	E18	I/O(G)	H12	GND	L6	I/O(A)	N22	I/O(E)	T16	GND
C3	VCCPLL(3)	E19	AD(25)	H13	VCC	L7	GND	P1	I/O(B)	T17	I/O(E)

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Table 41: QL5842 - 484 PBGA Pinout Table (Continued)

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
C4	PLLOUT(2)	E20	I/O(F)	H14	VCC	L8	GND	P2	I/O(B)	T18	I/O(E)
C5	I/O(A)	E21	I/O(F)	H15	GND	L9	GND	P3	I/O(B)	T19	I/O(E)
C6	I/O(H)	E22	I/O(F)	H16	AD(21)	L10	GND	P4	I/O(B)	T20	I/O(E)
C7	I/O(H)	F1	I/O(A)	H17	I/O(F)	L11	GND	P5	I/O(B)	T21	IOCTRL(E)
C8	I/O(H)	F2	INREF(A)	H18	I/O(F)	L12	GND	P6	VCCIO(B)	T22	I/O(E)
C9	IOCTRL(H)	F3	I/O(A)	H19	I/O(F)	L13	GND	P7	I/O(B)	U1	IOCTRL(B)
C10	I/O(H)	F4	I/O(A)	H20	I/O(F)	L14	VCC	P8	VCC	U2	I/O(B)
C11	AD(2)	F5	I/O(A)	H21	I/O(F)	L15	VCC	P9	GND	U3	IOCTRL(B)
C12	I/O(H)	F6	VCCIO(A)	H22	I/O(F)	L16	CLK(6)	P10	VCC	U4	I/O(B)
C13	AD(11)	F7	VCCIO(H)	J1	I/O(A)	L17	VCCIO(F)	P11	GND	U5	I/O(B)
C14	I/O(G)	F8	I/O(H)	J2	I/O(A)	L18	I/O(F)	P12	VCC	U6	I/O(C)
C15	PERRN	F9	VCCIO(H)	J3	I/O(A)	L19	(PCI)CLK	P13	VCC	U7	VCCIO(C)
C16	TRDYN	F10	AD(1)	J4	I/O(A)	L20	I/O(F)	P14	GND	U8	N/C
U9	VCCIO(C)	V8	I/O(C)	W7	N/C	Y6	I/O(C)	AA5	I/O(C)	AB4	I/O(B)
U10	I/O(C)	V9	N/C	W8	I/O(C)	Y7	I/O(C)	AA6	I/O(C)	AB5	I/O(B)
U11	VCCIO(C)	V10	I/O(C)	W9	I/O(C)	Y8	IOCTRL(C)	AA7	I/O(C)	AB6	I/O(C)
U12	VCCIO(D)	V11	I/O(C)	W10	I/O(C)	Y9	I/O(C)	AA8	INREF(C)	AB7	I/O(C)
U13	I/O(D)	V12	VDED2	W11	I/O(C)	Y10	I/O(C)	AA9	I/O(C)	AB8	IOCTRL(C)
U14	VCCIO(D)	V13	N/C	W12	I/O(D)	Y11	I/O(D)	AA10	I/O(C)	AB9	I/O(C)
U15	N/C	V14	I/O(D)	W13	I/O(D)	Y12	I/O(D)	AA11	I/O(C)	AB10	I/O(C)
U16	VCCIO(D)	V15	I/O(D)	W14	I/O(D)	Y13	I/O(D)	AA12	I/O(D)	AB11	I/O(C)
U17	VCCIO(E)	V16	INREF(D)	W15	I/O(D)	Y14	I/O(D)	AA13	I/O(D)	AB12	I/O(D)
U18	I/O(E)	V17	I/O(D)	W16	N/C	Y15	IOCTRL(D)	AA14	I/O(D)	AB13	I/O(D)
U19	I/O(E)	V18	I/O(E)	W17	I/O(D)	Y16	I/O(D)	AA15	I/O(D)	AB14	I/O(D)
U20	IOCTRL(E)	V19	I/O(E)	W18	I/O(E)	Y17	I/O(D)	AA16	I/O(D)	AB15	I/O(D)
U21	I/O(E)	V20	I/O(E)	W19	I/O(E)	Y18	I/O(E)	AA17	I/O(D)	AB16	IOCTRL(D)
U22	INREF(E)	V21	I/O(E)	W20	I/O(E)	Y19	PLLOUT(0)	AA18	I/O(D)	AB17	I/O(D)
V1	I/O(B)	V22	I/O(E)	W21	I/O(E)	Y20	PLLRST(1)	AA19	I/O(E)	AB18	I/O(D)
V2	I/O(B)	W1	I/O(B)	W22	I/O(E)	Y21	I/O(E)	AA20	GNDPLL(1)	AB19	I/O(E)
V3	I/O(B)	W2	I/O(B)	Y1	I/O(B)	Y22	I/O(E)	AA21	I/O(E)	AB20	GND
V4	I/O(B)	W3	I/O(B)	Y2	I/O(B)	AA1	TDO	AA22	I/O(E)	AB21	VCCPLL(1)
V5	I/O(B)	W4	I/O(B)	Y3	VCCPLL(2)	AA2	PLLOUT(1)	AB1	I/O(B)	AB22	I/O(E)
V6	I/O(C)	W5	I/O(B)	Y4	I/O(C)	AA3	GND	AB2	GNDPLL(2)		
V7	I/O(C)	W6	I/O(C)	Y5	I/O(C)	AA4	I/O(B)	AB3	PLLRST(2)		

VCCIO(F) and VCCIO(G) must be connected to VCCIO(PCI) (3.3 V).

Summary: 49 PCI pins, 262 user I/O, and 8 GCLK.

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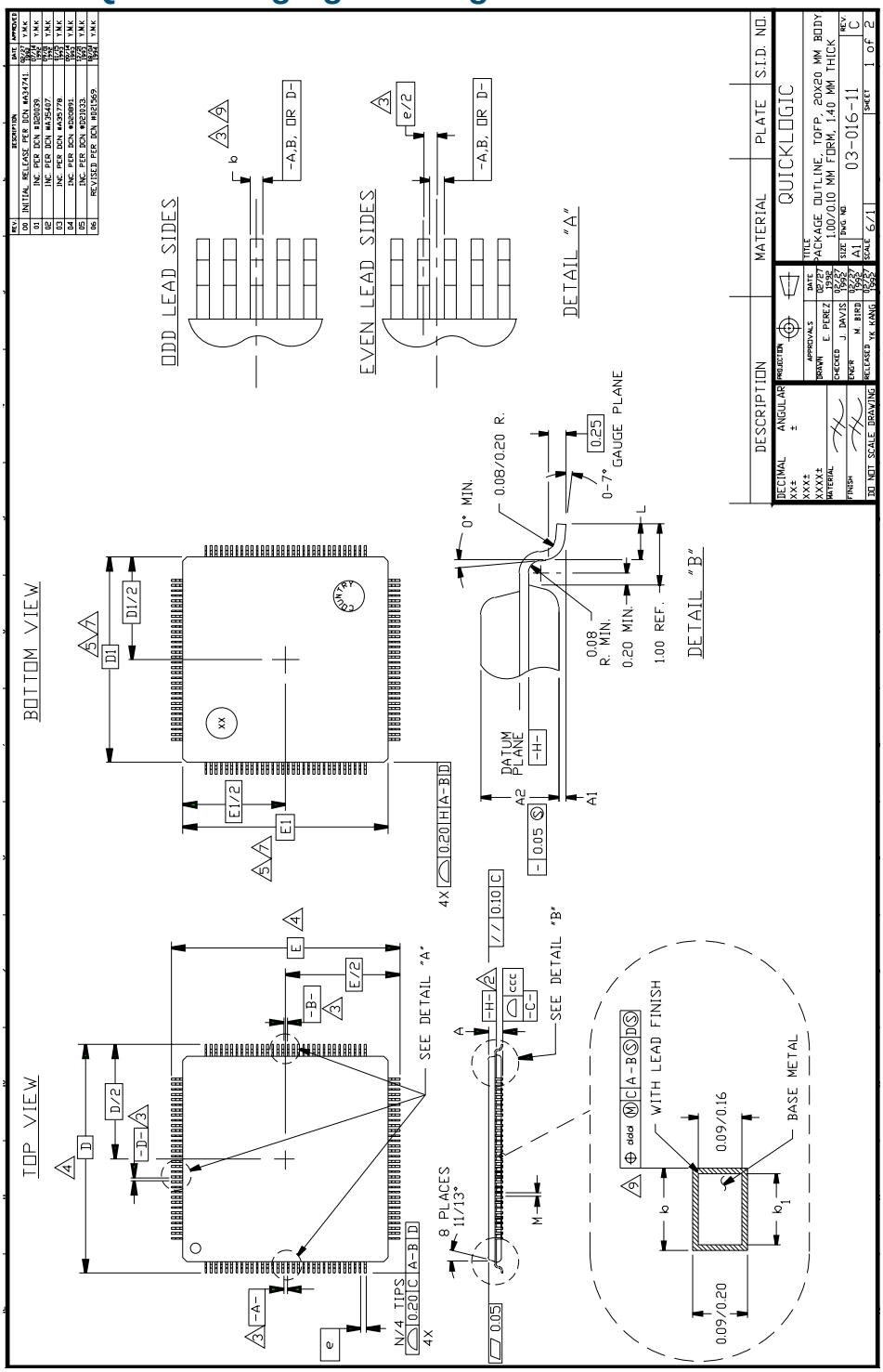
Package Mechanical Drawings

144 TQFP Packaging Drawing



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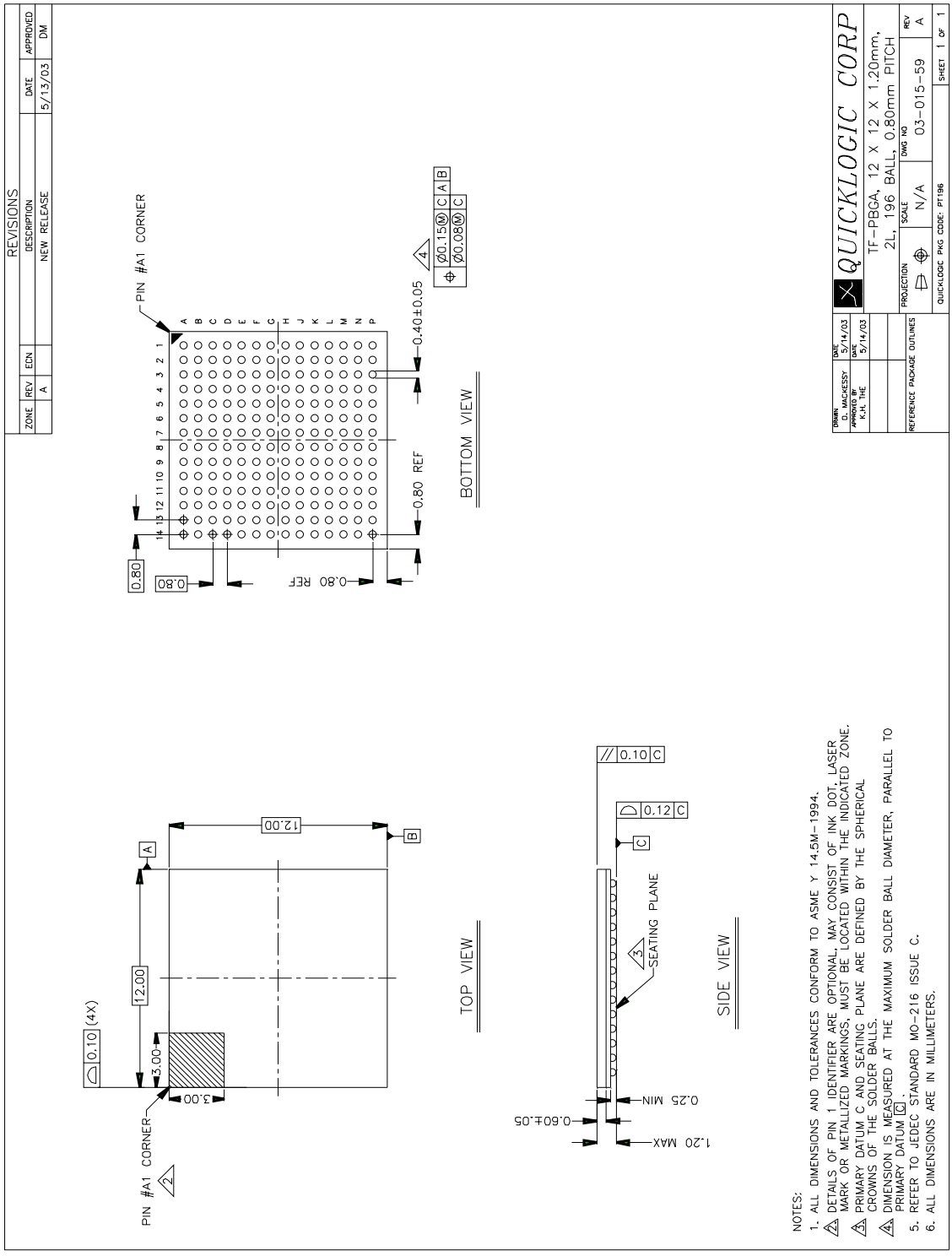
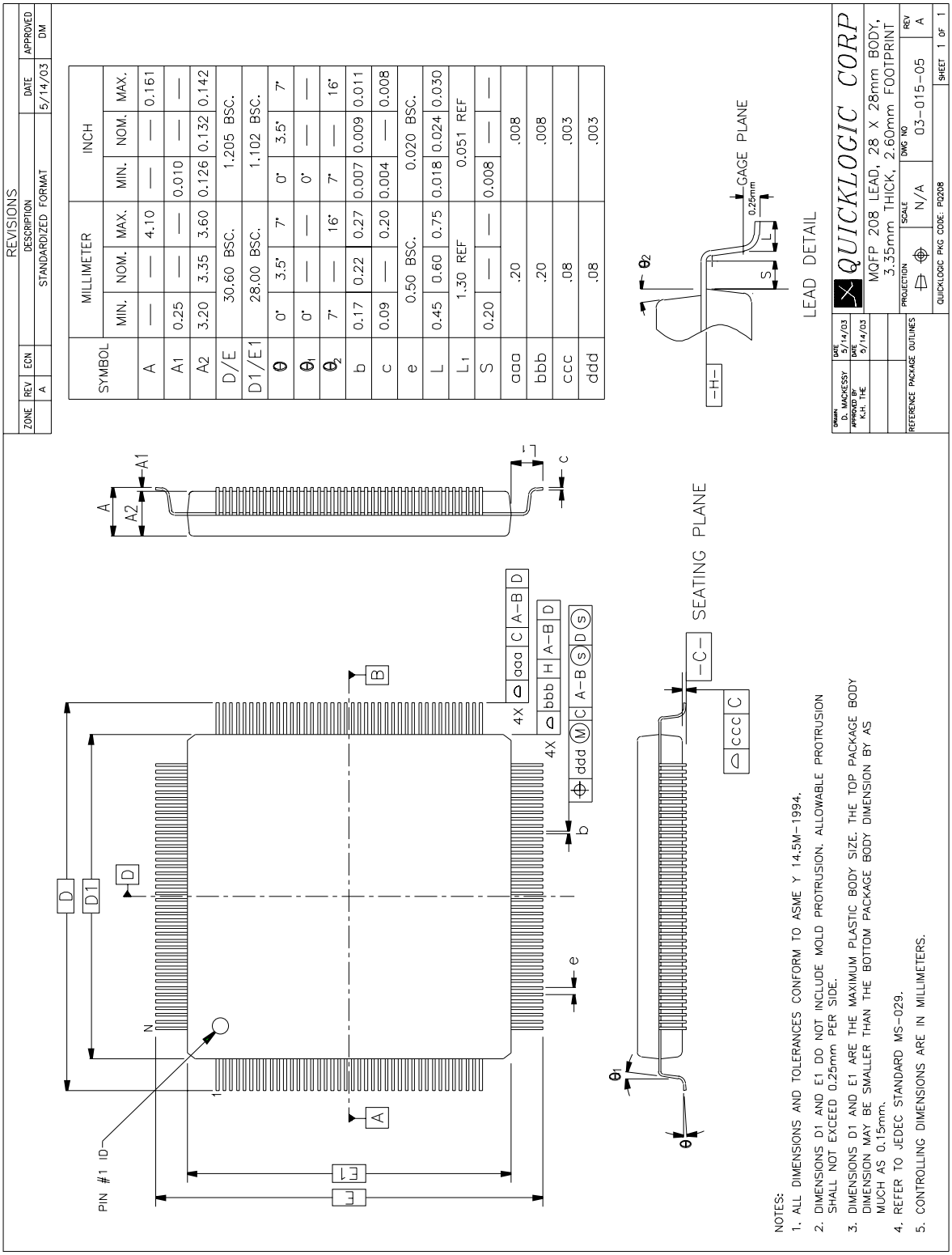
196 TFBGA Packaging Drawing



208 PQFP Packaging Drawing



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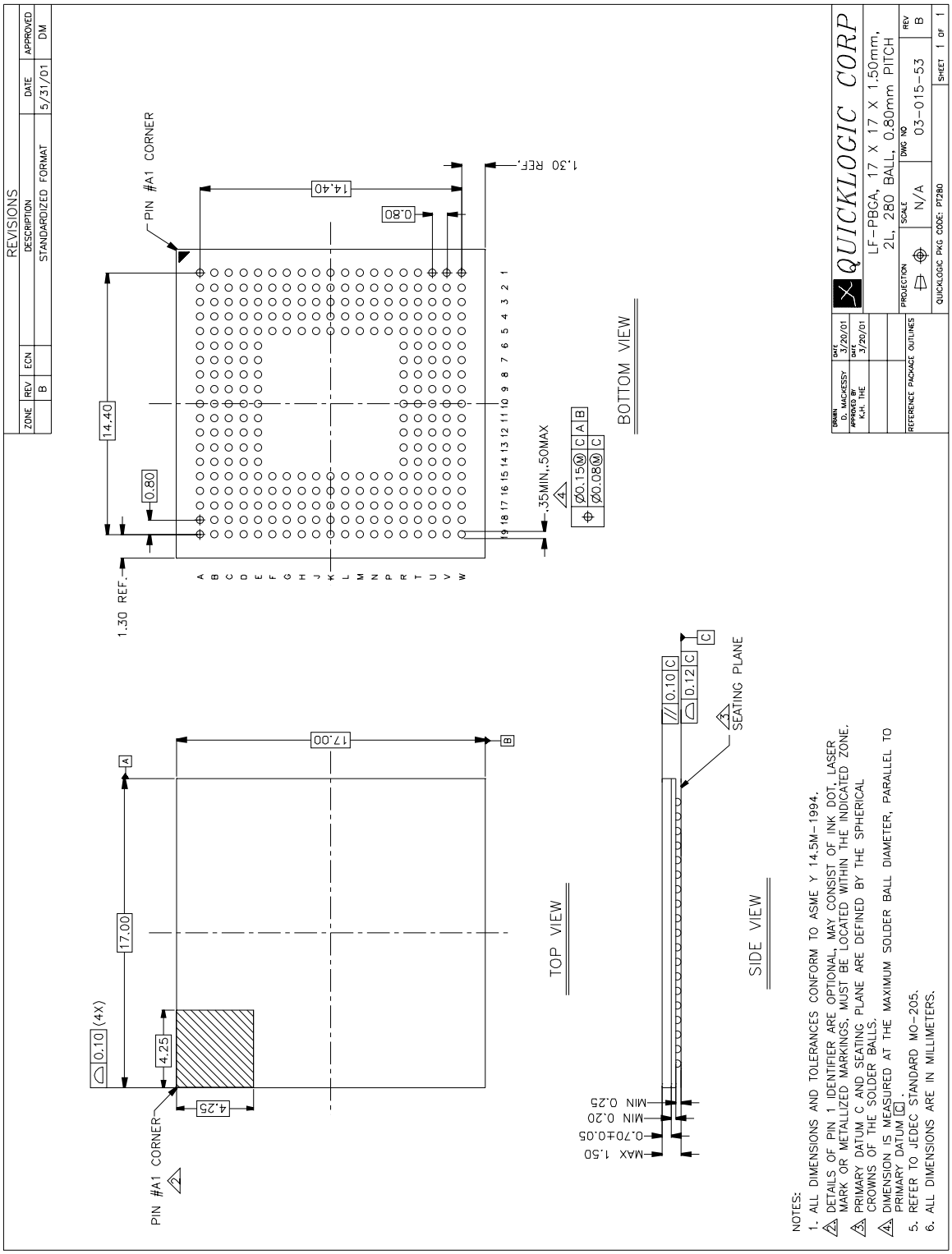
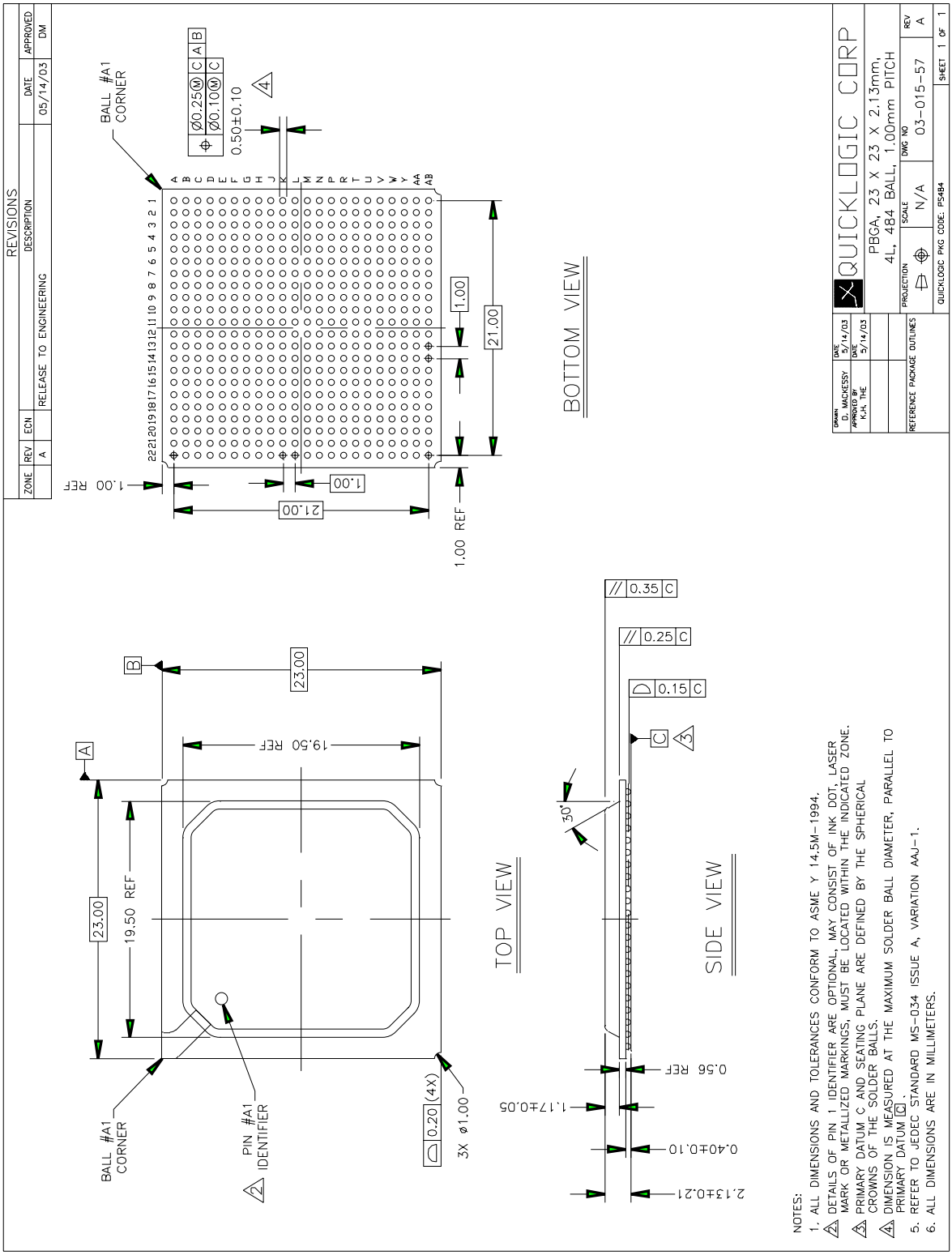
280 LFBGA Packaging Drawing



484 PBGA Packaging Drawing



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Packaging Information

The QL58x2 device family product packaging information is presented in **Table 42**.

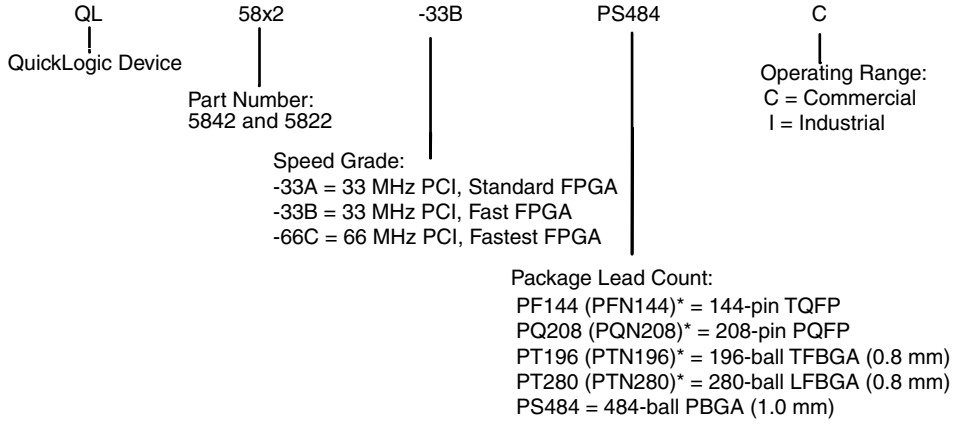
NOTE: Military temperature range plastic packages will be added as follow on products to the commercial and industrial products.

Table 42: Packaging Options

Device Information	Device			
	QL5822		QL5842	
	Pin	Pitch	Pin	Pitch
Package Definitions[a]	144 TQFP	0.50 mm	208 PQFP	0.50 mm
	196 TFBGA	0.80 mm	280 LFBGA	0.80 mm
	208 PQFP	0.50 mm	484 PBGA	1.00 mm
	280 LFBGA	0.80 mm	-	-

a. PQFP = Plastic Quad Flat Pack
TFBGA = Thin Fine Pitch Ball Grid Array
LFBGA = Low Profile Fine Pitch Ball Grid Array
TQFP = Thin Quad Flat Pack

Ordering Information



* Lead-free packaging is available, contact QuickLogic regarding availability (see Contact Information).

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Revision History

Revision	Date	Comments
A	October 2003	Bernhard Andretzky and Kathleen Murchek
B	November 2003	Bernhard Andretzky and Kathleen Murchek Updated Figure 1. Block Diagram
C	March 2004	Bernhard Andretzky and Kathleen Murchek Updated RAM information.
D	June 2004	Bernhard Andretzky and Kathleen Murchek Updated AC Characteristics tables values. Updated PLL descriptions.
E	July 2004	Bernhard Andretzky and Kathleen Murchek
F	August 2004	Bernhard Andretzky and Kathleen Murchek Updated pin tables.
G	November 2004	Bernhard Andretzky and Kathleen Murchek Updated pin tables.
H	March 2005	Mehul Kochar and Kathleen Murchek Added QL5822 - 280 device. Removed all QL5832 devices. Updated PLL information. Added lead-free packaging information. In the packaging information section, the pitch for the QL5822-196 TFBGA was corrected from 0.05 mm to 0.08 mm.

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