QL5064 QuickPCI Data Sheet

66 MHz/64-bit PCI Master/Target with Embedded Programmable Logic and Dual Port SRAM

Device Highlights

High Performance PCI Controller

- 64-bit/66 MHz Master/Target PCI Controller (automatically backwards compatible to 33 MHz or/and 32-bits)
- 75 MHz PCI Interface supported for embedded systems
- PCI Specification v2.2 compliance
- Programmable back-end interface with three 64-bit busses/100 MHz
- Provides full 533 MB/s PCI data transfer rates (600 MB/s at 75 MHz)

Advanced PCI Features

- DMA Chaining mode for queued DMA transactions
- Four-channel DMA mastering, plus a SPCI (Single PCI Access) mode
- Unlimited bursts supported in Master and Target mode
- Two Master Write FIFOs and two Master Read FIFOs, each 64-deep and 64 bits wide
- Target Read and Write FIFOs for pre-fetched reads and multipleposted writes
- Programmable interrupt controller
- I2O compliant under microprocessor control
- 16 Mailbox registers for message passing and semaphores
- Extended configuration space allowing Messaged Interrupts, power management, and future PCI enhancement support

Extremely Flexible and Configurable

- Supports processor-less systems, as well as 0 wait-state burst connections to all known 8/16/32/64 bit processors
- Includes non-volatile on-chip configuration data for total customization
- Independent PCI bus (66 MHz) and local bus (100 MHz) clocks
- All local interface, control, and glue-logic can be implemented on chip
- "PCI friendly" pinout simplifies board layout, supports 4-layer PCI boards

Advanced Master DMA Features

- Programmable DMA Channel Arbitration Scheme
- SPCI (Single PCI Access) mode may initiate any PCI Master command
- DMA controller configurable via PCI or back-end
- DMA Chaining mode allows a linked list of DMA transfers to occur without user intervention

High Performance PCI Target

- Write posting FIFO increases performance with queued transactions (up to 16 queued writes)
- Any BAR can be defined as pre-fetchable
- Six base address registers supported, configurable as memory or IO
- Unique "Target Blast Mode" enables high-performance and very low overhead streaming data to/from PCI

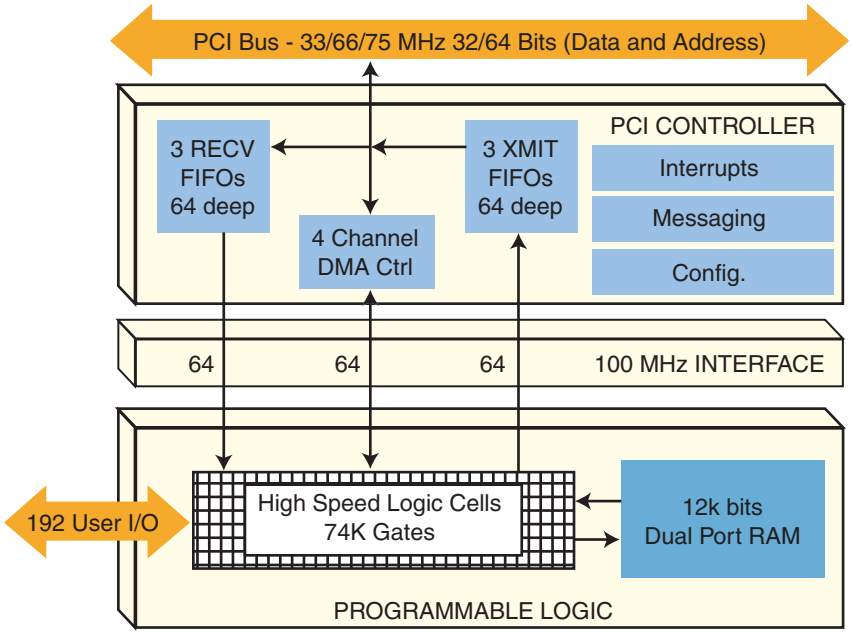
Expanded PCI Functionality

- Support for Configuration Space from 0x40 to 0x3FF
- PCI expanded capabilities support
- Expansion ROM supported with back-end memory
- Power management support
- Compact PCI hot-swap/hot-plug compliant
- Messaged Interrupts
- Configuration specified with anti-fuses on board, external EEPROM not needed

Programmable Logic

- 192 Programmable I/O pins in a 456 pin or 484 pin PBGA package
- 74K gates with 11 blocks (total of 12,672 bits) of dual-port RAM
- 250 MHz 16-bit counters, 275 MHz Datapaths, 160 MHz FIFOS
- All back-end interface and glue-logic can be implemented on chip

Figure 1: QL5064 Block Diagram



Architecture Overview

The QL5064 device in the QuickLogic QuickPCI ESP (Embedded Standard Products) family provides a complete and customizable PCI interface solution combined with 74,000 system gates of programmable logic. This device eliminates any need for the designer to worry about PCI bus compliance, yet allows for the maximum possible PCI bus bandwidth.

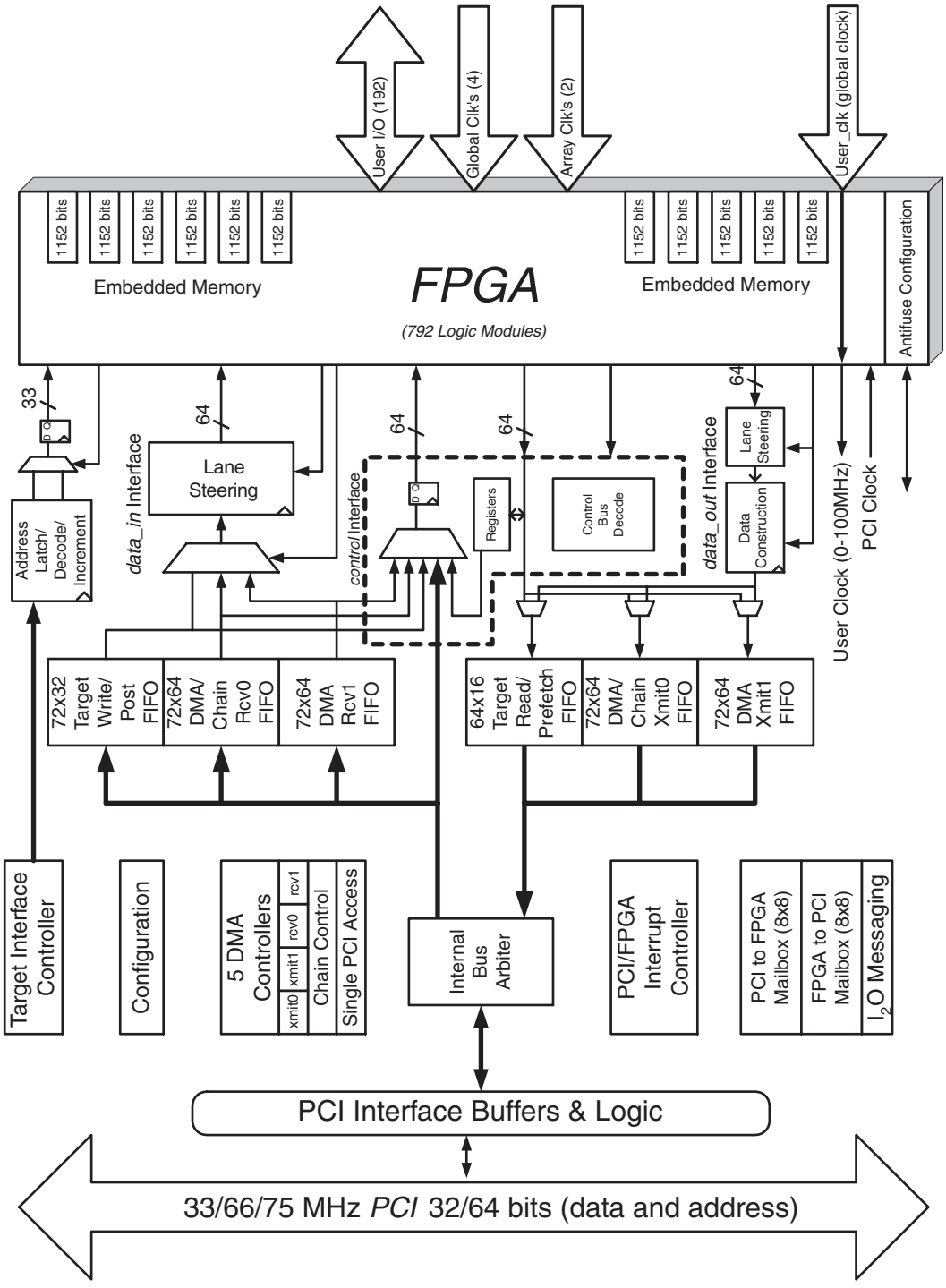
The programmable logic portion of the device is built from 792 QuickLogic Logic Cells, and 11 QuickLogic Dual-Port RAM Blocks. The configurable RAM blocks can each operate in 64x18, 128x9, 256x4, or 512x2 mode. These dual-port RAM blocks can be cascaded to achieve deeper or wider configurations. They can also be combined with logic cells to form FIFOs. See **RAM Module Features** on page 13 for more information.

The QL5064 device includes a complete pre-designed PCI Initiator/Target interface offering full burst mode transfers at 32 or 64 bits per clock cycle. At 66 MHz, this device offers support for 533 Mbytes/sec data transfer rates (66.6 MHz * 8 bytes per transfer). At the maximum speed of 75 MHz (exceeding the current maximum speed specification for PCI), the QL5064 device can achieve 600 Mbytes/sec data transfer rates. The PCI interface is configured via internal programmable configuration bits, so no external EEPROM or memory is needed.

The QL5064 device meets PCI 2.2 electrical and timing specifications and has been fully hardware-tested. The QL5064 device features 3.3-volt operation with multi-volt compatible I/Os. Thus it can easily operate in 3.3-volt only systems, as well as mixed 3.3 volt/5 volt system. It can be placed on a universal signaling PCI board.

A wide range of additional features complements the QL5064 device. The FPGA side of the device is 5 volt and 3.3-volt PCI-compliant and is capable of implementing FIFOs at 160 MHz, and counters at over 250 MHz. I/O pins provide individually controlled output enables, dedicated input/feedback registers, and full JTAG capability for boundary scan and test. In addition, the QL5064 device provides the benefits of non-volatility, high design security, immediate functionality on power-up, and a self-contained single chip solution.

Figure 2: QL5064 Device Block Diagram



Applications

The QL5064 device supports maximum PCI transfer rates, so many applications exist which are ideally suited to the device's high performance. High speed data communications, telecommunications, and computing systems are just a few of the broad range of applications areas that can benefit from the high speed PCI interface and programmable logic.

The PCI Interface can also act as a PCI Host Controller. This can be accomplished by glue-less interface to most popular 8/16/32/64-bit microprocessors.

Six FIFOs for Increased Performance

The PCI interface includes the following six FIFO buffers:

- Two 64x64 PCI Master Transmit Buffers
- Two 64x64 PCI Master Receive Buffers
- One 16x64 PCI Target Read/Pre-Fetch Buffer
- One 32x64 PCI Target Write/Post Buffer

All FIFO buffers are 72 bits wide (64 data bits + 8-bit byte enables). PCI Initiator-mode buffers are 64 deep and support sustained burst transfers. PCI Target mode buffers are provided for both Read and Write operations to the PCI Target, supporting pre-fetched reads with configurable registers.

All FIFOs can operate with independent read and write clocks, so that the programmable logic design can interface to the FIFOs at up to 100 MHz (a clock asynchronous to the 33/66 MHz PCI clock). All data synchronization is accomplished in the PCI core.

The transmit FIFOs have full flags and the receive FIFOs have empty flags. Both types of FIFOs have programmable status flags that may be used to determine if either of the transmit FIFOs are almost full or if either of the receive FIFOs are almost empty.

DMA Feature Overview

Each Master-mode FIFO has its own DMA controller to support maximum data throughput. Combining one Initiator-Mode Transmit FIFO with one Initiator-Mode Receive FIFO also supports DMA Chaining. This unique and flexible DMA chaining mode permits a 'linked-list' of transfers to be completed by the DMA controller without software or processor intervention.

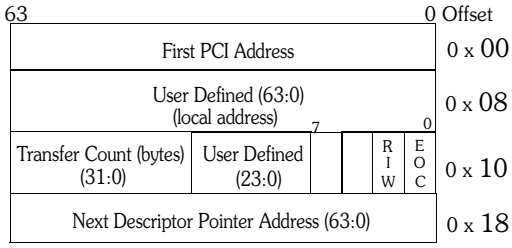
DMA Registers are accessible by the FPGA (back-end interface), as well as the PCI bus.

DMA Chaining descriptors are made of four 64-bit Quad-Words, or 32 bytes of data per descriptor. Each descriptor defines a DMA transaction (memory start location, size, read/write) as well as 88 bits of user-defined information (such as a descriptor identifier, or back-end address).

DMA Chaining is a powerful DMA feature, allowing the QL5064 device to drive continuous pre-defined DMA transactions with no processor or software interaction.

Single PCI Access (SPCI) reads and writes are supported for single quad-word transfers that do not require FIFOs. SPCI supports IO reads and writes, configuration reads and writes, special cycles, interrupt acknowledge cycles, as well as standard memory read/write transactions.

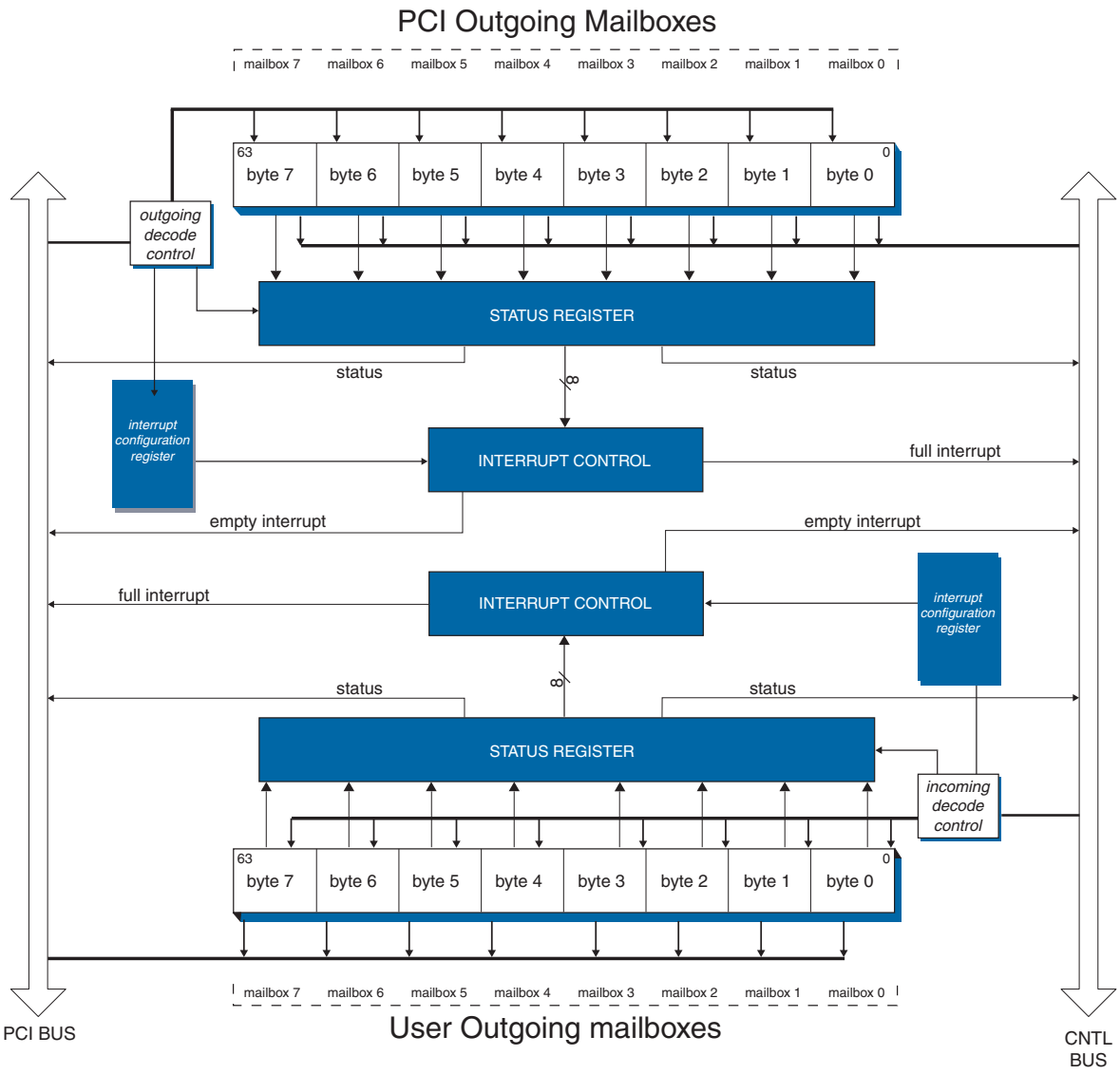
Figure 3: DMA Chaining Descriptor



Mailbox Registers and I_2O

The PCI interface contains 16 bytes of mailbox registers to support message/semaphore passing between the programmable logic design and the PCI bus. These mailbox registers are memory mapped to a dedicated register bank within the first 256 bytes of BAR 0. Eight bytes are provided for the FPGA to PCI direction, and eight bytes are also provided for the PCI to FPGA direction. Status flags and interrupts are available for each direction as well. **Figure 4** shows the mailbox structure within the QL5064 device. Hardware controlled queues allow full I_2O messaging support with a processor and local I_2O drivers.

Figure 4: Mailbox Structure



Internal Bus Structure

The internal interface between the PCI Controller and the FPGA logic cells is both simple and flexible. The interface is configurable, based on the needs of the FPGA design. Configuration is accomplished at the time of programming the FPGA.

The FPGA/PCI interface supports very high bandwidth data transfers via three 64-bit busses. The interface is fully synchronous, and supports a separate clock from the PCI clock. The Interface clock can run at up to 100 MHz.

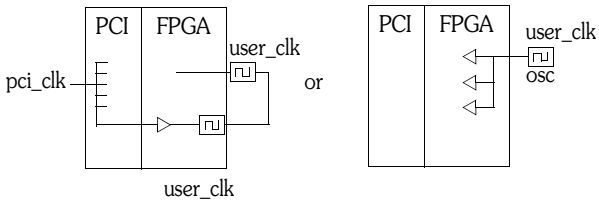
The interface has three busses: DataIN, DataOUT, and Control_DATA. The DataIN bus moves the data from the PCI bus to the back-end. The DataOUT bus moves data from the back-end to the PCI bus. The Control_DATA bus moves the data from the PCI bus to the back-end and from the back-end to the PCI bus. It also accesses the internal control registers. All three busses can operate simultaneously at zero wait states.

Clocking

All bus accesses to the QL5064 from the FPGA (back-end) interface are synchronous to the back-end user clock - called user_clk. The user_clk is supplied on a dedicated external pin. The PCI clock may be routed out to a pin, and then back into the device to be used as the user_clk if desired. The user_clk signal may be asynchronous to the pci_clk signal, and may run at up to 100 MHz with no PLL requirements.

All busses on the back-end of the QL5064 device can sustain data movement on every cycle of user_clk.

Figure 5: FPGA to PCI Synchronization

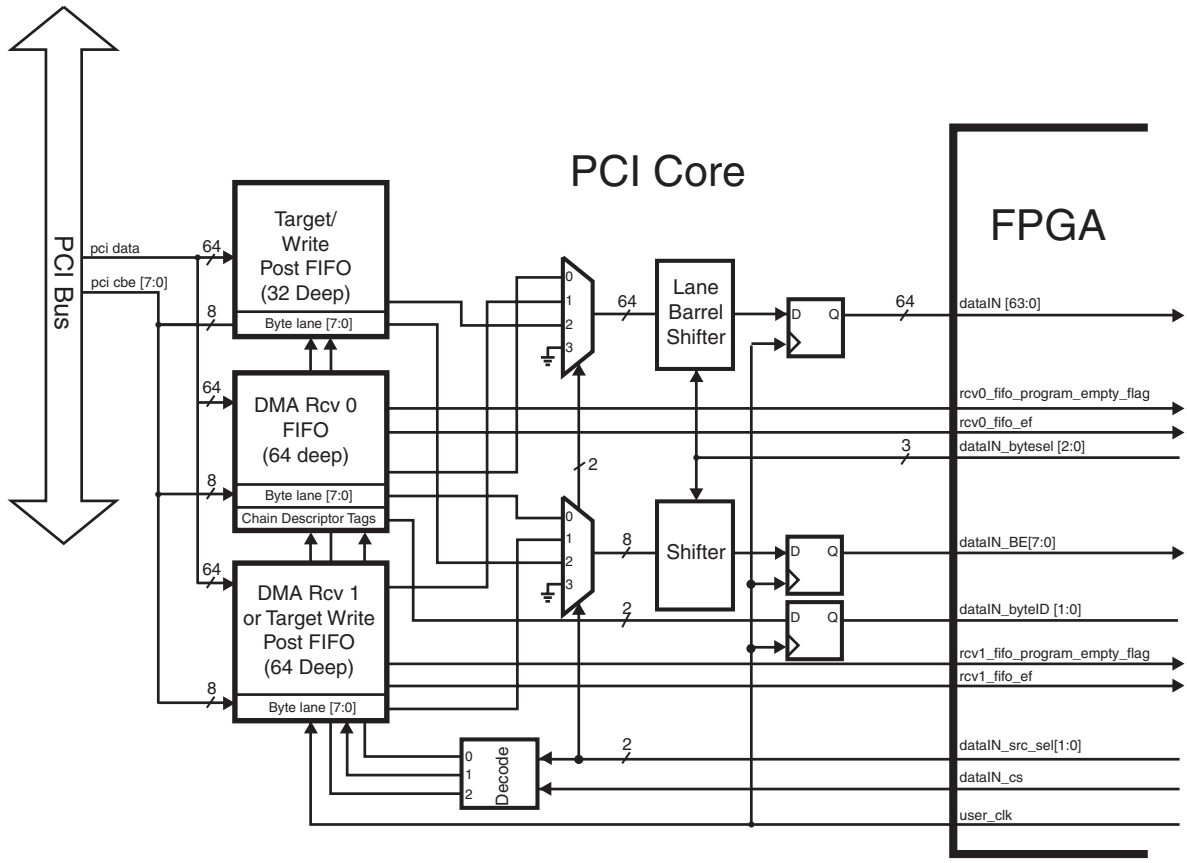


DataIN Bus Description

The DataIN bus transfers data from the PCI bus to the back-end interface. This data can come from three different data paths: either one of the two DMA receive FIFOs, or the Target Write/Post FIFO. For proper data management, empty and almost empty flags from the two DMA receive FIFOs are accessible to the back-end design. The almost empty flags are configured through the Control_DATA bus interface or the PCI bus. Interface to the Target Write/Post FIFO is accomplished through the Target interface signals. A block diagram of the DataIN and Target control connections is shown in **Figure 6**.

Data is transferred to the DataIN bus in the same byte lane in which is was transferred over the PCI bus. To assist with re-aligning or compacting data in the back-end interface, a byte-lane barrel shifter provides the means to manipulate byte lane positioning. This is accomplished with the byte_select[2:0] input. See the DataIN Bus section of the internal signal descriptions for more information.

Figure 6: DataIN Bus Description



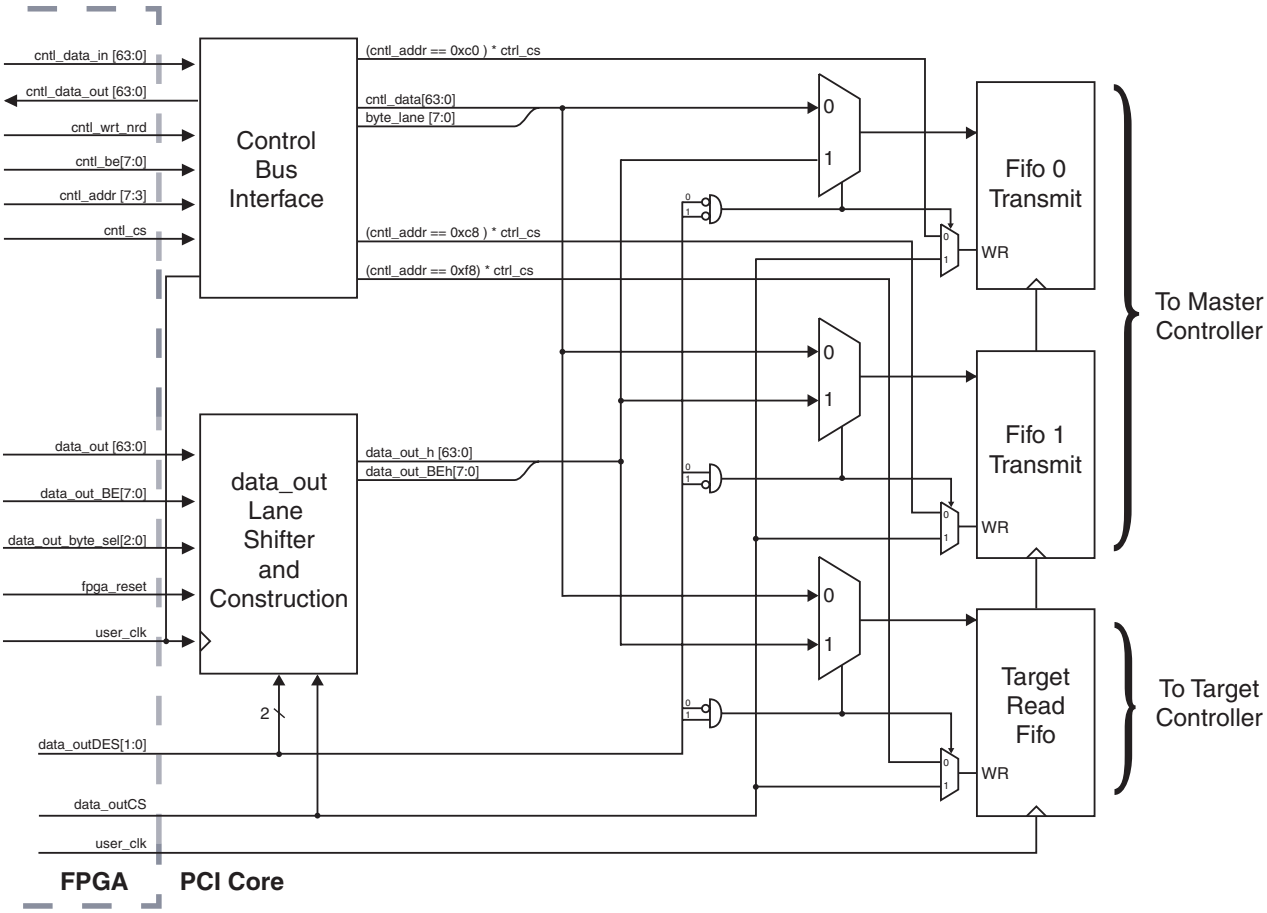
DataOUT Bus Description

The DataOUT bus is used to transfer data from the back-end interface to the PCI bus. This bus is connected to three destinations within the QL5064 device: either one of the two DMA transmit FIFOs, or the Target Read/Pre-Fetch FIFO. For proper data management and high data throughput, full and almost full flags are available for each of the two DMA transmit FIFOs. The almost full flags are fully configurable via the Control_DATA bus interface or the PCI bus. Interface to the Target Read/Pre-Fetch FIFO is accomplished through the Target interface signals. A block diagram of the DataOUT connections is shown in **Figure 7**.

The data_outDES[1:0] signals select a particular FIFO to be connected to the DataOUT bus. A block diagram of the DataOUT bus and its connections is shown in **Figure 7**.

Data written to the DMA transmit FIFOs or the Target Read/Pre-fetch FIFO must be set up in the same byte lanes in which the data will be transferred in the PCI bus. To aid with aligning, re-aligning, or compacting data that is to be written to the FIFOs via the DataOUT bus, a byte-lane barrel shifter is present, controlled by the data_out_shift[2:0] signals. See the DataOUT bus section of **Table 2** for more information.

Figure 7: DataOUT and Control Bus Description



Control_DATA Bus Description

The Control_DATA bus is the heart of the control circuitry for the PCI interface. The intent of this bus is to provide access to all of the control structures necessary for a microprocessor interfaced to the QL5064 device to be able to marshal all PCI operations. The Control_DATA bus, like the DataIN and DataOUT buses, is synchronous to user_clk, and can be written or read on every clock. This is a bi-directional bus that offers read and write access at 64-bits. In addition to all control structures, this bus is designed to access all of the six FIFOs.

PCI Master Arbitration

Five possible masters could be driving PCI master transactions on the PCI bus, and as a result, a flexible arbitration controller has been included in the QL5064 device. The five sources for PCI master transactions include: Transmit FIFO 0, Transmit FIFO 1, Receive FIFO 0, Receive FIFO 1, and SPCI (Single PCI Access). (SPCI is a means for the back-end design to initiate single quad-word transfers directly on the PCI bus for master transactions, bypassing the DMA FIFOs). SPCI Mastering is controlled through the Control_DATA bus.

Three arbitration modes have been defined for the QL5064 device. These modes are round robin, prioritized, and customized. In all modes, the SPCI Mastering always has highest priority. The arbitration scheme is selected by setting the proper values in the Arbitration Mode bits of configuration registers (offset 0xD0, bits 49:48). The selection is: 00b - round robin, 01b - prioritized, 10b - customized, 11b - reserved.

Round robin arbitration simply cycles through the four Master FIFOs in the following order: Transmit 0 (T0), Transmit 1 (T1), Receive 0 (R0), Receive 1 (R1). Prioritized mode uses values assigned to DMA_arbitration_priority bits in the configuration memory (offset 0xD0). Masters set to equal priority are arbitrated (high to low): T0, T1, R0, R1.

Customized arbitration mode uses two buses and back-end logic. The fpga_bus_req[3:0] signals (1 bit per FIFO) indicate to the programmable logic design which master is requesting the bus. The fpga_bus_req bits are assigned: [0]-R1, [1]-R0, [2]-T1, [3]-T0. The back-end design should set fpga_arb_sel[1:0] according to which master should be granted the bus. The fpga_arb_sel bus uses the enumeration: 00-R1, 01-R0, 10-T1, 11-T0.

Control Registers

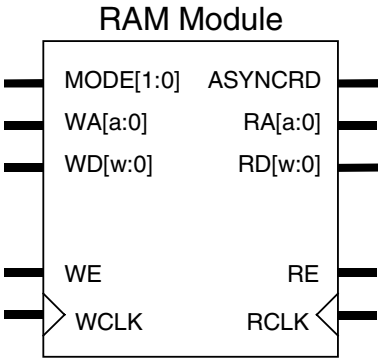
DMA Control and QL5064 registers can be accessed from the PCI bus or the back-end Control_DATA bus. On the PCI side, these registers are accessed through BAR 0, with offsets 0x00 to 0xFF (below 0x100). The breakdown of this memory space can be seen in **Table 1**.

Table 1: User Memory Map

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Master Write Address 0[63:0] (r/w)	00
Master Write Count Status0[31:0] (r only) | Master Write Transfer Count0[31:0] (r/w)	08
Master Write Address 1[63:0] (r/w)	10
Master Write Count Status1[31:0] (r only) | Master Write Transfer Count1[31:0] (r/w)	18
00 | strt | 32 bit | cmd[3:0] | byte lanes[7:0] | Receive FIFO 1 Byte Lane[7:0] | Bus Request: XMT 0, XMT 1, RCV 0, RCV 1, XMT 0, XMT 1 | Pipeline Not Empty | tag0 [1:0] | Receive FIFO 0 Byte Lane[7:0] | XM, XM, XM, XM, R2, R2, R2, R2 | Chip Revision ID [7:0] (r only) | User ID [7:0] (r only) antifuse	20
0000 | ep16 | ep8 | wrt | wwt | BAR Enable (r only): rom, 5, 4, 3, 2, 1, 0, BAR5, BAR4, BAR3, BAR2, BAR1, BAR0 | Target BAR Configuration (r only) | Target FIFO Threshold MSB's[3:0] | Target FIFO Control -- Emptyness Threshold: BAR5, BAR4, BAR3, BAR2, BAR1, BAR0 | 0 | Target Prefetch Cntl: pc, BAR[5:0] | 0 | Target Burst Request: pc, BAR[5:0]	28
I_2O Interrupt Mask Bit [3] → | I_2O Interrupt Service Request Bit [3] →	30
Reserved	38
I_2O Outbound Queue Pointer | I_2O Inbound Queue Pointer	40
Master Read Address 0[63:0] (r/w) / Chain Descriptor Start Address [63:0] (r/w)	48
Master Read Count Status0[31:0] (r only) | Master Read Transfer Count0[31:0] (r/w)	50
Master Read Address 1[63:0] (r/w)	58
Master Read Count Status1[31:0] (r only) | Master Read Transfer Count1[31:0] (r/w)	60
00 | XMIT FIFO 1 Almost Full[5:0] (r/w) | 00 | XMIT FIFO 0 Almost Full[5:0] (r/w) | 00 | XMIT FIFO 1 Almost Empty[5:0] (r/w) | 00 | XMIT FIFO 0 Almost Empty[5:0] (r/w) | 00 | Receive FIFO1 Almost Full[5:0] (r/w) | 00 | Receive FIFO0 Almost Full[5:0] (r/w) | 00 | Receive FIFO1 Almost Empty[5:0] (r/w) | 00 | Receive FIFO0 Almost Empty[5:0] (r/w)	68
User Incoming Mail 7 | User Incoming Mail 6 | User Incoming Mail 5 | User Incoming Mail 4 | User Incoming Mail 3 | User Incoming Mail 2 | User Incoming Mail 1 | User Incoming Mail 0	70
User Outgoing Mail 7 | User Outgoing Mail 6 | User Outgoing Mail 5 | User Outgoing Mail 4 | User Outgoing Mail 3 | User Outgoing Mail 2 | User Outgoing Mail 1 | User Outgoing Mail 0	78
0000_0000 | 0000_0000 | 0000_0000 | 0000_0000 | 0000 | I_2O Interrupt: oflf, ople, iplf, ifle | is | SP | DMA Interrupt: CE, chn, rcv1, rcv0, xmt1, xmt0 | User Outgoing MB Empty [7:0] | User Incoming MB Full [7:0]	80
0000_0000 | 0000_0000 | PCI Incoming MB Empty Interrupt Mask[7:0] | PCI Outgoing MB Empty Interrupt Mask[7:0] | 0000 | I_2O Int Mask: oflf, ople, iplf, ifle | IM | SP | Ma | DMA Interrupt Mask: CE, chn, rcv1, rcv0, xmt1, xmt0 | User Outgoing MB Empty Interrupt Mask[7:0] | User Incoming MB Full Interrupt Mask[7:0]	88
0000 | PED | MRT | MA | RTA | 00 | Error: SPCI, Chn, rcv1, rcv0, xmt1, xmt0 | 0 | TUR W | TAV | TUR | TUM | User region [2:0] | user_be_req[7:0] | 0000 | I_2O Status: oflf, ople, iplf, ifle | BI | 0 | Chain Ptr Fetch End | DMA Start/Done#: chn, rcv1, rcv0, xmt1, xmt0 | User Outgoing MB Status [7:0] | User Incoming MB Status [7:0]	90
Single PCI Access Address Register[63:0] (r/w)	98
Single PCI Access Data Register[63:0] (r/w)	a0
Reserved	a8
Receive FIFO0[63:0] (r only)	b0
Receive FIFO1[63:0] (r only)	b8
Transmit FIFO0[63:0] (w only)	c0
Transmit FIFO1[63:0] (w only)	c8
0000_0000 | 0000_00 | Arb Mode [1:0] | DMA Arbitration Priority: rcv1[1:0], rcv0[1:0], xmt1[1:0], xmt0[1:0] | 0000 | DMA 32/64#: rcv1, rcv0, xmt1, xmt0 | 0000 | DMA SPC: rcv1, rcv0, xmt1, xmt0 | 0 | FIFO Flush: xmt1, xmt0 | DMA Cancel: Chn, rcv1, rcv0, xmt1, xmt0 | 000 | ib | ob | BIST Code[3:0] | 0 | BE En [1:0] | Max Retry [1:0] | FIFO Thresh TO[1:0] | lat en	d0
Reserved	d8
Reserved	e0
Reserved	e8
Target Control Address[63:0] (r only) | 000	f0
Target Control Data[63:0] (r/w)	f8
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	

RAM Module Features

Figure 8: RAM Module



Mode:	64x18	128x9	256x4	512x2
Address Busses [a:0]	[5:0]	[6:0]	[7:0]	[8:0]
Data Busses [w:0]	[17:0]	[8:0]	[3:0]	[1:0]

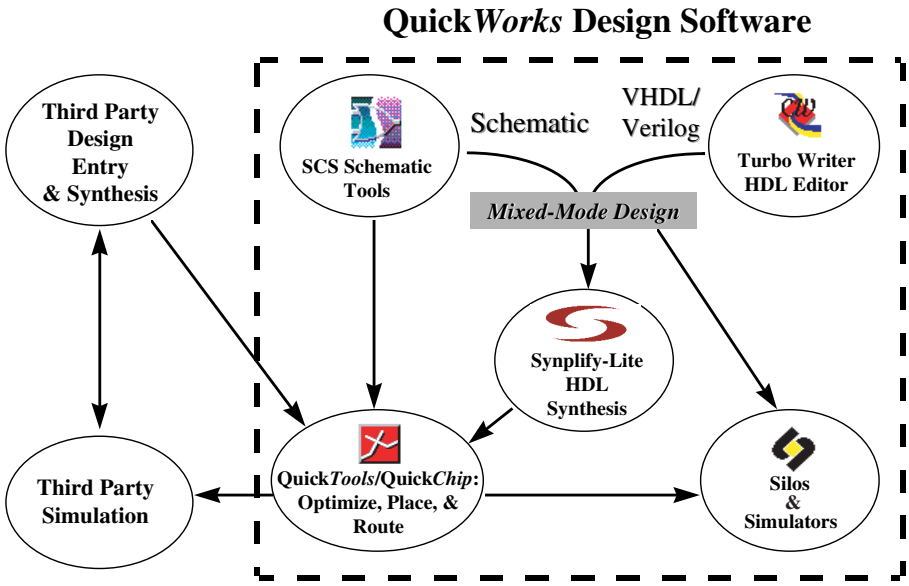
The RAM modules are "dual-ported," with independent READ and WRITE ports and separate READ and WRITE clocks. The READ ports support asynchronous and synchronous operation, while the WRITE ports support synchronous operation. Each port has 18 data lines and 9 address lines, allowing word lengths of up to 18 bits and address spaces of up to 512 words. Depending on the mode selected, however, some higher order data or address lines may not be used.

The Write Enable (WE) line acts as a clock enable for synchronous write operation. The Read Enable (RE) acts as a clock enable for synchronous READ operation (ASYNCRD input low), or as a flow-through enable for asynchronous READ operation (ASYNCRD input high).

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules. This approach allows up to 512 words deep configurations as large as 22 bits wide in the QL5064 device.

A similar technique can be used to create depths greater than 512 words. In this case address signals higher than the eighth bit are encoded onto the write enable (WE) input for WRITE operations. The READ data outputs are multiplexed together using encoded higher READ address bits for the multiplexer SELECT signals.

Figure 9: QuickWorks Tool Suite



JTAG Support

JTAG pins support IEEE standard 1149.1a to provide boundary scan capability for QL5064 devices. Six pins are dedicated to JTAG and programming functions on each QL5064 device, and are unavailable for general design input and output signals. These pins are: TDI, TDO, TCK, TMS, and TRSTB are JTAG. The sixth pin, STM, is used only for programming.

Development Tool Support

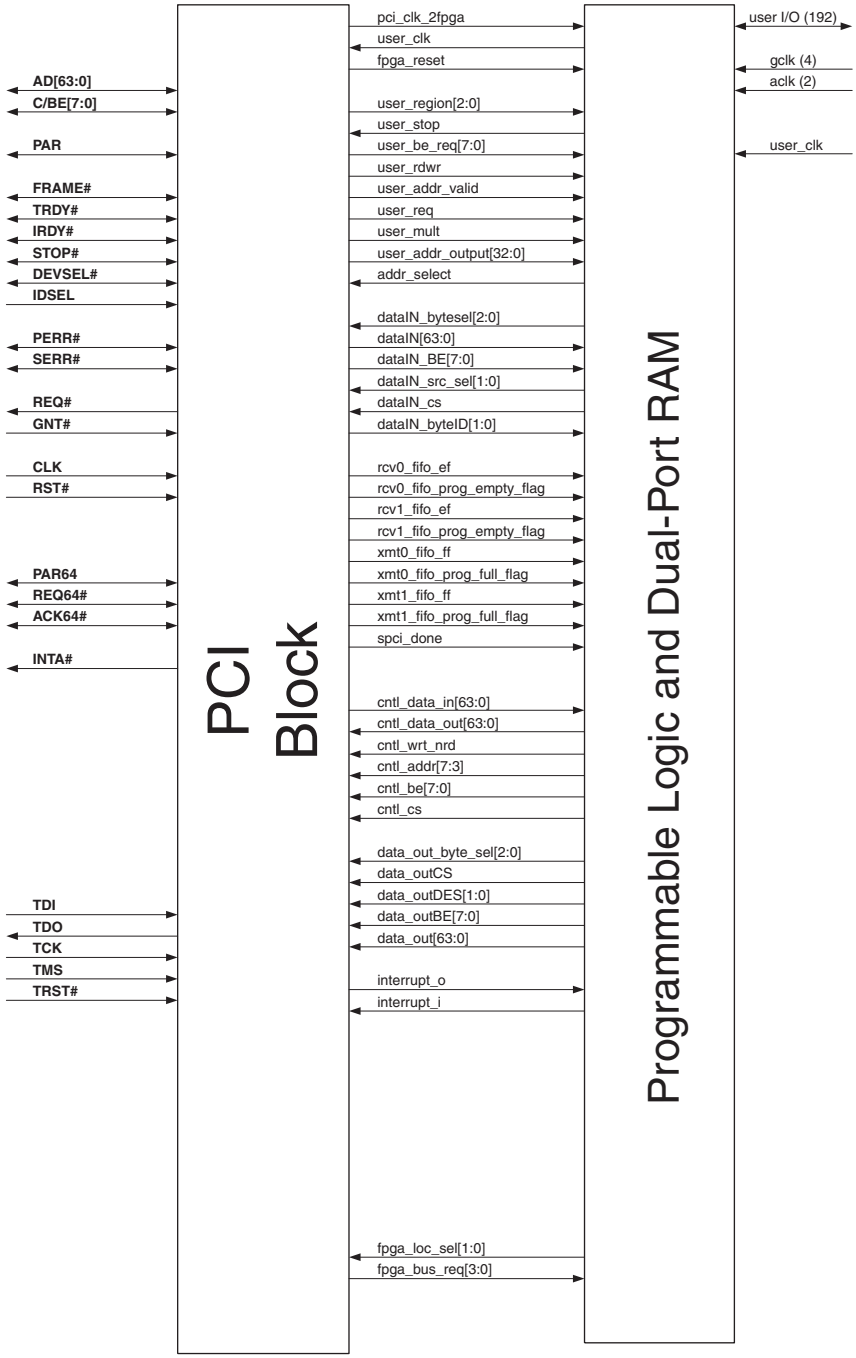
Software support for the QL5064 device is available through the QuickWorks development package. This turnkey PC-based QuickWorks package, shown in **Figure 9**, provides a complete ESP software solution with design entry, logic synthesis, place and route, and simulation. QuickWorks includes VHDL, Verilog, schematic, and mixed-mode entry with fast and efficient logic synthesis provided by the integrated Synplicity Synplify Lite tool, specially tuned to take advantage of the QL5064 architecture. QuickWorks also provides functional and timing simulation for guaranteed timing and source-level debugging.

The UNIX-based QuickTools and PC-based QuickWorks-Lite packages are a subset of QuickWorks and provide a solution for designers who use schematic-only design flow third-party tools for design entry, synthesis, or simulation. QuickTools and QuickWorks-Lite read EDIF netlists and provide support for all QuickLogic devices. QuickTools and QuickWorks-Lite also support a wide range of third-party modeling and simulation tools. In addition, the PC-based package combines all the features of QuickWorks-Lite with the SCS schematic capture environment, providing a low-cost design entry and compilation solution.

PCI to Programmable Logic Interface

The QL5064 device is designed to be highly customizable. **Figure 10** illustrates the interface signals present between the configurable PCI core, and the programmable logic region of the QL5064 device. Detailed descriptions of each of these interface signals follow in the next section.

Figure 10: PCI to Programmable Logic Interface Block Diagram



PCI Back-End Interface Signals

The PCI back-end internal signals can interface directly to pins or to internal logic cells or RAM blocks in the programmable logic region of the device. These signals are used to customize the device so that it can connect to other devices on the board directly, without any glue-logic required.

Table 2: PCI Back-End Interface Signals

Symbol	I/O[a]	Description
Clocks		
pci_clk_2fpga	I	Buffered version of the PCI clock. For use in the FPGA.
user_clk	O	FPGA supplied clock used for all interface to the embedded PCI core. This signal is required and all communication between the embedded PCI core and the FPGA is synchronous to this clock with the exception of the DMA arbitrary signals.
fpga_reset	I	Active High. Global reset signal from the PCI core. Active High. This signal should be used as the global reset for the FPGA and all other supporting circuitry.
Target Interface		
user_region [2:0]	I	When target_addr_valid is active, these signals indicate which of the following regions are being accessed. 3'b000 BAR0 3'b001 BAR1 3'b010 BAR2 3'b011 BAR3 3'b100 BAR4 3'b101 BAR5 3'b110 Expansion ROM 3'b111 Configuration Space 0x40-0xff
user_stop	O	Active High. Stops prefetch after the current cycle.
user_be_req [7:0]	I	Active High. Byte lanes requested by PCI for all target accesses.
user_rdwr	I	When target_addr_valid is active, a logic '1' indicates that the requested transaction is a read. When '0' the present transaction is a write.
user_addr_valid	I	Active High. Indicates that PCI is requesting a sequentially continuing target access.
user_req	I	Active High. When active, PCI is requesting at least one piece of data to be transferred. Deasserted after an advance generated by a read or write from the target FIFOs or after 'target_user_stop' is asserted.
user_mult	I	Active High. PCI is requesting at least 2+ pieces of data to be transferred.
user_addr_output [32:0]	I	The current address of the PCI target transaction. Incremented automatically by a quad word when a 64-bit piece of target data is written or read.
addr_select	O	Selects which half of the 64-bit PCI address for a target transaction is placed on the user_addr [32:0] bus. 0 - [35:3] 1 - 00000. [63:36]

Table 2: PCI Back-End Interface Signals (Continued)

Symbol	I/O[a]	Description
DataIN Bus - (PCI - FPGA)		
dataIN [63:0]	I	Active High. A 64-bit bus connecting to the FIFOs. Used by the FPGA to obtain data being transferred from the PCI bus to the FPGA.
dataIN_src_sel[1:0]	O	Active High. Data source select signals determines which FIFO is connected to the dataIN bus: 00 Receive FIFO0 01 Receive FIFO1 10 Target Write post FIFO 11 Not defined (returns 0)
dataIN_cs	O	Active High. Chip select for read operations on the dataIN bus. When active, advances the pointer for the FIFO selected by dataIN_src_sel[1:0]
dataIN_BE[7:0]	I	Active High. Indicates which byte lane is active for the current transfer occurring on dataIN[63:0]. dataIN_BE[7] dataIN[63:56] dataIN_BE[6] dataIN[55:48] dataIN_BE[5] dataIN[47:40] dataIN_BE[4] dataIN[39:32] dataIN_BE[3] dataIN[31:24] dataIN_BE[2] dataIN[23:16] dataIN_BE[1] dataIN[15:08] dataIN_BE[0] dataIN[07:00]
dataIN_bytesel[2:0]	I	dataIN_BE[7:0] are shifted along with the data. Sets the number of bytes to barrel shift the 64-bit dataIN bus and the dataIN_BE bus.
dataIN_byteID[1:0]	I	Active High. Tag bits for the DMA chain descriptor pointer. When active, indicates that chain descriptor information is available at the output of Receive FIFO0. dataIN_byteID[1:0] 00 Normal data 01 Descriptor dword 0 (PCI starting address) 10 Descriptor dword 1 (user defined) 11 Descriptor dword 2 (transfer count, et al.)
FIFO Status Signals		
rcv0_fifo_ef	I	Active High. Receive FIFO0 is empty.
rcv0_fifo_prog_empty_flag	I	Active High. Receive FIFO0 contains a number of entries less than or equal to the threshold set in register 0x68, bits 37:32.
rcv1_fifo_ef	I	Active High. Receive FIFO1 is empty.
rcv1_fifo_prog_empty_flag	I	Active High. Receive FIFO1 contains a number of entries less than or equal to the threshold set in register 0x68, bits 45:40.
xmt0_fifo_ff	I	Active High. Transmit FIFO0 is full.
xmt0_fifo_prog_full_flag	I	Active High. Transmit FIFO0 contains a number of entries greater than or equal to the threshold set in register 0x68, bits 53:48.
xmt1_fifo_ff	I	Active High. Transmit FIFO1 is full.

Table 2: PCI Back-End Interface Signals (Continued)

Symbol	I/O[a]	Description
xmt1_fifo_prog_full_flag	I	Active High. Transmit FIFO1 contains a number of entries greater than or equal to the threshold set in register 0x68, bits 61:56.
Miscellaneous Interface Signals		
SPCI_done	I	Active High. Single PCI Access done.
Control Bus Interface Signals		
cntl_data_in[63:0]	I	Active High. A 64-bit bus used to read to the various memory mapped registers of the QL5064.
cntl_wrt_nrd	O	Control bus write/not read. When '1' current access to the control bus is a write. When '0' current access to the control bus is a read.
cntl_addr[7:3]	O	Active High. Control bus address bits 7:3. Selects which of the 64-bit registers the control bus is accessing.
cntl_be[7:0]	O	cntl_be[7] cntl_data[63:56] cntl_be[6] cntl_data[55:48] cntl_be[5] cntl_data[47:40] cntl_be[4] cntl_data[39:32] cntl_be[3] cntl_data[31:24] cntl_be[2] cntl_data[23:16] cntl_be[1] cntl_data[15:08] cntl_be[0] cntl_data[07:00]
cntl_data_out[63:0]	O	Active High. A 64-bit bus used to write to the various QL5064 memory mapped registers.
cntl_cs	O	Active High. Control bus chip select.
Data OUT Bus Interface Signals		
data_out[63:0]	O	A 64-bit bus connecting to the FIFOs. Used by the FPGA to write data from the FPGA to the PCI bus via the three output FIFOs.
data_outCS	O	Active High. Chip select for the data_out bus.
data_outDES[1:0]	O	Destination select for the data_out bus. 00 Transmit FIFO0 01 Transmit FIFO1 10 Target/Read Post FIFO 11 No destination (parked)
data_out_byte_sel[2:0]	O	Lane shifting selection for the construction registers before the FIFOs data_out_BE[7:0] are also shifted accordingly. Sets the number of bytes to barrel shift the 64-bit data_out bus and the 8-bit data_outBE bus.
data_outBE[7:0]	O	Active High. Indicates which byte lane is active for the current transfer occurring on data_out[63:0]. data_outBE[7] data_out[63:56] data_outBE[6] data_out[55:48] data_outBE[5] data_out[47:40] data_outBE[4] data_out[39:32] data_outBE[3] data_out[31:24] data_outBE[2] data_out[23:16] data_outBE[1] data_out[15:08] data_outBE[0] data_out[07:00]

Table 2: PCI Back-End Interface Signals (Continued)

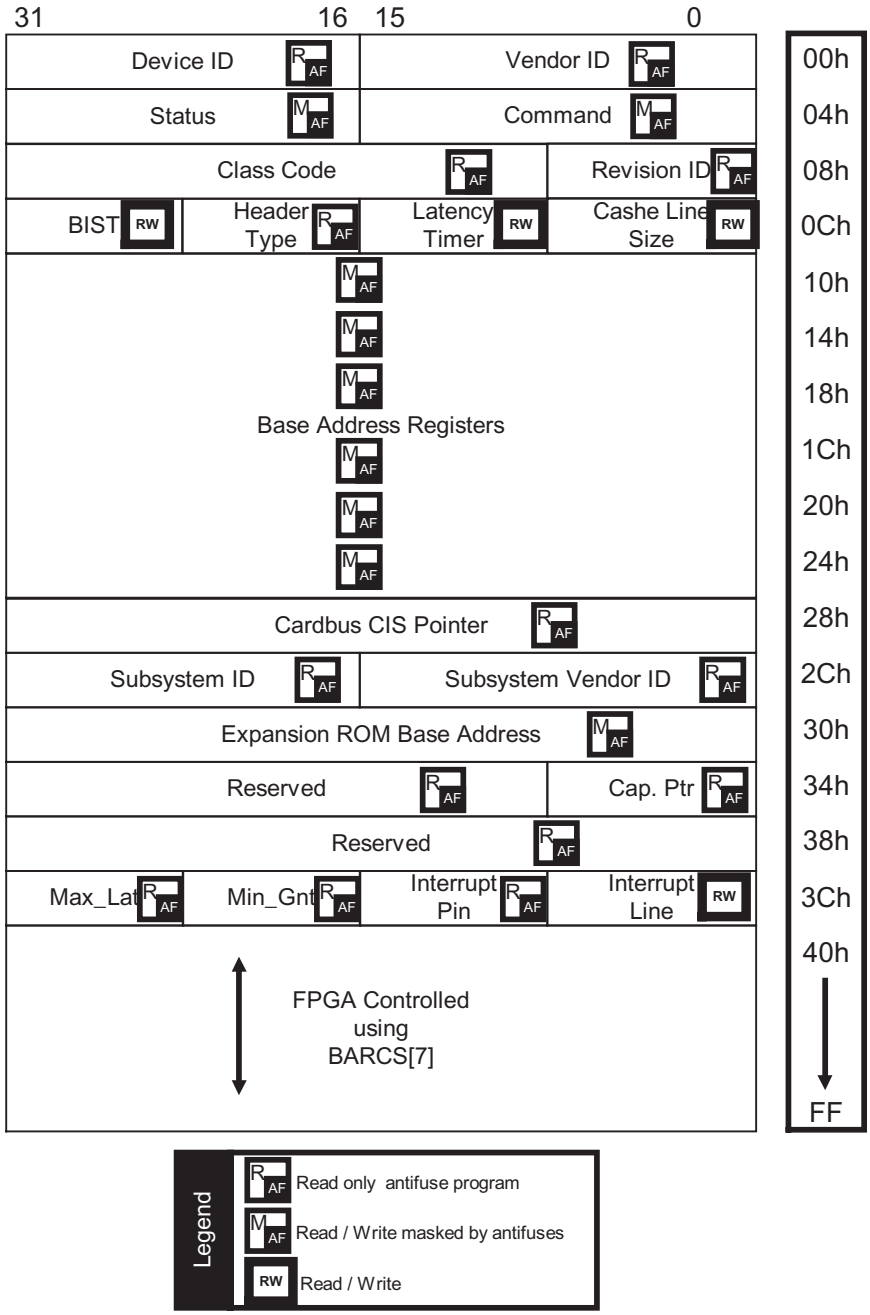
Symbol	I/O[a]	Description
Interrupt Control		
interrupt_i	O	Active High and level sensitive. When active and not masked, asserts a PCI interrupt.
interrupt_o	I	Active High. Indicates an interrupt is pending for the FPGA to service.
Master Arbitration Control		
fpga_loc_sel[1:0]	O	FPGA arbitration select. If the FPGA has control of the master-modeling arbitration, these bits determine which DMA channel should initiate a DMA transfer after the next arbitration cycle. Has relationship to pci_clk. 00 => Receive channel 1 has access to the bus 01 => Receive channel 0 has access to the bus 10 => Transmit channel 1 has access to the bus 11 => Transmit channel 0 has access to the bus
fpga_bus_req[3:0]	I	Active High. Master request status. Indicates that the respective master has need to access the PCI bus. Has relationship to pci_clk. fpga_bus_req[0] = receive channel 1 fpga_bus_req[1] = receive channel 0 fpga_bus_req[2] = transmit channel 1 fpga_bus_req[3] = transmit channel 0

a. I = Input from PCI to FPGA
O = Output from FPGA to PCI

Configuration Space

Defaults for most configuration space parameters can be programmed into the Via-Link antifuse-based configuration region in the device. Also, by fully supporting the extended configuration space region beyond the 40(hex), the full enhanced feature set of the PCI bus is available to the user.

Figure 11: Configuration Space Block Diagram



AC Characteristics

The AC characteristics are calculated at V_{CC} = 3.3 V, T_A = 25°C (K=1.00). To calculate delays, multiply the appropriate K factor in **Table 15** by the numbers presented in **Table 3** through **Table 10**. Logic cell diagrams and waveforms are provided from **Figure 12** through **Figure 20**.

Figure 12: QuickPCI Logic Cell Configuration

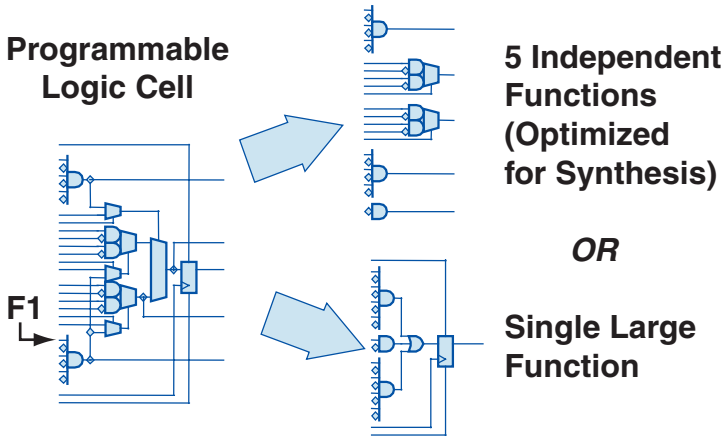


Table 3: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{PD}	Combinatorial Delay[b]	1.4	1.7	2.0	2.3	3.5
t_{SU}	Setup Time[b]	1.8	1.8	1.8	1.8	1.8
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.8	1.1	1.4	1.7	2.9
t_{CWHI}	Clock High Time	1.6	1.6	1.6	1.6	1.6
t_{CWLO}	Clock Low Time	1.6	1.6	1.6	1.6	1.6
t_{SET}	Set Delay	1.4	1.7	2.0	2.3	3.5
t_{RESET}	Reset Delay	1.2	1.5	1.8	2.1	3.3
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.
b. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 4: RAM Cell Synchronous Write Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	8
t_{SWA}	WA Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWA}	WA Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{SWD}	WD Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWD}	WD Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{SWE}	WE Setup Time to WCLK	1.0	1.0	1.0	1.0	1.0
t_{HWE}	WE Hold Time to WCLK	0.0	0.0	0.0	0.0	0.0
t_{WCRD}	WCLK to RD (WA=RA)[a]	5.0	5.3	5.6	5.9	7.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 5: RAM Cell Synchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{SRA}	RA Setup Time to RCLK	1.0	1.0	1.0	1.0	1.0
t_{HRA}	RA Hold Time to RCLK	0.0	0.0	0.0	0.0	0.0
t_{SRE}	RE Setup Time to RCLK	1.0	1.0	1.0	1.0	1.0
t_{HRE}	RE Hold Time to RCLK	0.0	0.0	0.0	0.0	0.0
t_{RCRD}	RCLK to RD[b]]	4.0	4.3	4.6	4.9	6.1

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.
b. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 6: RAM Cell Asynchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	8
RPDRD	RA to RD[a]	3.0	3.3	3.6	3.9	5.1

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 7: Input-Only Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register Clock Enable Setup Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 8: Clock Cells

Symbols	Parameter	Propagation Delays (ns) Loads per Half Column[a]										
		1	2	3	4	8	10	12	14	16	18	20
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	.16	1.7	1.8	1.9	2	2.1
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3	1.4	1.5	1.6	1.7

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 8 loads per half column. The global clock has up to 11 loads per half column.

Table 9: I/O Cell Input Delays

Symbol	Parameter	Propagation Delays (ns) Fanout[a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock To Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register Clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and T_A = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 10: I/O Cell Output Delays

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-State [a]	2.0				
t_{PLZ}	Output Delay Low to Tri-State [a]	1.2				

a. Loads are used for t_{PXZ}.

The loads presented in **Figure 13** are used for t_{PXZ}.

Figure 13: Loads used for t_{PXZ}

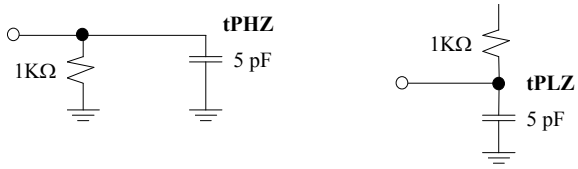


Table 11: PCI DC Specifications for 3.3 V Signaling

Symbol	Parameter	Condition	Min.	Max.	Units
Vcc	Supply Voltage		3.0	3.6	V
Vcc	Supply Voltage (for 75MHz only)		3.15	3.6	V
Vih	Input High Voltage		0.5Vcc	Vcc+0.5	V
Vil	Input Low Voltage		-0.5	0.3Vcc	V
Vipu	Input Pull-up Voltage		0.7Vcc		V
Iil	Input Leakage Current	0<Vin<Vcc		±10	mA
Voh	Output High Voltage	Iout=-500mA	0.9Vcc		V
Vol	Output Low Voltage	Iout=1500mA		0.1Vcc	V
Cin	Input Pin Capacitance			10	pF
Cclk	CLK Pin Capacitance		5	12	pF
CIDSEL	IDSEL Pin Capacitance			8	PF
Lpin	Pin Inductance			20	nH
Ioff	PME# Input Leakage	Vo£3.6VVcc off or floating	-	1	mA

Table 12: PCI DC Specifications for 5 V Signaling

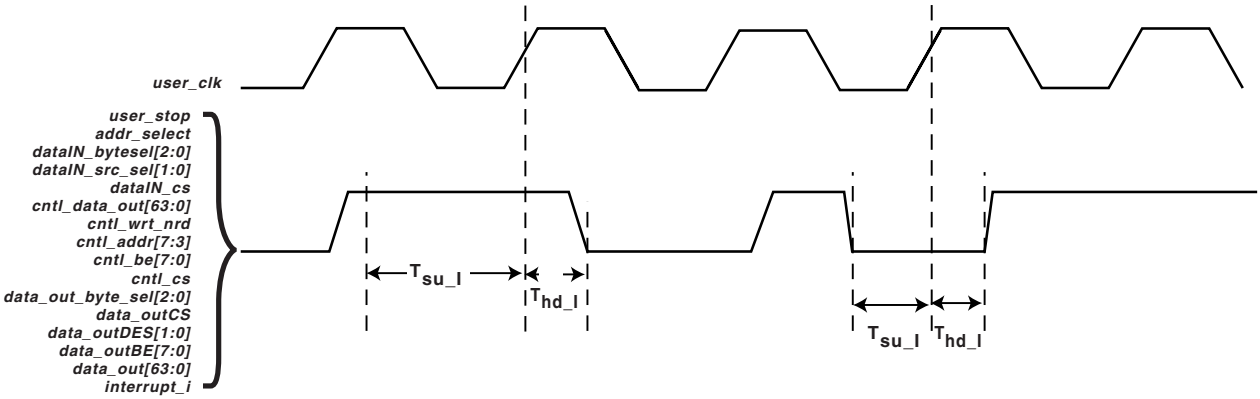
Symbol	Parameter	Condition	Min.	Max.	Units
Vcc	Supply Voltage		4.75	5.25	V
Vih	Input High Voltage		2.0	Vcc+0.5	V
Vil	Input Low Voltage		-0.5	0.8	V
Iih	Input High Leakage Current	Vin=2.7		70	mA
Iil	Input Low Leakage Current	Vin=0.5		-70	mA
Voh	Output High Voltage	Iout=-2mA	2.4		V
Vol	Output Low Voltage	Iout=3mA, 6mA		0.55	V
Cin	Input Pin Capacitance			10	pF
Cclk	CLK Pin Capacitance		5	12	pF
CIDSEL	IDSEL Pin Capacitance			8	PF
Lpin	Pin Inductance			20	nH
Ioff	PME# input leakage	Vo£5.25VVcc off or floating	-	1	mA

Table 13: PCI Timing Parameters

Symbol	Parameter	75 MHz		66 MHz		33 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Tval	CLK to Signal Valid Delay -bused signals	2	5.34	2	6	2	11	ns
Tval (ptp)	CLK to Signal Valid Delay - point to point signals	2	5.34	2	6	2	12	ns
Ton	Float to Active Delay	2	-	2	-	2	-	ns
Toff	Active to Float Delay	-	12.45	-	14	-	28	ns
Tsu	Input Setup Time to CLK - bused signals	2.67	-	3	-	7	-	ns
Tsu(ptp)	Input Setup Time to CLK - point to point signals	4.45	-	5	-	10, 12	-	ns
Th	Input Hold Time from CLK	0	-	0	-	0	-	ns
Trst	Reset Active Time after power stable	1	-	1	-	1	-	ms
Trst-clk	Reset Active Time after CLK stable	100	-	100	-	100	-	ms
Trst-off	Reset Active to output float delay	-	40	-	40	-	40	ns
trrsu	REQ64# to RST# setup time	10Tcyc	-	10Tcyc	-	10Tcyc	-	ns
trrh	RST# to REQ64# hold time	0	50	0	50	0	50	ns
Trhfa	RST# high to first Configuration access	225	-	225	-	225	-	clocks
Trhff	RST# high to first FRAME# assertion	5		5		5		clocks

Timing Diagrams

Figure 14: FPGA to PCI Core Signal Timing



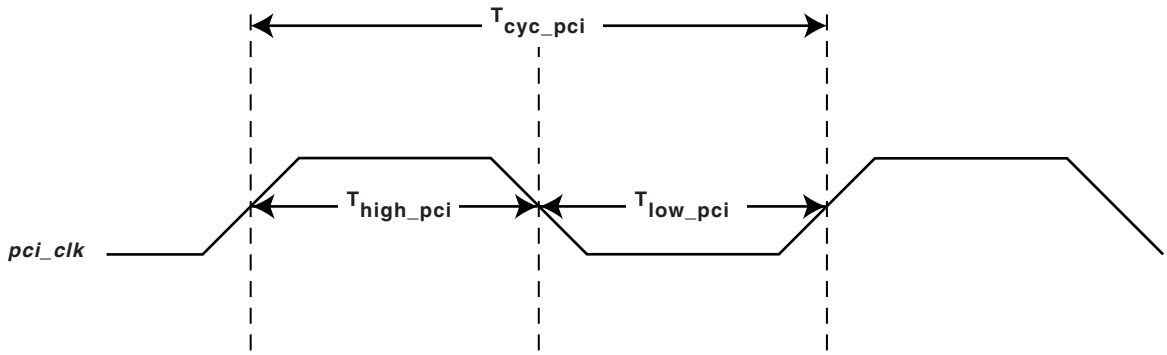
For Signals: data_out[*], data_outBE[*], dataIN_bytesel[*], cntl_data_out[*], cntl_be[*], addr_select, user_stop, interrupt_i

Symbol	Parameter	33A/66A Best	33A/66A Nominal	33A/66A Worst	33B/66B Best	33B/66B Nominal	33B/66B Worst	75C Best	75C Nominal	75C Worst	Unit
T_{su_I}		1.425	1.890	2.850	1.425	1.828	2.726	1.425	1.673	2.416	ns
T_{hd_I}		0.5	—	—	0.5	—	—	0.5	—	—	ns

For Signals: data_outCS, data_outDES[*], data_out_byte_sel[*], dataIN_src_sel[*], dataIN_cs, cntl_wrt_nrd, cntl_addr[*], cntl_cs

Symbol	Parameter	33A/66A Best	33A/66A Nominal	33A/66A Worst	33B/66B Best	33B/66B Nominal	33B/66B Worst	75C Best	75C Nominal	75C Worst	Unit
T_{su_I}		2.015	2.672	4.030	2.015	2.584	3.854	2.015	2.365	3.416	ns
T_{hd_I}		0.5	—	—	0.5	—	—	0.5	—	—	ns

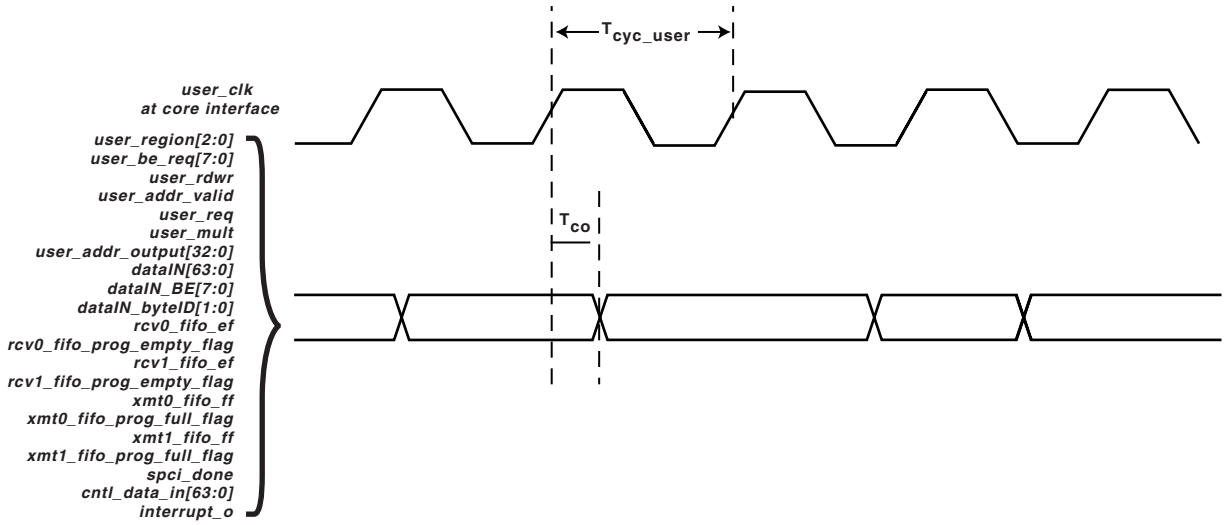
Figure 15: PCI Clock Signal AC Parameters



Symbol	Parameter	33A/66A Min.	33A/66A Max.	33B/66B Min.	33B/66B Max.	75C Min.	75C Max.	Unit
T_{cyc_pci}	***pci_clk*** cycle time	30/15	—	30/15	—	13.33	—	ns
T_{high_pci}	***pci_clk*** high time	11	—	6	—	5.3	—	ns
T_{low_pci}	***pci_clk*** low time	11	—	6	—	5.3	—	ns
	pci_clk slew rate[1]	1	4	1.5	4	1.5	4	V/ns

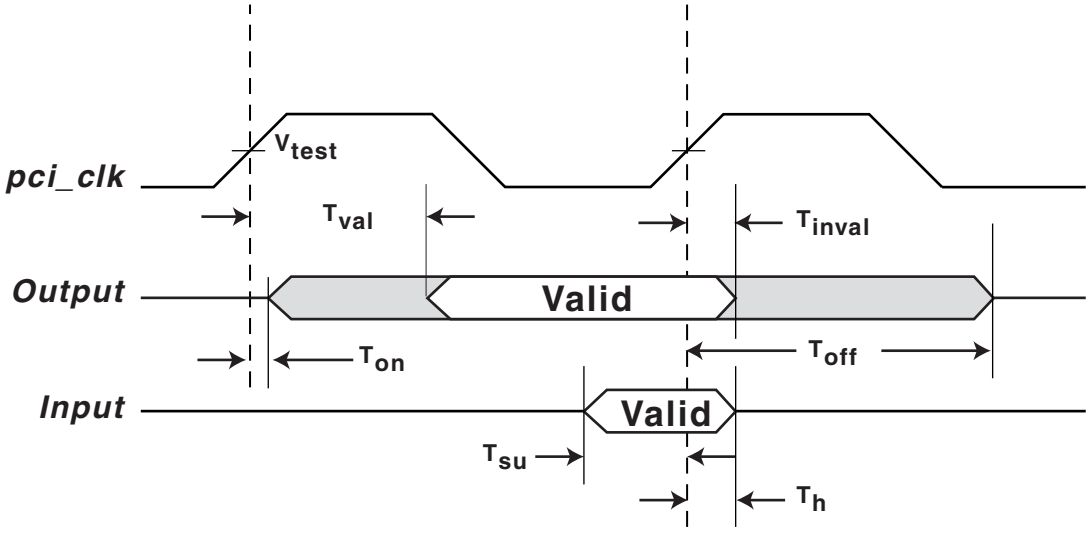
[1] 0.2 V_{cc} to 0.6 V_{cc}

Figure 16: PCI Core to FPGA Signal Timing



Symbol	Parameter	33A/66A			33B/66B			75C			Unit
		Best	Nominal	Worst	Best	Nominal	Worst	Best	Nominal	Worst	
T_{cyc_user}	***user_clk*** cycle time	10	—	—	10	—	—	10	—	—	ns
T_{co}		3.071	4.072	6.141	3.071	3.939	5.874	3.071	3.605	5.207	ns

Figure 17: PCI Signal Timing Specifications

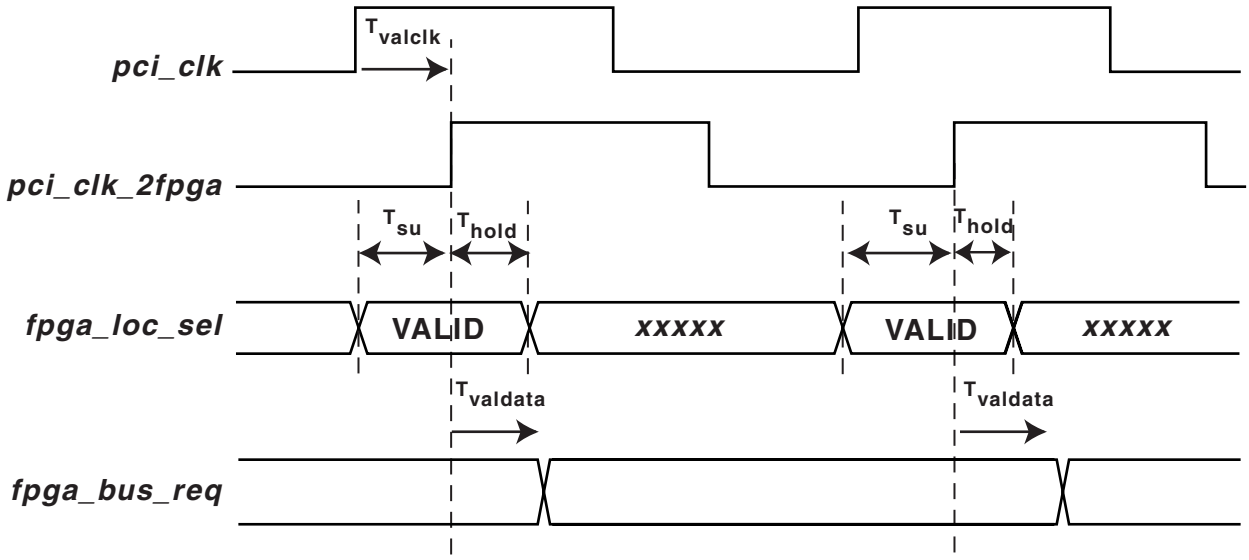


Note: V_{test}—1.5V for 5-V signals; 0.4 V_{cc} for 3.3-V signals

Symbol	Parameter	33A/66A Min.	33A/66A Max.	33B/66B Min.	33B/66B Max.	75C Min.	75C Max.	Unit
T_{val}	***pci_clk*** to signal valid delay—bussed signals	2	11	2	6	2	5.33	ns
$T_{val(ptp)}$	***pci_clk*** to signal valid delay—point-to-point	2	12	2	6	2	5.33	ns
T_{on}	Reset float to active delay	2	—	2	—	2	—	ns
T_{off}	Reset active to float delay	—	28	—	14	—	12	ns
T_{su}	Input setup time to ***pci_clk***—bussed signals	7	—	3	—	2.66	—	ns
$T_{su(ptp)}$	Input setup time to ***pci_clk***—point-to-point	10	—	5	—	4.44	—	ns
T_h	Input signal hold time from ***pci_clk***	0	—	0	—	0	—	ns

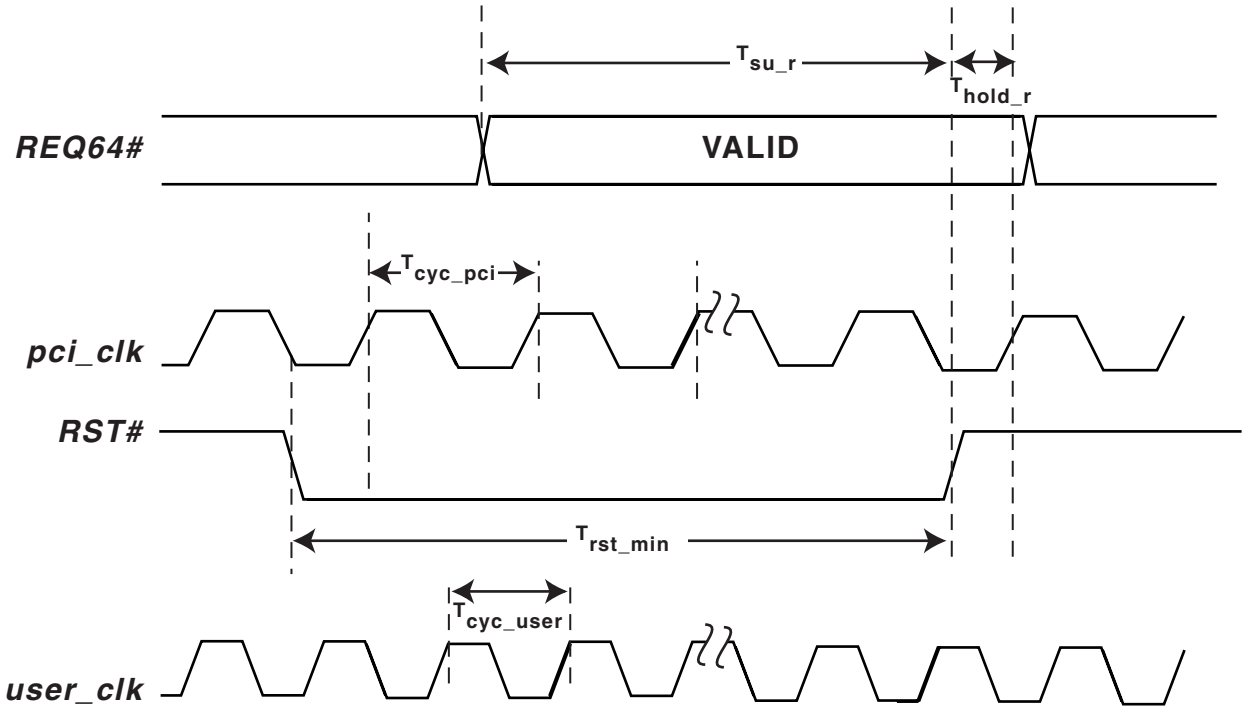
Note: All primary interface signals are synchronized to ***p_clk***.
All secondary interface signals are synchronized to ***s_clk.***

Figure 18: PCI Clock Related Interface Timing



Symbol	Parameter	33A/66A Best	33A/66A Nominal	33A/66A Worst	33B/66B Best	33B/66B Nominal	33B/66B Worst	75C Best	75C Nominal	75C Worst	Unit
T_{valclk}		2.040	2.705	4.080	2.040	2.617	3.903	2.040	2.395	3.459	ns
T_{su}		1.831	2.404	3.625	1.813	2.325	3.467	1.813	2.128	3.073	ns
T_{hold}		0	—	—	0	—	—	0	—	—	ns
$T_{valdata}$		3.946	5.232	7.891	3.946	5.061	7.548	3.946	4.632	6.691	ns

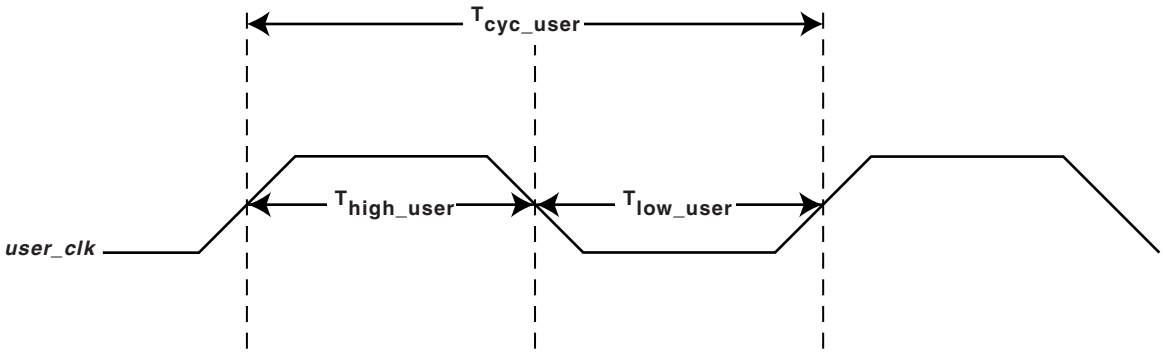
Figure 19: PCI Reset Signal AC Parameter



Symbol	Parameter	33A/66A Min.	33A/66A Max.	33B/66B Min.	33B/66B Max.	75C Min.	75C Max.	Unit
T_{cyc_user}	***user_clk*** cycle time	10	—	10	—	10	—	ns
T_{cyc_pci}	***pci_clk*** cycle time	30/15	—	30/15	—	13.33	—	ns
T_{su_r}		300	—	150	—	133	—	ns
T_{hold_r}		0	—	0	—	0	—	ns
T_{rst_min}[1]		4 ***pci_clk*** followed by 4 ***user_clk***						clk periods

[1]User_clk must be running for proper reset function to complete.

Figure 20: User Clock Signal AC Parameter



Symbol	Parameter	33A/66A Min.	33A/66A Max.	33B/66B Min.	33B/66B Max.	75C Min.	75C Max.	Unit
T_{cyc_user}	***user_clk*** cycle time	10	—	10	—	10	—	ns
T_{high_user}	***user_clk*** high time	2	—	2	—	2	—	ns
T_{low_user}	***user_clk*** low time	2	—	2	—	2	—	ns

DC Characteristics

The DC Specifications are provided in the **Table 14** through **Table 16**.

Table 14: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 to 4.6V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 to 7.0V	ESD Pad Protection	±2000V
Input Voltage	-0.5V to V_{CCIO} +0.5V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Max Lead Temperature	300°C

Table 15: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{CC}	Supply Voltage		3.15	3.6	3.0	3.6	3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.15	5.5	3.0	5.5	3.0	5.25	V
T_A	Ambient Temperature		-55		-40	85	0	70	°C
T_J	Junction Temperature			125					
K	Delay Factor	-33A Speed Grade	0.42	1.04	0.43	1.02	0.46	0.99	
		-33B Speed Grade	0.42	0.92	0.43	0.90	0.46	0.88	
		-66A Speed Grade	0.42	1.04	0.43	1.02	0.46	0.99	
		-66B Speed Grade	0.42	0.92	0.43	0.90	0.46	0.88	
		-75C Speed Grade[a]	NA	NA	0.43	0.81	0.46	0.79	

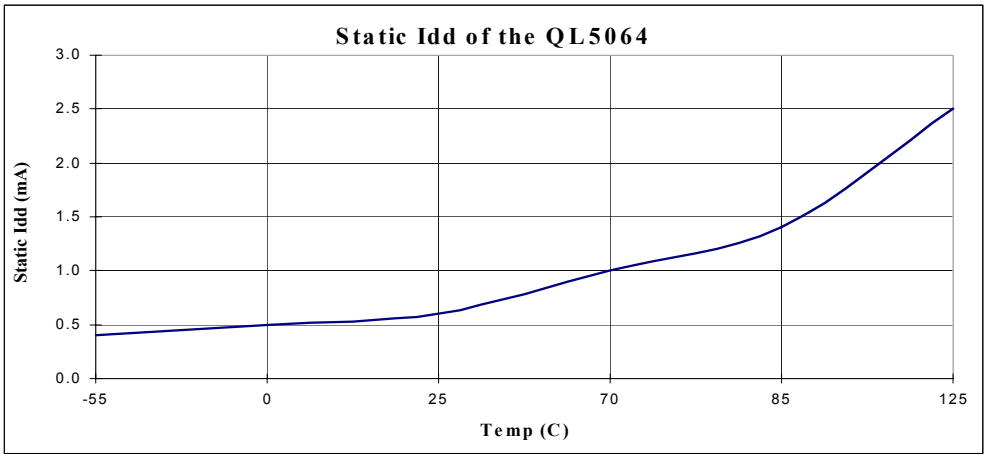
a. At V_{CC} minimum of 3.15 V.

Table 16: DC Input and Output Levels

Symbol	Parameter	Conditions	Min.	Max.	Unit
VIH	Input HIGH Voltage		0.5 VCC	VCCIO+0.5	V
VIL	Input LOW Voltage		-0.5	0.3VCC	V
VOH	Output HIGH Voltage	IOH = -12 mA	2.4		V
		IOH = -500 mA	0.9VCC		V
VOL	Output LOW Voltage	IOL = 16 mA		0.45	V
		IOL = 1.5 mA		0.1VCC	V
II	I or I/O Input Leakage Current	VI = VCCIO or GND	-10	10	mA
IOZ	3-State Output Leakage Current	VI = VCCIO or GND	-10	10	mA
CI	Input Capacitance [a]			10	pF
IOS	Output Short Circuit Current [b]	VO = GND	-15	-180	mA
		VO = VCC	40	210	mA
ICC	Quiescent Current [c]	VI, VIO = VCCIO or GND	0.50 (typ.)	4	mA
ICCIO	Quiescent Current on VCCIO		0	100	mA
Idd	Static Idd Current	See **Figure 21**			

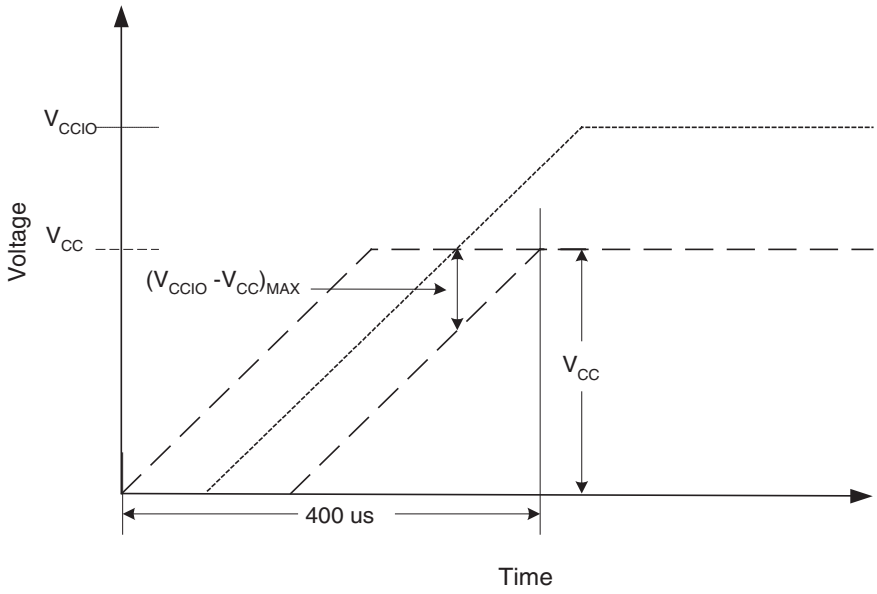
a. Capacitance is sample tested only.
b. Only one output at a time. Duration should not exceed 30 seconds.
c. For commercial grade devices only. Maximum ICC is 5 mA for all industrial grade devices.
For AC conditions, contact QuickLogic Customer Engineering.

Figure 21: Static Idd of the QL5064



Power-up Sequencing

Figure 22: Power-up Sequencing



When powering up a device, the V_{CC}/V_{CCIO} rails must take 400 µs or longer to reach the maximum value (refer to **Figure 22**).

NOTE: Ramping V_{CC}/V_{CCIO} to the maximum voltage faster than 400 µs can cause the device to behave improperly.

For users with a limited power budget, keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV when ramping up the power supply.

QL5064 Pin Type Descriptions

The QL5064 device pins are indicated in the **Table 17**. These are pins on the device, some of which connect to the PCI bus, and others that are programmable as user I/O.

Table 17: Pin Type Descriptions

Type	Description
IN	**Input.** A standard input-only signal.
OUT	**Totem Pole Output.** A standard active output driver.
T/S	Tri-state. A bi-directional, tri-state input/output pin.
S/T/S	**Sustained Tri-State.** An active low tri-state signal driven by one PCI agent at a time. It must be driven high for at least one clock before being disabled (set to Hi-Z). A pull-up needs to be provided by the PCI system central resource to sustain the inactive state once the active driver has released the signal.
O/D	**Open Drain.** Allows multiple devices to share this pin as a wired-or.

Table 18: Pin / Bus Names and Functions

Pin/Bus Name	Type	Function
VCC	IN	**Supply Pin.** Tie to 3.3 V supply.
VCCIO	IN	**Supply Pin for I/O.** Set to 3.3 V for 3.3 V I/O, 5 V for 5.0 V compliant I/O.
GND	IN	**Ground Pin.** Tie to GND on the PCB.
T/GND	IN	**Thermal Ground.** Used to dissipate heat from the device. Tie to GND on the PCB.
I/O	T/S	**Programmable Input/Output/Tri-State/Bi-directional Pin.**
I/GCLK	IN	**Programmable Input-Only or Global Clock Pin.** Tie to VCC or GND if unused.
I/ACLK	IN	**Programmable Input-Only or Array Clock Pin.** Tie to VCC or GND if unused.
TDI	IN	**JTAG Data In.** Tie to VCC if unused.
TDO	OUT	**JTAG Data Out.** Leave unconnected if unused.
TCL	IN	**JTAG Clock.** Tie to GND if unused.
TMS	IN	**JTAG Test Mode Select.** Tie to VCC if unused.
TRSTB	IN	**JTAG Reset.** Tie to GND if unused.
STM	IN	**QuickLogic Reserved Pin.** Tie to GND on the PCB.
FLOAT	OUT	**Test Data Out Pin for QuickLogic Use Only.** Must be isolated and floating at all times

QL5064 External Device Pins

Table 19: QL5064 External Device Pins

Pin/Bus Name	Type	Function
AD[63:0]	T/S	**PCI Address and Data.** 32-bit multiplexed address/data bus.
CBEN[7:0]	T/S	**PCI Bus Command and Byte Enables.** Multiplexed bus which contains byte enables for AD[31:0] or the Bus Command during the address phase of a PCI transaction.
PAR	T/S	**PCI Parity.** Even Parity across AD[31:0] and C/BEN[3:0] busses. Driven one clock after address or data phases. Master drives PAR on address cycles and PCI writes. The Target drives PAR on PCI reads.
PAR64	T/S	**PCI Parity Upper DWORD.** Even Parity across AD[63:32] and C/BEN[7:4] busses.
FRAMEN	S/T/S	**PCI Cycle Frame.** Driven active by current PCI Master during a PCI transaction. Driven low to indicate the address cycle, driven high at the end of the transaction.
REQ64N	S/T/S	**PCI Request 64-bit transfer.** Driven by the PCI Master to request a 64-bit transfer. Same signal timing as FRAMEN.
DEVSELN	S/T/S	**PCI Device Select.** Driven by a Target that has decoded a valid base address.
ACK64N	S/T/S	**PCI Acknowledge 64-bit Transfer.** Driven by a Target which has decoded a valid base address for a 64-bit data transfer. Same timing as DEVSELN.
CLK	IN	**PCI System Clock Input.**
RSTN	IN	**PCI System Reset Input.**
REQN	T/S	**PCI Request.** Indicates to the Arbiter that this PCI Agent (Initiator) wishes to use the bus. A point to point signal between the PCI Device and the System Arbiter.
GNTN	IN	**PCI Grant.** Indicates to a PCI Agent (Initiator) that it has been granted access to the PCI bus by the Arbiter. A point to point signal between the PCI device and the System Arbiter.
PERRN	S/T/S	**PCI Data Parity Error.** Driven active by the initiator or target two clock cycles after a data parity error is detected on the AD and C/BEN busses.
SERRN	O/D	**PCI System Error.** Driven active when an address cycle parity error, data parity error during a special cycle, or other catastrophic error is detected.
IDSEL	IN	**PCI Initialization Device Select.** Use to select a specific PCI Agent during System Initialization.
IRDYN	S/T/S	**PCI Initiator Ready.** Indicates the Initiator's ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDYN and TRDYN are active.
TRDYN	S/T/S	**PCI Target Ready.** Indicates the Target's ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDYN and TRDYN are active.
STOPN	S/T/S	**PCI Stop.** Used by a PCI Target to end a burst transaction.
INTAN	O/D	**Interrupt A.** Asynchronous Active-Low Interrupt Request.

NOTE: Signal names that end in the character 'N" are active-low (for example, Mst_IRDYN).

456 Pin PBGA Pinout Diagram

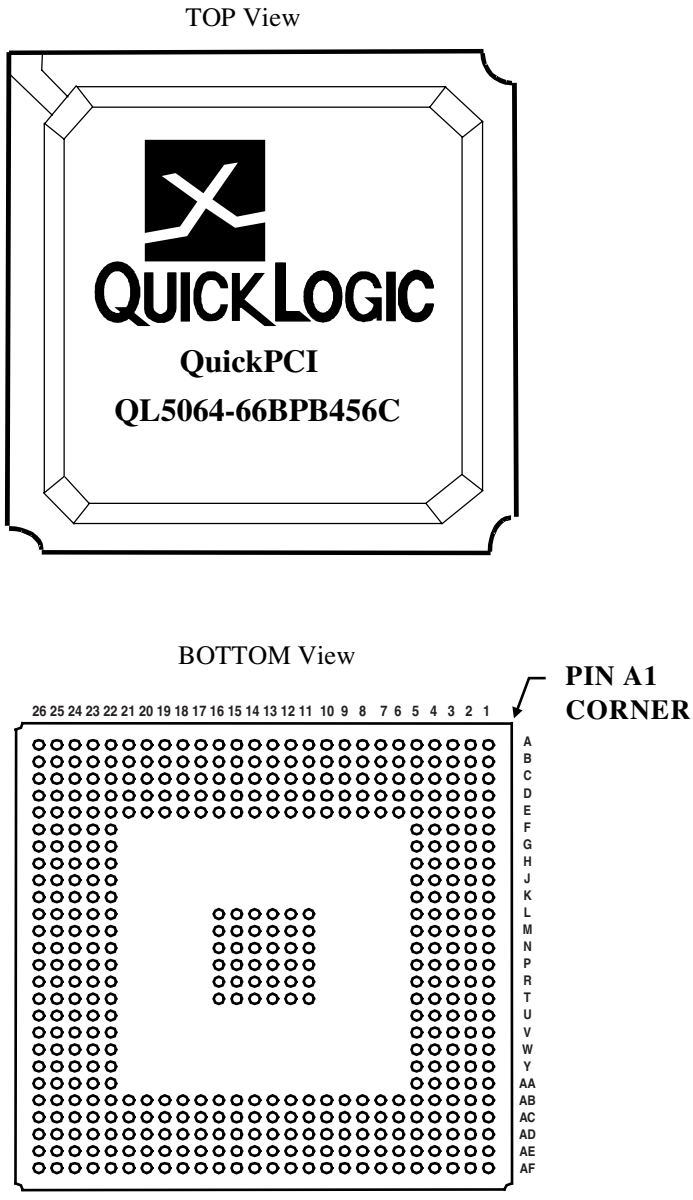


Figure 23: 456 Pin PBGA Pinout Diagram

456 Pin PBGA Pinout Table

Table 20: 456 PBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	NC	B11	NC	C21	I/O	E5	GND	G5	NC	L1	STOPN
A2	NC	B12	NC	C22	I/O	E6	VCC	G22	GND	L2	TRDYN
A3	AD[29]	B13	I/O	C23	I/O	E7	GND	G23	I/O	L3	IRDYN
A4	REQN	B14	I/O	C24	I/O	E8	NC	G24	I/O	L4	CBEN[0]
A5	GNTN	B15	I/O	C25	TCK	E9	GND	G25	I/O	L5	NC
A6	AD[22]	B16	I/O	C26	I/O	E10	NC	G26	I/O	L11	T/GND
A7	AD[28]	B17	I/O	D1	AD[21]	E11	GND	H1	AD[14]	L12	T/GND
A8	RSTN	B18	I/O	D2	AD[23]	E12	GND	H2	CBEN[1]	L13	T/GND
A9	FLOAT	B19	I/O	D3	NC	E13	VCC	H3	AD[13]	L14	T/GND
A10	NC	B20	I/O	D4	GND	E14	GND	H4	NC	L15	T/GND
A11	NC	B21	I/O	D5	AD[16]	E15	GND	H5	NC	L16	T/GND
A12	VCCIO	B22	I/O	D6	NC	E16	GND	H22	I/O	L22	I/O
A13	I/O	B23	I/O	D7	IDSEL	E17	I/O	H23	I/O	L23	I/O
A14	I/O	B24	I/O	D8	NC	E18	GND	H24	I/O	L24	I/O
A15	I/O	B25	I/O	D9	GND	E19	I/O	H25	I/O	L25	I/O
A16	I/O	B26	STM	D10	FLOAT	E20	GND	H26	I/O	L26	I/O
A17	I/O	C1	CBEN[3]	D11	NC	E21	VCC	J1	AD[10]	M1	AD[6]
A18	I/O	C2	AD[25]	D12	GND	E22	GND	J2	AD[12]	M2	GCLK
A19	I/O	C3	NC	D13	I/O	E23	I/O	J3	AD[11]	M3	ACK64N
A20	I/O	C4	TDO	D14	I/O	E24	I/O	J4	NC	M4	NC
A21	I/O	C5	AD[27]	D15	GND	E25	I/O	J5	GND	M5	GND
A22	I/O	C6	AD[18]	D16	I/O	E26	I/O	J22	I/O	M11	T/GND
A23	I/O	C7	AD[24]	D17	I/O	F1	DEVSELN	J23	I/O	M12	T/GND
A24	I/O	C8	NC	D18	GND	F2	CBEN[2]	J24	I/O	M13	T/GND
A25	I/O	C9	VCCIO	D19	I/O	F3	PAR	J25	I/O	M14	T/GND
A26	I/O	C10	NC	D20	I/O	F4	NC	J26	I/O	M15	T/GND
B1	NC	C11	NC	D21	I/O	F5	VCC	K1	FRAMEN	M16	T/GND
B2	NC	C12	I/O	D22	I/O	F22	VCC	K2	NC	M22	I/O
B3	NC	C13	I/O	D23	GND	F23	I/O	K3	AD[9]	M23	I/O
B4	AD[31]	C14	I/O	D24	I/O	F24	I/O	K4	NC	M24	I/O
B5	AD[30]	C15	I/O	D25	I/O	F25	I/O	K5	VCC	M25	I/O
B6	AD[20]	C16	I/O	D26	I/O	F26	I/O	K22	GND	M26	I/O
B7	AD[26]	C17	I/O	E1	AD[17]	G1	SERRN	K23	I/O	N1	GCLK
B8	INTAN	C18	I/O	E2	AD[19]	G2	PERRN	K24	I/O	N2	NC
B9	FLOAT	C19	I/O	E3	NC	G3	AD[15]	K25	I/O	N3	PCI CLK
B10	NC	C20	I/O	E4	NC	G4	NC	K26	I/O	N4	GCLK
N5	VCC	R23	I/O	W1	AD[61]	AB11	GND	AC25	I/O	AE13	I/O
N11	T/GND	R24	I/O	W2	AD[59]	AB12	I/O	AC26	I/O	AE14	I/O
N12	T/GND	R25	I/O	W3	AD[58]	AB13	I/O	AD1	NC	AE15	I/O
N13	T/GND	R26	GCLK/I (USER CLK)	W4	AD[56]	AB14	GND	AD2	NC	AE16	I/O
N14	T/GND	T1	AD[3]	W5	NC	AB15	VCC	AD3	AD[45]	AE17	I/O
N15	T/GND	T2	AD[1]	W22	I/O	AB16	I/O	AD4	AD[46]	AE18	I/O
N16	T/GND	T3	CBEN[7]	W23	I/O	AB17	I/O	AD5	AD[44]	AE19	I/O
N22	GND	T4	CBEN[5]	W24	I/O	AB18	VCC	AD6	AD[38]	AE20	I/O
N23	I/O	T5	VCC	W25	I/O	AB19	GND	AD7	NC	AE21	I/O
N24	I/O	T11	T/GND	W26	I/O	AB20	I/O	AD8	FLOAT	AE22	I/O
N25	I/O	T12	T/GND	Y1	AD[57]	AB21	VCC	AD9	NC	AE23	I/O
N26	I/O	T13	T/GND	Y2	AD[55]	AB22	GND	AD10	NC	AE24	TMS

Table 20: 456 PBGA Pinout Table (Continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
P1	AD[4]	T14	T/GND	Y3	AD[54]	AB23	I/O	AD11	I/O	AE25	NC
P2	AD[8]	T15	T/GND	Y4	AD[52]	AB24	I/O	AD12	I/O	AE26	I/O
P3	AD[2]	T16	T/GND	Y5	NC	AB25	I/O	AD13	I/O	AF1	AD[43]
P4	AD[0]	T22	GND	Y22	GND	AB26	I/O	AD14	I/O	AF2	AD[39]
P5	NC	T23	I/O	Y23	I/O	AC1	NC	AD15	I/O	AF3	AD[35]
P11	T/GND	T24	I/O	Y24	I/O	AC2	NC	AD16	I/O	AF4	AD[33]
P12	T/GND	T25	I/O	Y25	I/O	AC3	NC	AD17	I/O	AF5	AD[32]
P13	T/GND	T26	I/O	Y26	I/O	AC4	GND	AD18	I/O	AF6	AD[34]
P14	T/GND	U1	NC	AA1	AD[53]	AC5	AD[48]	AD19	I/O	AF7	FLOAT
P15	T/GND	U2	CBEN[6]	AA2	AD[51]	AC6	NC	AD20	I/O	AF8	NC
P16	T/GND	U3	PAR64	AA3	AD[50]	AC7	NC	AD21	I/O	AF9	NC
P22	I/O	U4	AD[62]	AA4	NC	AC8	VCCIO	AD22	I/O	AF10	I/O
P23	GCLK/I	U5	GND	AA5	VCC	AC9	NC	AD23	TRSTB	AF11	I/O
P24	ACLK/I	U22	I/O	AA22	VCC	AC10	NC	AD24	I/O	AF12	I/O
P25	I/O	U23	I/O	AA23	NC	AC11	I/O	AD25	I/O	AF13	I/O
P26	ACLK/I	U24	I/O	AA24	I/O	AC12	I/O	AD26	NC	AF14	I/O
R1	AD[7]	U25	I/O	AA25	I/O	AC13	I/O	AE1	TDI	AF15	I/O
R2	AD[5]	U26	I/O	AA26	I/O	AC14	VCCIO	AE2	AD[41]	AF16	I/O
R3	REQ64N	V1	CBEN[4]	AB1	AD[49]	AC15	I/O	AE3	AD[37]	AF17	I/O
R4	NC	V2	AD[63]	AB2	AD[47]	AC16	I/O	AE4	AD[42]	AF18	I/O
R5	NC	V3	AD[60]	AB3	NC	AC17	I/O	AE5	AD[40]	AF19	I/O
R11	T/GND	V4	NC	AB4	NC	AC18	I/O	AE6	AD[36]	AF20	I/O
R12	T/GND	V5	NC	AB5	GND	AC19	I/O	AE7	NC	AF21	I/O
R13	T/GND	V22	GND	AB6	VCC	AC20	I/O	AE8	FLOAT	AF22	I/O
R14	T/GND	V23	I/O	AB7	NC	AC21	I/O	AE9	NC	AF23	I/O
R15	T/GND	V24	I/O	AB8	NC	AC22	I/O	AE10	NC	AF24	I/O
R16	T/GND	V25	I/O	AB9	NC	AC23	GND	AE11	I/O	AF25	I/O
R22	VCC	V26	I/O	AB10	VCC	AC24	I/O	AE12	I/O	AF26	I/O

484 Pin PBGA Pinout Diagram

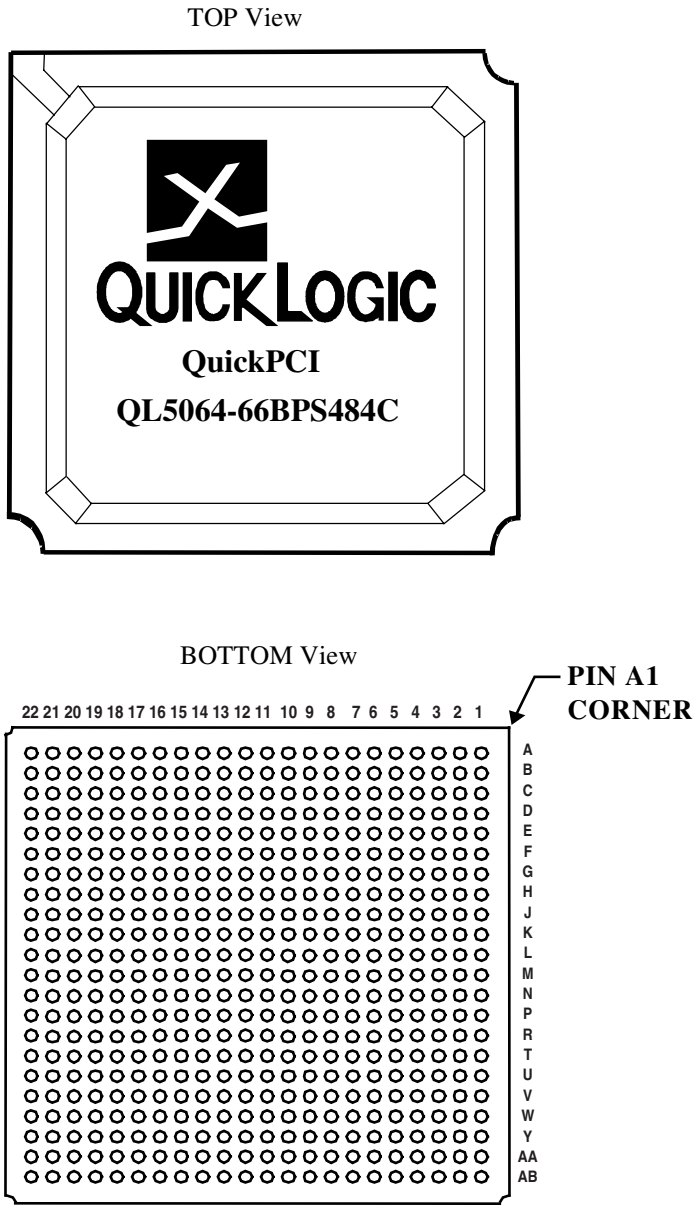


Figure 24: 484 Pin PBGA Pinout Diagram

484 Pin PBGA Pinout Table

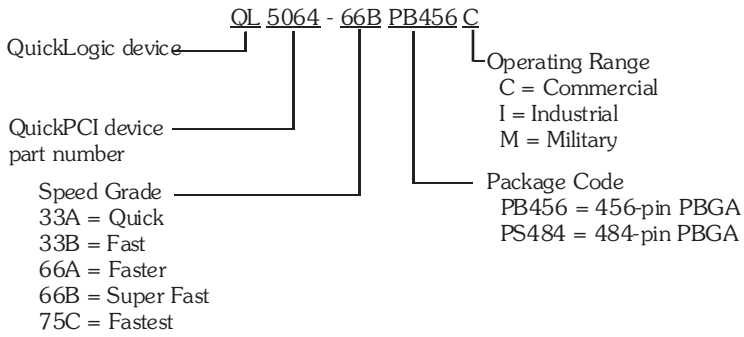
Table 21: 484 PBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A01	NC	B19	I/O	D15	I/O	F11	I/O	H7	VCC	K3	FRAMEN
A02	NC	B20	TCK	D16	I/O	F12	I/O	H8	GND	K4	STOPN
A03	AD[29]	B21	NC	D17	NC	F13	GND	H9	VCC	K5	IRDYN
A04	AD[27]	B22	NC	D18	NC	F14	I/O	H10	VCC	K6	VCC
A05	AD[30]	C1	AD[21]	D19	STM	F15	GND	H11	I/O	K7	VCC
A06	IDSEL	C2	NC	D20	I/O	F16	VCC	H12	GND	K8	GND
A07	AD[26]	C3	NC	D21	I/O	F17	I/O	H13	NC	K9	GND
A08	FLOAT	C4	NC	D22	I/O	F18	I/O	H14	VCC	K10	GND
A09	I/O	C5	AD[31]	E1	PERRN	F19	I/O	H15	GND	K11	GND
A10	I/O	C6	GNTN	E2	AD[15]	F20	I/O	H16	I/O	K12	GND
A11	I/O	C7	NC	E3	AD[25]	F21	I/O	H17	I/O	K13	GND
A12	I/O	C8	VCCIO	E4	AD[23]	F22	I/O	H18	I/O	K14	GND
A13	I/O	C9	I/O	E5	NC	G1	CBEN[1]	H19	NC	K15	GND
A14	I/O	C10	I/O	E6	VCC	G2	AD[13]	H20	I/O	K16	I/O
A15	I/O	C11	I/O	E7	AD[20]	G3	NC	H21	I/O	K17	I/O
A16	I/O	C12	I/O	E8	AD[28]	G4	SERRN	H22	I/O	K18	I/O
A17	I/O	C13	I/O	E9	FLOAT	G5	GND	J1	AD[9]	K19	I/O
A18	I/O	C14	I/O	E10	I/O	G6	VCC	J2	CBEN[0]	K20	I/O
A19	I/O	C15	I/O	E11	VCC	G7	GND	J3	NC	K21	I/O
A20	I/O	C16	I/O	E12	I/O	G8	INTAN	J4	AD[10]	K22	I/O
A21	NC	C17	I/O	E13	I/O	G9	GND	J5	GND	L1	AD[6]
A22	NC	C18	I/O	E14	I/O	G10	I/O	J6	GND	L2	GCLK
B1	NC	C19	I/O	E15	I/O	G11	GND	J7	GND	L3	GCLK
B2	NC	C20	I/O	E16	I/O	G12	NC	J8	VCC	L4	NC
B3	TDO	C21	I/O	E17	VCC	G13	I/O	J9	GND	L5	GCLK
B4	AD[16]	C22	I/O	E18	VCC	G14	GND	J10	GND	L6	ACK64N
B5	REQN	D1	CBEN[2]	E19	I/O	G15	GND	J11	GND	L7	GND
B6	AD[18]	D2	PAR	E20	I/O	G16	GND	J12	GND	L8	VCC
B7	AD[22]	D3	AD[19]	E21	I/O	G17	I/O	J13	GND	L9	GND
B8	RSTN	D4	CBEN[3]	E22	I/O	G18	I/O	J14	GND	L10	GND
B9	VCCIO	D5	NC	F1	DEVSELN	G19	I/O	J15	VCC	L11	GND
B10	I/O	D6	NC	F2	NC	G20	I/O	J16	GND	L12	GND
B11	I/O	D7	AD[24]	F3	AD[17]	G21	I/O	J17	I/O	L13	GND
B12	I/O	D8	NC	F4	NC	G22	I/O	J18	I/O	L14	GND
B13	I/O	D9	FLOAT	F5	NC	H1	AD[12]	J19	NC	L15	VCC
B14	I/O	D10	NC	F6	GND	H2	NC	J20	I/O	L16	GND
B15	I/O	D11	I/O	F7	VCC	H3	AD[11]	J21	I/O	L17	I/O
B16	I/O	D12	I/O	F8	GND	H4	NC	J22	I/O	L18	I/O
B17	I/O	D13	NC	F9	GND	H5	VCC	K1	TRDYN	L19	I/O
B18	I/O	D14	I/O	F10	GND	H6	AD[14]	K2	NC	L20	I/O

Table 21: 484 PBGA Pinout Table (Continued)

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
L21	I/O	N18	I/O	R15	GND	U12	I/O	W9	I/O	AA6	AD[48]
L22	I/O	N19	NC	R16	VCC	U13	I/O	W10	I/O	AA7	NC
M1	AD[4]	N20	I/O	R17	VCC	U14	I/O	W11	I/O	AA8	NC
M2	NC	N21	I/O	R18	I/O	U15	GND	W12	I/O	AA9	FLOAT
M3	AD[2]	N22	I/O	R19	I/O	U16	I/O	W13	I/O	AA10	I/O
M4	AD[0]	P1	AD[1]	R20	I/O	U17	GND	W14	I/O	AA11	I/O
M5	PCI CLK	P2	AD[3]	R21	I/O	U18	VCC	W15	I/O	AA12	I/O
M6	GND	P3	NC	R22	I/O	U19	I/O	W16	I/O	AA13	I/O
M7	GND	P4	CBEN[6]	T1	CBEN[4]	U20	I/O	W17	NC	AA14	I/O
M8	VCC	P5	GND	T2	AD[60]	U21	I/O	W18	NC	AA15	I/O
M9	GND	P6	VCC	T3	NC	U22	I/O	W19	NC	AA16	I/O
M10	GND	P7	GND	T4	AD[59]	V1	AD[55]	W20	I/O	AA17	I/O
M11	GND	P8	GND	T5	GND	V2	AD[56]	W21	I/O	AA18	I/O
M12	GND	P9	GND	T6	AD[62]	V3	NC	W22	I/O	AA19	TMS
M13	GND	P10	GND	T7	GND	V4	AD[47]	Y1	AD[52]	AA20	I/O
M14	GND	P11	GND	T8	GND	V5	VCC	Y2	AD[49]	AA21	NC
M15	VCC	P12	GND	T9	GND	V6	AD[40]	Y3	NC	AA22	NC
M16	GND	P13	GND	T10	I/O	V7	AD[36]	Y4	NC	AB1	NC
M17	ACLK/I	P14	GND	T11	GND	V8	FLOAT	Y5	AD[41]	AB2	NC
M18	ACLK/I	P15	GND	T12	I/O	V9	I/O	Y6	AD[37]	AB3	TDI
M19	NC	P16	GND	T13	I/O	V10	I/O	Y7	AD[38]	AB4	AD[43]
M20	GCLK/I (USER CLK)	P17	I/O	T14	I/O	V11	VCCIO	Y8	AD[34]	AB5	AD[46]
M21	GCLK/I	P18	I/O	T15	I/O	V12	I/O	Y9	FLOAT	AB6	AD[42]
M22	I/O	P19	I/O	T16	GND	V13	I/O	Y10	I/O	AB7	AD[33]
N1	AD[8]	P20	I/O	T17	I/O	V14	I/O	Y11	I/O	AB8	AD[32]
N2	NC	P21	I/O	T18	I/O	V15	I/O	Y12	I/O	AB9	VCCIO
N3	AD[7]	P22	I/O	T19	NC	V16	I/O	Y13	I/O	AB10	I/O
N4	AD[5]	R1	CBEN[7]	T20	I/O	V17	VCC	Y14	I/O	AB11	I/O
N5	VCC	R2	NC	T21	I/O	V18	I/O	Y15	I/O	AB12	I/O
N6	REQ64N	R3	CBEN[5]	T22	I/O	V19	I/O	Y16	I/O	AB13	I/O
N7	VCC	R4	NC	U1	AD[61]	V20	I/O	Y17	I/O	AB14	I/O
N8	GND	R5	AD[63]	U2	AD[58]	V21	I/O	Y18	I/O	AB15	I/O
N9	GND	R6	PAR64	U3	AD[53]	V22	I/O	Y19	I/O	AB16	I/O
N10	GND	R7	NC	U4	NC	W1	AD[54]	Y20	NC	AB17	I/O
N11	GND	R8	GND	U5	AD[57]	W2	AD[51]	Y21	I/O	AB18	I/O
N12	GND	R9	VCC	U6	GND	W3	AD[50]	Y22	I/O	AB19	TRSTB
N13	GND	R10	I/O	U7	VCC	W4	NC	AA1	NC	AB20	I/O
N14	GND	R11	NC	U8	VCC	W5	NC	AA2	NC	AB21	NC
N15	GND	R12	GND	U9	I/O	W6	AD[44]	AA3	AD[45]	AB22	NC
N16	I/O	R13	I/O	U10	I/O	W7	NC	AA4	AD[39]		
N17	I/O	R14	VCC	U11	I/O	W8	NC	AA5	AD[35]		

Ordering Information



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Revision History

Revision	Date	Comments
A	Sept 1999	First release.
B	March 2001	Updated electrical specs.
C	Dec 2001	Re-formatted and re-organized for better clarity.
D	Jan 2002	Updated 484 pin table & added ordering info.
E	August 2003	Updated Delay Factor information in Operating Range table.
F	November 2003	Jason Lew and Kathleen Murchek Updated 484 pinout table.
G	November 2003	Bernhard Andretzky and Kathleen Murchek Updated format and edited document.

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