

M61110FP/GP

Coil-less VIF/SIF

REJ03F0021-0200Z

Rev.2.0

Mar.12.2004

Description

M61110FP is a semiconductor integrated circuit consisting of VIF/SIF signal processing for CTVs and VCRs. M61110FP provides low cost and high performance system with the coil-less AFT

Feature

- Coil-less AFT
- PLL FM demodulation for Audio. No external parts and adjustment. (Target S/N=70dB)
- The PLL-SPLIT system provides good sound sensitivity and reduces buzz.
- Video output is 2.2Vp-p through EQ AMP
- Easy to add Buzz cancel
- Hi speed IF AGC
- Built-in QIF AGC
- Improve over modulation characteristics and Vcc ripple rejection
- Open collector RF AGC output (5-9V available).

Application

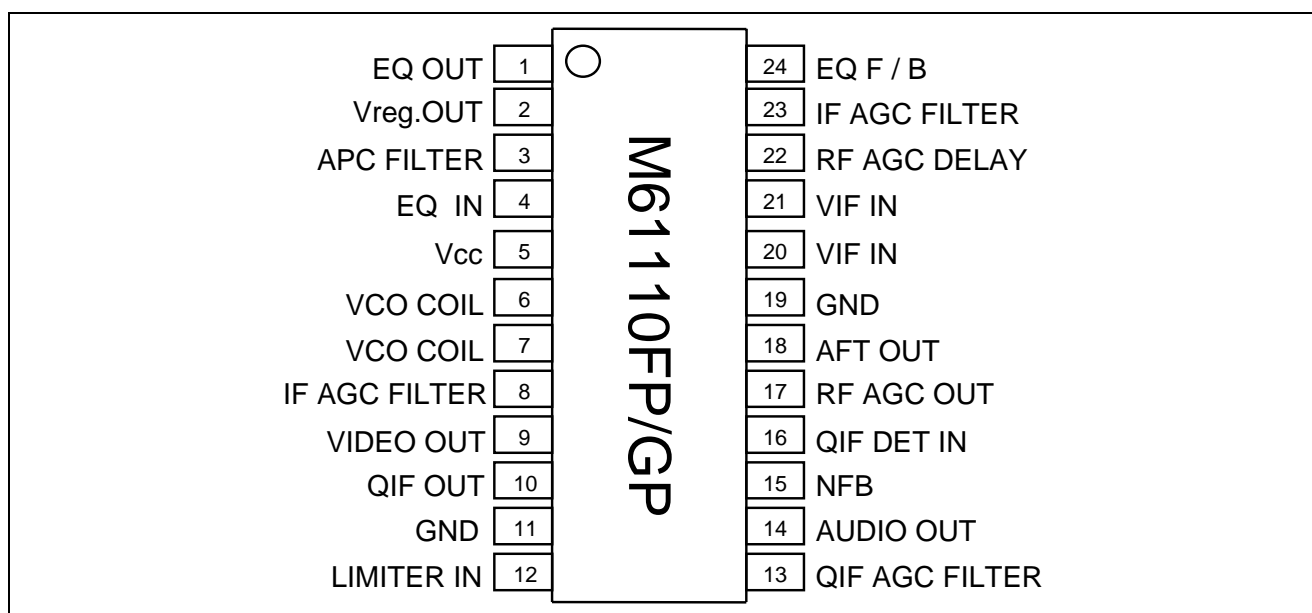
TV set, VCR tuners.

Recommended Operating Condition (Ta = 25°C, unless otherwise noted)

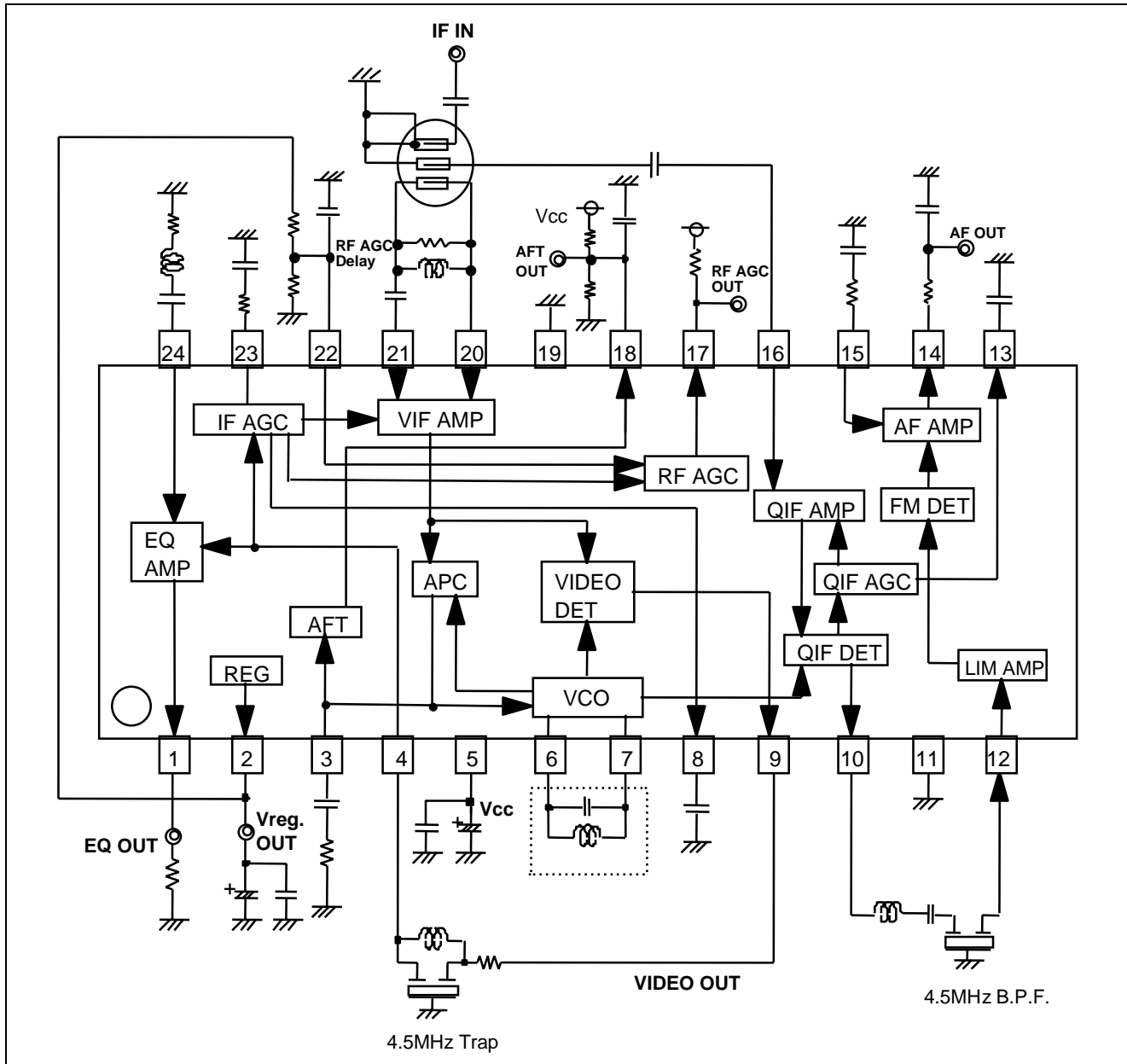
Supply Voltage Range (Vcc).....4.75 to 5.25 V

Rated Supply Voltage (Vcc).....5.0 V

Pin configuration

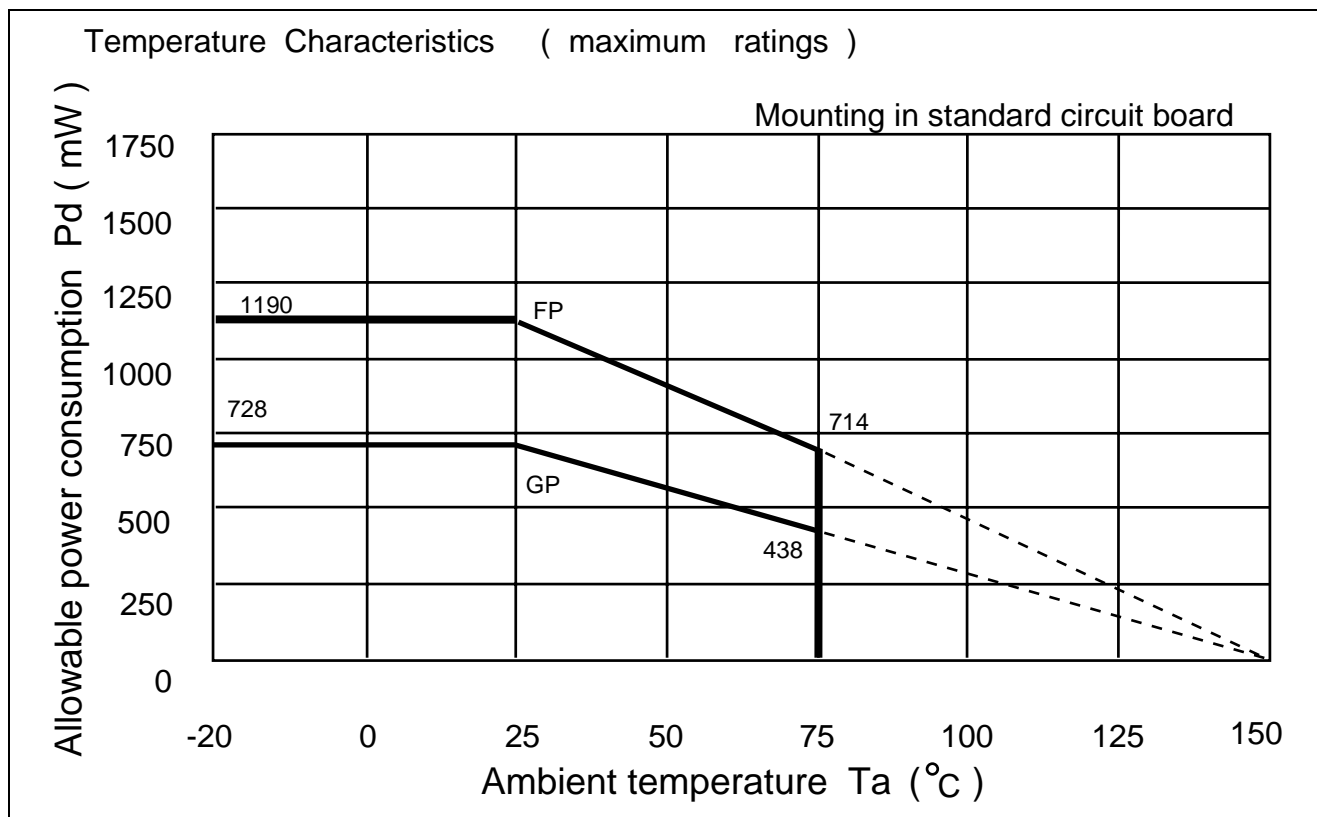


Block diagram and peripheral circuit



Absolute maximum ratings ($T_a = 25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	V_{cc}	6.0	V	
Power Consumption	P_d	1190(FP), 728(GP)	mW	
Operating Temperature	T_{opr}	-20 to +75	$^{\circ}\text{C}$	
Storage Temperature	T_{stg}	-40 to +150	$^{\circ}\text{C}$	



Electrical Characteristics (Vcc=5V, Ta=25°C, unless otherwise noted)

VIF Section

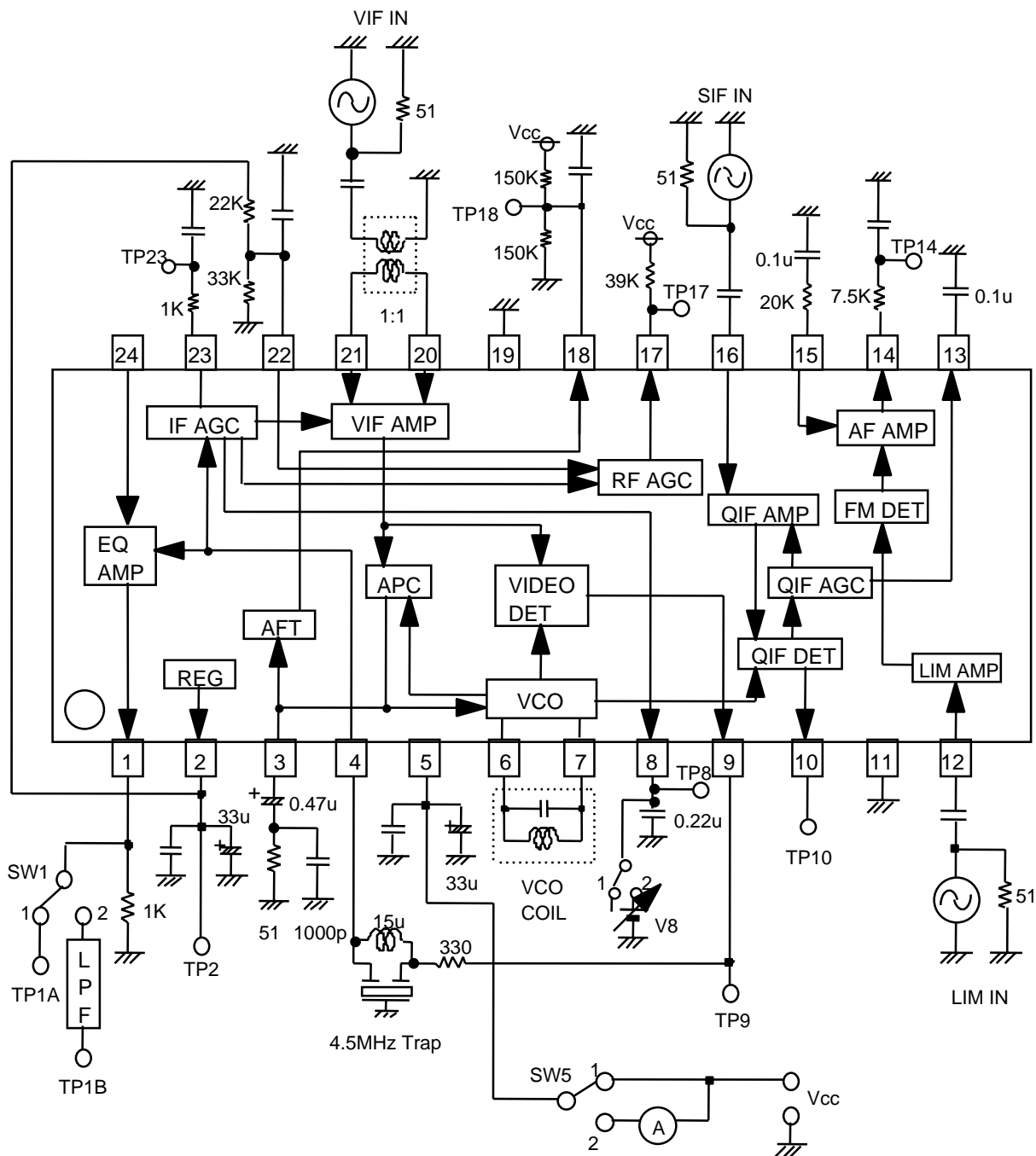
No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits			Unit	Note
								Min	Typ	Max		
1	Circuit Current	Icc	1	A	—	—	SW5 = 2	40	50	60	mA	
2	Vreg. Output Voltage	Vreg.	1	TP2	—	—		3.2	3.5	3.8	V	
3	Video Output Voltage 9	Vo det9	1	TP9	VIF IN	SG1		0.85	1.1	1.35	Vp-p	
4	Video Output Voltage 1	Vo det	1	TP1A	VIF IN	SG1		1.85	2.2	2.55	Vp-p	
5	Video S/N	Video S/N	1	TP1B	VIF IN	SG2	SW1 = 2	51	56	—	dB	1
6	Video Band Width	BW	1	TP1A	VIF IN	SG3	SW8 = 2 V8 = Variable	5.0	7.0	—	MHz	2
7	Input Sensitivity	VIN MIN	1	TP1A	VIF IN	SG4		—	48	52	dBμ	3
8	Maximum Allowable	VIN MAX	1	TP1A	VIF IN	SG5		104	110	—	dBμ	4
9	AGC Control Range Input	GR	—	—	—	—		55	62	—	dB	5
10	IF AGC Voltage 1	V8	1	TP8	VIF IN	SG6		2.8	3.1	3.4	V	
11	IF AGC Voltage 2	V23	1	TP23	VIF IN	SG6		2.8	3.1	3.4	V	
12	Maximum RF AGC	V17H	1	TP17	VIF IN	SG6		4.5	4.9	—	V	
13	Minimum RF AGC	V17L	1	TP17	VIF IN	SG7		—	0.1	0.5	V	
14	RF AGC Delay Point	V17	1	TP17	VIF IN	SG8		86	89	92	dBμ	6
15	Capture Range U	CR-U	1	TP1A	VIF IN	SG9		1.0	1.5	—	MHz	7
16	Capture Range L	CR-L	1	TP1A	VIF IN	SG9		1.1	1.6	—	MHz	8
17	Capture Range T	CR-T	—	—	—	—		2.3	3.1	—	MHz	9
18	AFT Sensitivity	μ	1	TP18	VIF IN	SG10		22	32	44	mV/kHz	10
19	AFT Minimum Voltage	V18H	1	TP18	VIF IN	SG10		4.4	4.8	—	V	10
20	AFT Maximum Voltage	V18L	1	TP18	VIF IN	SG10		—	0.1	0.5	V	10
21	AFT defeat	AFT def	1	TP18	VIF IN	—		2.2	2.5	2.8	V	
22	Inter Modulation	IM	1	TP1A	VIF IN	SG11	SW8 = 2 V8 = Variable	35	40	—	dB	11
23	Differential Gain	DG	1	TP1A	VIF IN	SG12		—	2	5	%	
24	Differential Phase	DP	1	TP1A	VIF IN	SG12		—	2	5	deg	

Electrical Characteristics ($V_{CC}=5V$, $T_a=25^{\circ}C$, unless otherwise noted)

SIF Section

No.	Parameter	Symbol	Test Circuit	Test Point	Input Point	Input SG	Measurement switches set to position 1 unless otherwise noted	Limits			Unit	Note
								Min	Typ	Max		
25	QIF det OUT1	QIF1	1	TP10	VIF IN	SG2		94	100	106	dB μ	
					QIF IN	SG13						
26	QIF det OUT2	QIF2	1	TP10	VIF IN	SG2		94	100	106	dB μ	
					QIF IN	SG14						
27	AF Output	VoAF	1	TP14	SIF IN	SG16		400	600	880	mVrms	
28	AF Output Distortion	THD AF	1	TP14	SIF IN	SG16		—	0.2	0.9	%	
29	Limiting Sensitivity	LIM	1	TP14	SIF IN	SG17		—	42	55	dB μ	12
30	AM Rejection	AMR	1	TP14	SIF IN	SG18		61	68	—	dB	13
31	AF S/N	AF S/N	1	TP14	SIF IN	SG19		63	70	—	dB	14

Measurement Circuit Diagram



* All the capacitors are 0.01uF, unless otherwise noted.

* The Measurement Circuit 1 is Mitsubishi standard evaluation fixture.

Input Signal**SG 50 Ω Termination**

1	f0 = 45.75MHz AM 20kHz 77.8% 90dB μ
2	f0 = 45.75MHz 90dB μ CW
3	f1 = 45.75MHz 90dB μ CW f2 = Frequency Variable 70dB μ } CW Mixed Signal
4	f0 = 45.75MHz AM 20kHz 77.8% Level Variable
5	f0 = 45.75MHz AM 20kHz 14.0% Level Variable
6	f0 = 45.75MHz 80dB μ CW
7	f0 = 45.75MHz 110dB μ CW
8	f0 = 45.75MHz Level Variable CW
9	f0 = Frequency Variable AM 20kHz 77.8% 90dB μ
10	f0 = Frequency Variable 90dB μ CW
11	f1 = 45.75MHz 90dB μ CW f2 = 42.17MHz 80dB μ CW } Mixed Signal f3 = 41.25MHz 80dB μ CW
12	f0 = 45.75MHz 87.5% TV modulation 10stair-steps waveform Sync Tip Level 90dB μ
13	f1 = 41.25MHz 95dB μ CW
14	f1 = 41.25MHz 75dB μ CW
15	f1 = 45.75MHz 90dB μ CW f2 = 41.25MHz 70dB μ CW } Mixed Signal
16	f0 = 4.5MHz 90dB μ FM 400Hz +/-25kHzdev
17	f0 = 4.5MHz Level Variable FM 400Hz +/-25kHzdev
18	f0 = 4.5MHz 90dB μ AM 400Hz 30%
19	f0 = 4.5MHz 90dB μ CW
20	f0 = 4.5MHz Level Variable CW

Notes

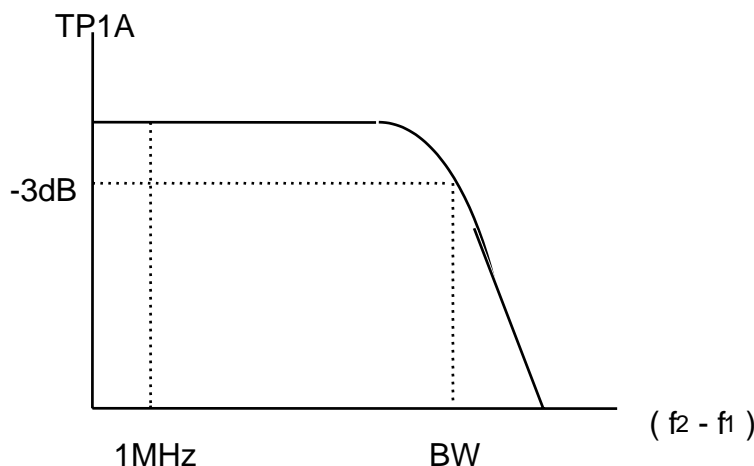
1. Video S/N

Input SG2 to VIF IN and measure the video out (Pin 1) noise in r.m.s. at TP1B through a 5MHz (−3dB) L.P.F.

$$S/N = 20 \log \left(\frac{0.7 \times V_{o \text{ det}}}{\text{NOISE}} \right) \text{ [dB]}$$

2. Video Band Width : BW

1. Measure the 1MHz component level of Video output TP1A with a spectrum analyzer when SG3 ($f_2 = 44.75\text{MHz}$) is input to VIF IN. At that time, measure the voltage at TP8 with SW8, set to position 2, and then fix V8 at that voltage.
2. Reduce f_2 and measure the value of $(f_2 - f_1)$ when the $(f_2 - f_1)$ component level reaches −3dB from the 1MHz component level as shown below.



3. Input Sensitivity : VIN MIN

Input SG4 ($V_i = 90\text{dB}\mu$) to VIF IN, and then gradually reduce V_i and measure the input level when the 20kHz component of Video output TP1A reaches −3dB from $V_{o \text{ det}}$ level.

4. Maximum Allowable Input : VIN MAX

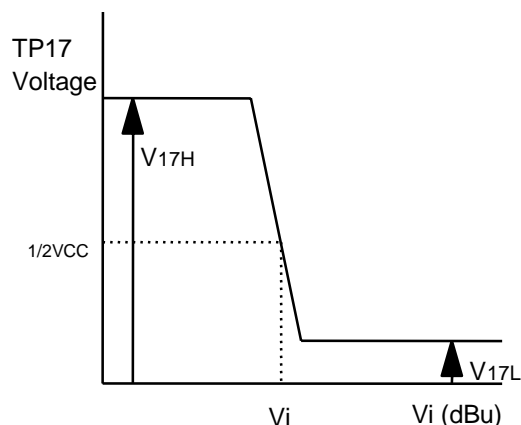
1. Input SG5 ($V_i = 90\text{dB}\mu$) to VIF IN, and measure the level of the 20kHz component of Video output.
2. Gradually increase the V_i of SG and measure the input level when the output reaches −3dB.

5. AGC Control Range: GR

$$GR = VIN \text{ MAX} - VIN \text{ MIN [dB]}$$

6. RF AGC Operating Voltage: V17

Input SG8 to VIF IN and gradually reduce V_i and then measure the input level when RF AGC output TP17 reaches $1/2V_{CC}$, as shown below.


7. Capture range: CR-U

1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
2. And decrease the frequency of SG9 and measure the frequency f_U when the VCO is locked.

$$CR-U = f_U - 45.75 \text{ [MHz]}$$

8. Capture range: CR-L

1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
2. And increase the frequency of SG9 and measure the frequency f_L when the VCO is locked.

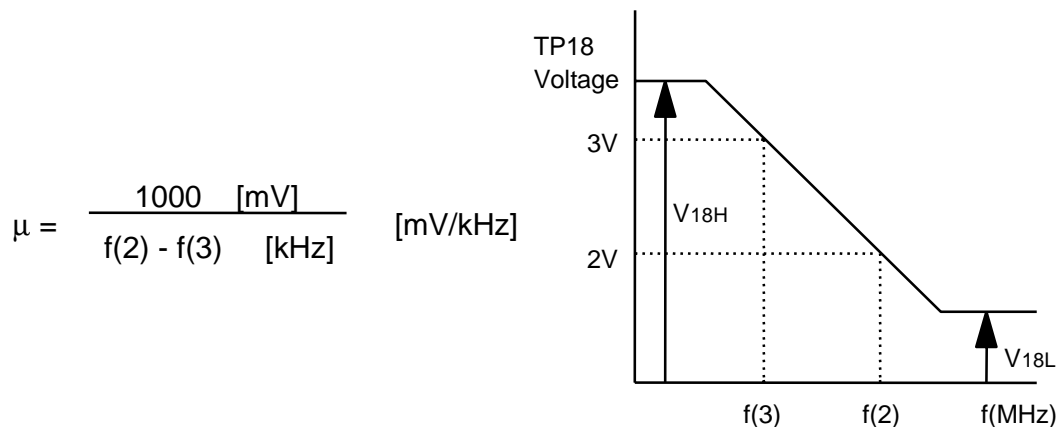
$$CR-L = 45.75 - f_L \text{ [MHz]}$$

9. Capture range: CR-T

$$CR-T = CR-U + CR-L \text{ [MHz]}$$

10. AFT sensitivity : μ , Maximum AFT voltage : V18H , Minimum AFT voltage : V18L

1. Input SG10 to VIF IN, and set the frequency of SG10 so that the voltage of AFT output TP18 is 3[V] . This frequency is named $f(3)$.
2. Set the frequency of SG10 so that the AFT output voltage is 2[V]. This frequency is named $f(2)$.
3. IN the graph shown below, maximum and minimum DC voltage are V 18H and V18L , respectively.



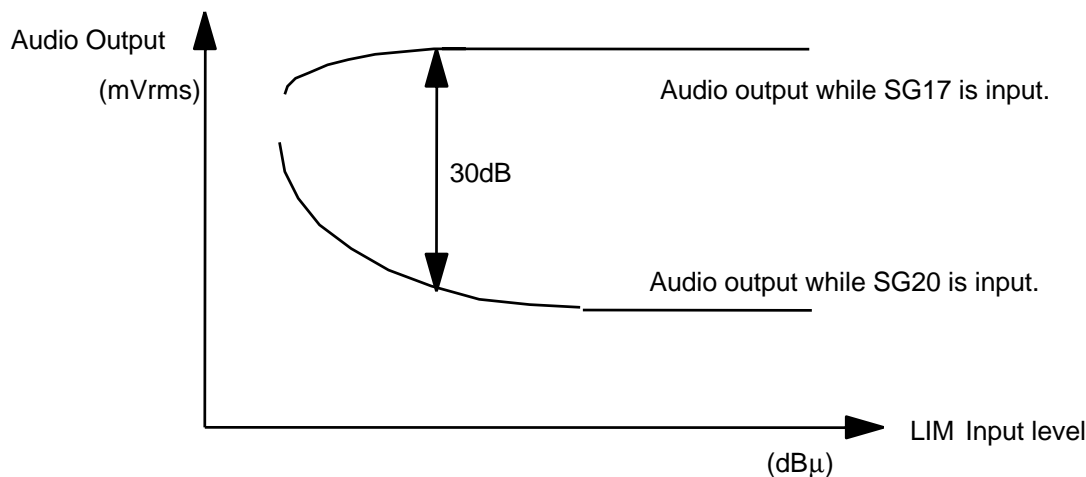
11. Inter modulation: IM

1. Input SG11 to VIF IN, and measure video output TP9 with an oscilloscope.
2. Adjust AGC filter voltage V8 so that the minimum DC level of the output waveform is 1.5V.
3. At that time, measure TP1A with a spectrum analyzer .

The inter modulation is defined as a difference between 0.92MHz and 3.58 MHz frequency components.

12. Limiting Sensitivity: LIM

1. Input SG17 to LIM IN, and measure the 400Hz component level of AF output TP14.
2. Input SG20 to LIM IN, and measure the noise level of AF output TP14 .
3. The input limiting sensitivity is defined as the input level when the difference between each 400Hz components of audio output (TP14) is 30dB, as shown below.


13. AM Rejection: AMR

1. Input SG18 to LIM IN, and measure the output level of Audio output (TP14).
This level is named VAM.
2. AMR is;

$$AMR = 20\log \left(\frac{VoAF \text{ (mVrms)}}{VAM \text{ (mVrms)}} \right) \quad [dB]$$

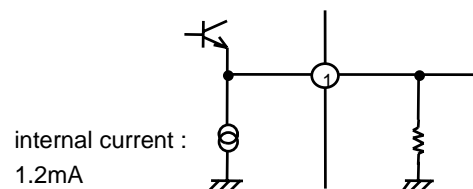
14. AF S/N: AF S/N

1. Input SG19 to LIM IN, and measure the output noise level of Audio output (TP14).
This level is named VN.
2. S/N is;

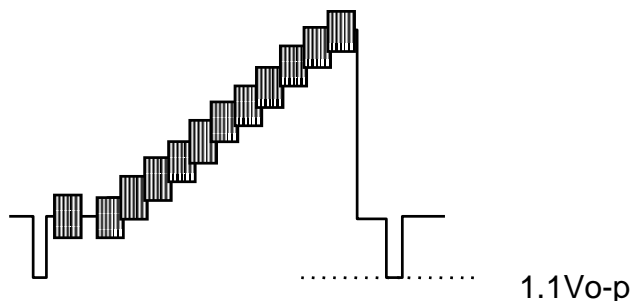
$$S/N = 20\log \left(\frac{VoAF \text{ (mVrms)}}{VN \text{ (mVrms)}} \right) \quad [dB]$$

Pin peripheral circuit explanation

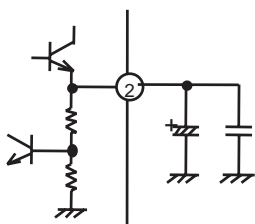
*Pin 1 (EQ OUT)



EQ output amplitude is positive 2.2Vp-p in case of 87.5% video modulation.



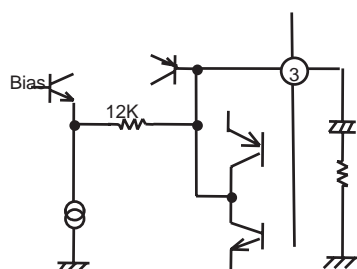
*Pin 2 (Vreg.OUT)



It is a regulated 3.5V output which has current drive capability of approximately 1mA.

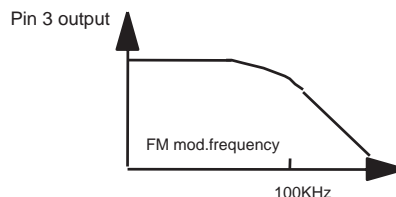
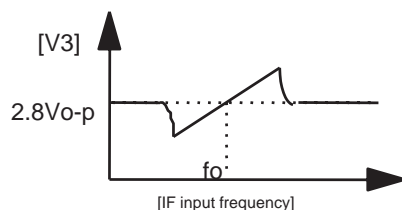
In the locked state, the cut-off frequency of the filter is adjusted effectively by an external resistor so that it will be in the range of around 30 to 200kHz.

*Pin3 (APC FILTER)

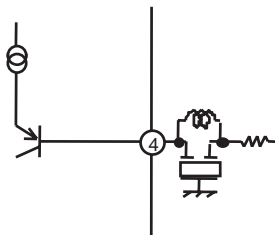


In case the cut-off frequency is lower, the pull-in speed becomes slow. On the other hand, a higher cut-off frequency widens the pull-in range and band width, which results in a degradation in the S/N ratio.

So, in the actual TV system design, the appropriate constant should be chosen for getting desirable performance considering above conditions.

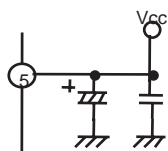


*PIN 4 (EQ IN)



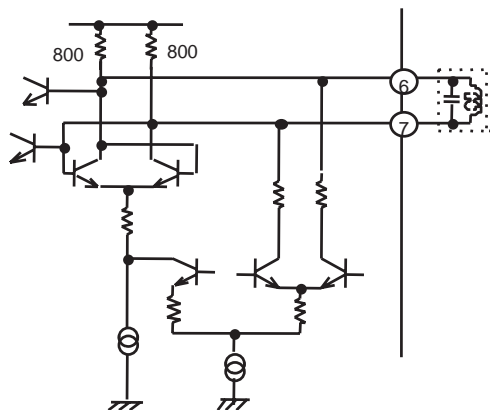
The input is open base.
If DC information is not input to pin9, IF AGC dose not work normally.
Please pay attention.

*PIN 5 (Vcc)



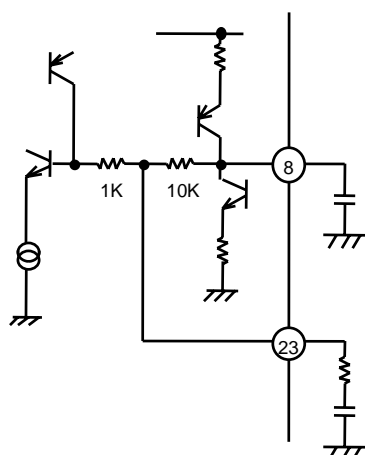
It is Vcc pin. (only one Vcc pin in this IC)

*PIN 6, PIN 7 (VCO COIL)

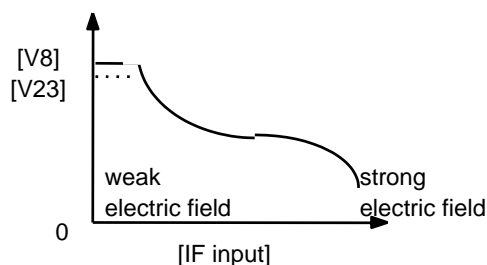


Connecting a tuning coil and capacitor to these pins enables an oscillation. The oscillation frequency is tuned in 'fo'. In the actual adjustment, the coil is tuned so that the AFT voltage reaches to $V_{cc}/2$ with 'fo' as an input.
The printed pattern around these pins should be designed carefully to prevent an pull-in error of VCO, caused by the leakage interference from the large signal level oscillator to adjacent pins. The interconnection should be designed as short as possible.
In case the printed pattern has the interference problem, a capacitor of about 1pF is connected between pin6 or pin7 and GND so as to cancel the interference and keep enough pull-in range even in a low input level.

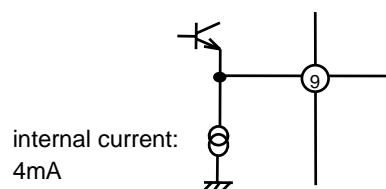
*PIN 8, PIN 23 (IF AGC FILTER)



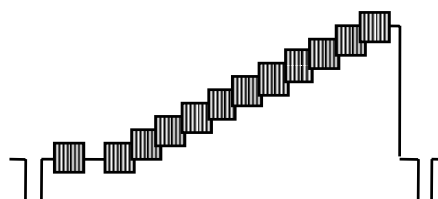
2-pins filter characteristics are available by utilizing the dynamic AGC circuit .
And AGC speed can be changed, if pin23 on the external resistor is variable.



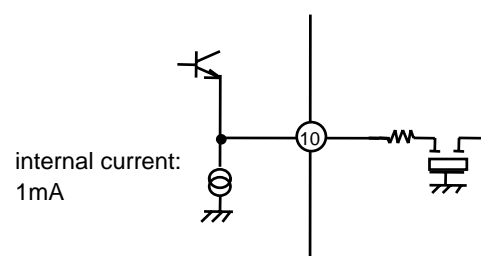
*PIN 9 (VIDEO OUT)



Video output amplitude is positive 1.1Vp-p in case of 87.5% video modulation.



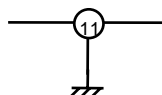
*PIN 10 (QIF OUT)



In the split carrier system, the carrier signal to SIF is provided from pin10 through the emitter follower.

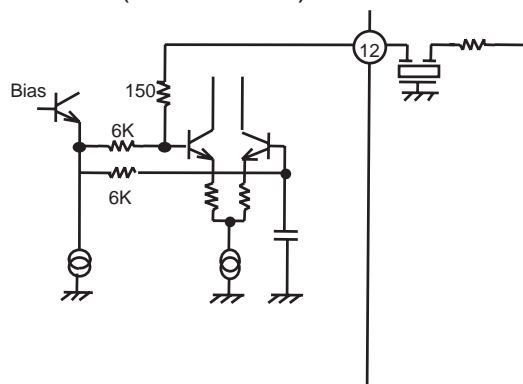
And please open this pin, when it is used in the inter carrier system.

*PIN 11 (GND)



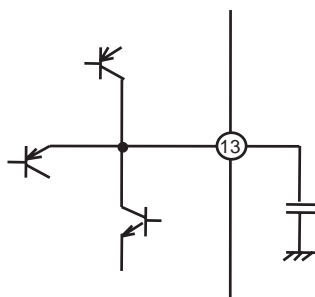
This is GND of the SIF part .

*PIN 12 (LIMITER IN)



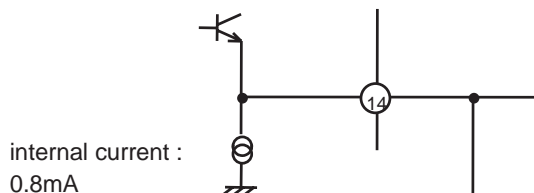
The input impedance is 6.15KΩ.

*PIN 13 (QIF AGC FILTER)



AGC speed can be changed by this pin's external capacity.

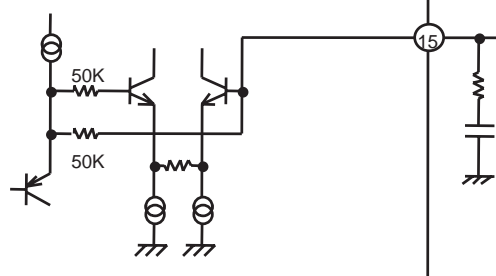
*PIN 14 (AUDIO OUT)



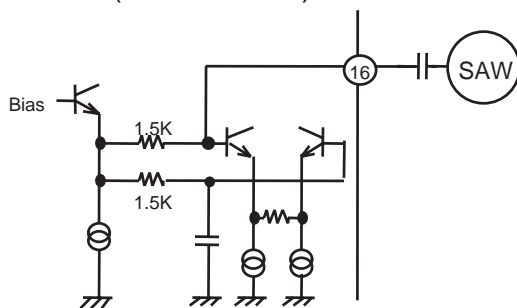
The FM detector can respond to SIF signals without an adjustment and external components by adopting the PLL technique. The capacitor between pin14 and pin15, which fixes the de-emphasis characteristics, can be determined considering the combination of an equivalent resistance of the IC and this capacitor itself.

Frequency response of audio output is decided with external capacitor value of pin15. And audio output level can be made it small when it connected external capacitor to pin15 and resistance in series.

*PIN 15 (NFB)

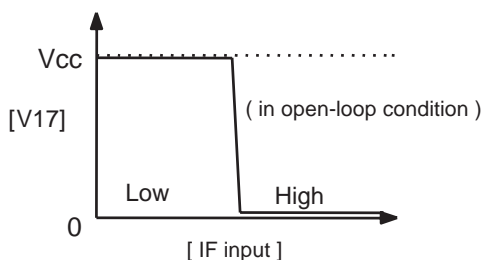
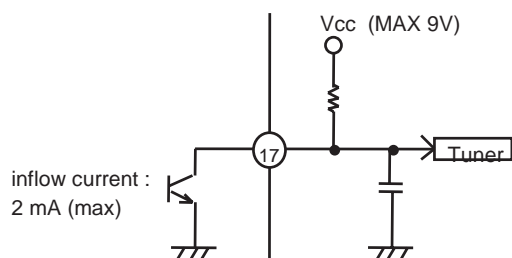


*PIN 16 (QIF DET IN)



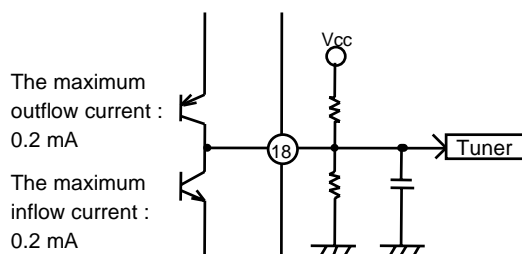
The input impedance is 1.5KΩ.

*PIN 17 (RF AGC OUT)

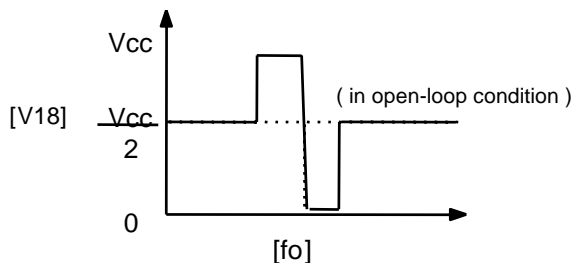


Connecting a non-polarity capacitor of 1uF between pin17 to pin22 improves AGC operating speed.
In that case, the capacitors between pin17 and pin22 to ground should be removed.
It is possible for Pin17 to connect to Vcc with 9V.

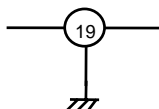
*PIN 18 (AFT OUT)



AFT output is provided by a high impedance source, the detection sensitivity can be set by an external resistor. The muting operation will be on in following two cases;
1) the APC is out of locked
2) the video output becomes small enough in a low input level.

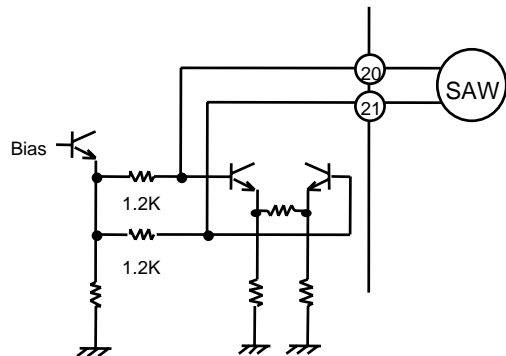


*PIN 19 (GND)



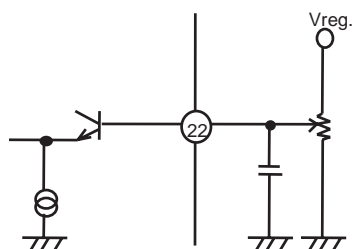
This is GND other than SIF part.

*PIN 20, PIN 21 (VIF IN)



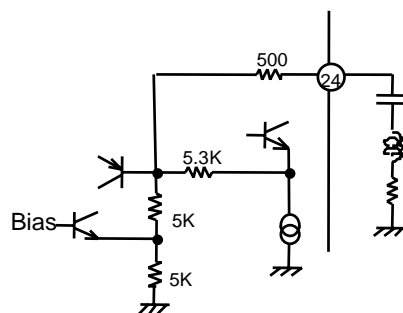
It should be designed carefully for impedance matching with the SAW filter.

*PIN 22 (RF AGC DELAY)

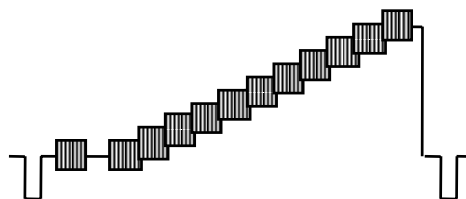


The applied voltage to the pin22 is for changing RF AGC delay point .

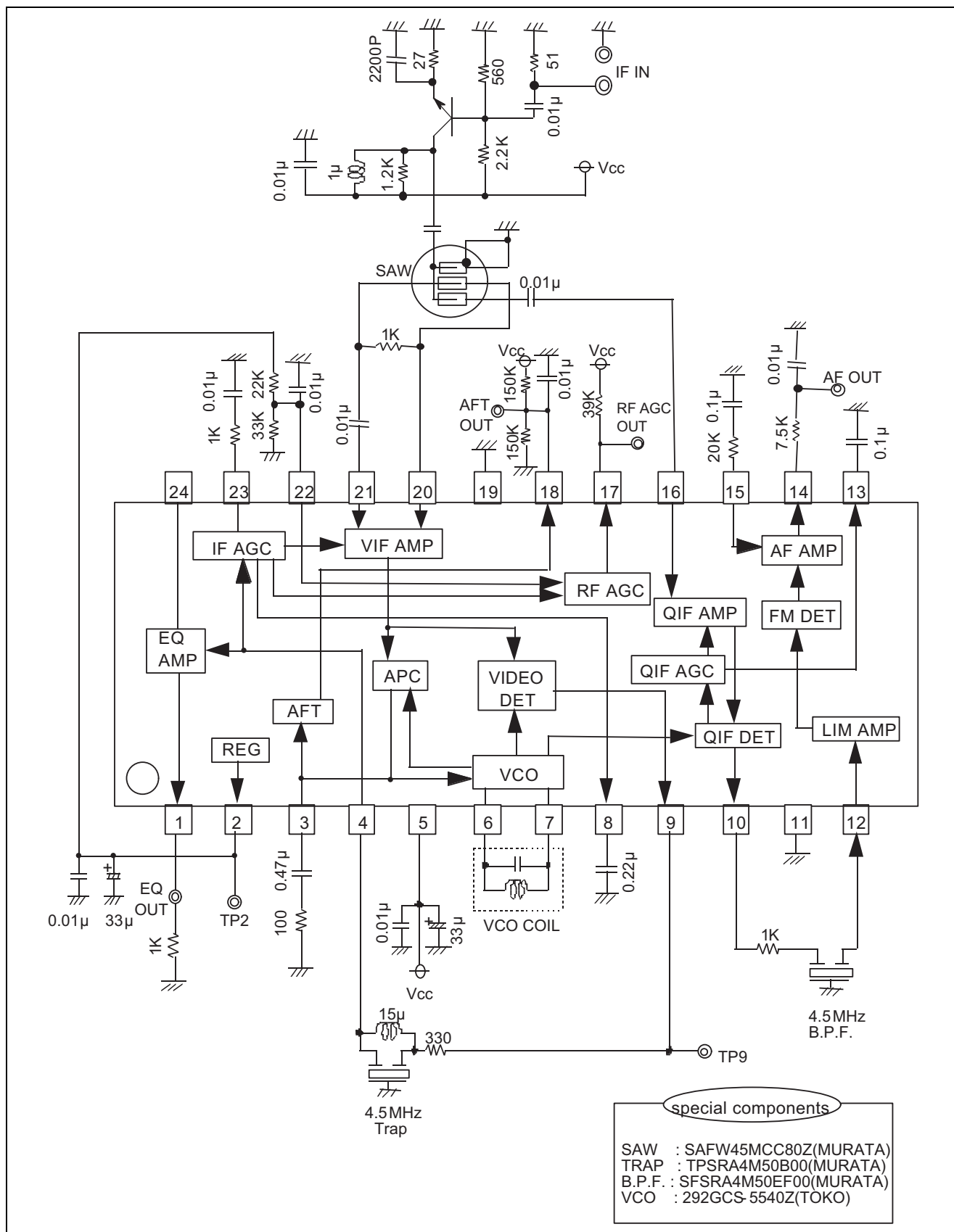
*PIN 24 (EQ F/B)



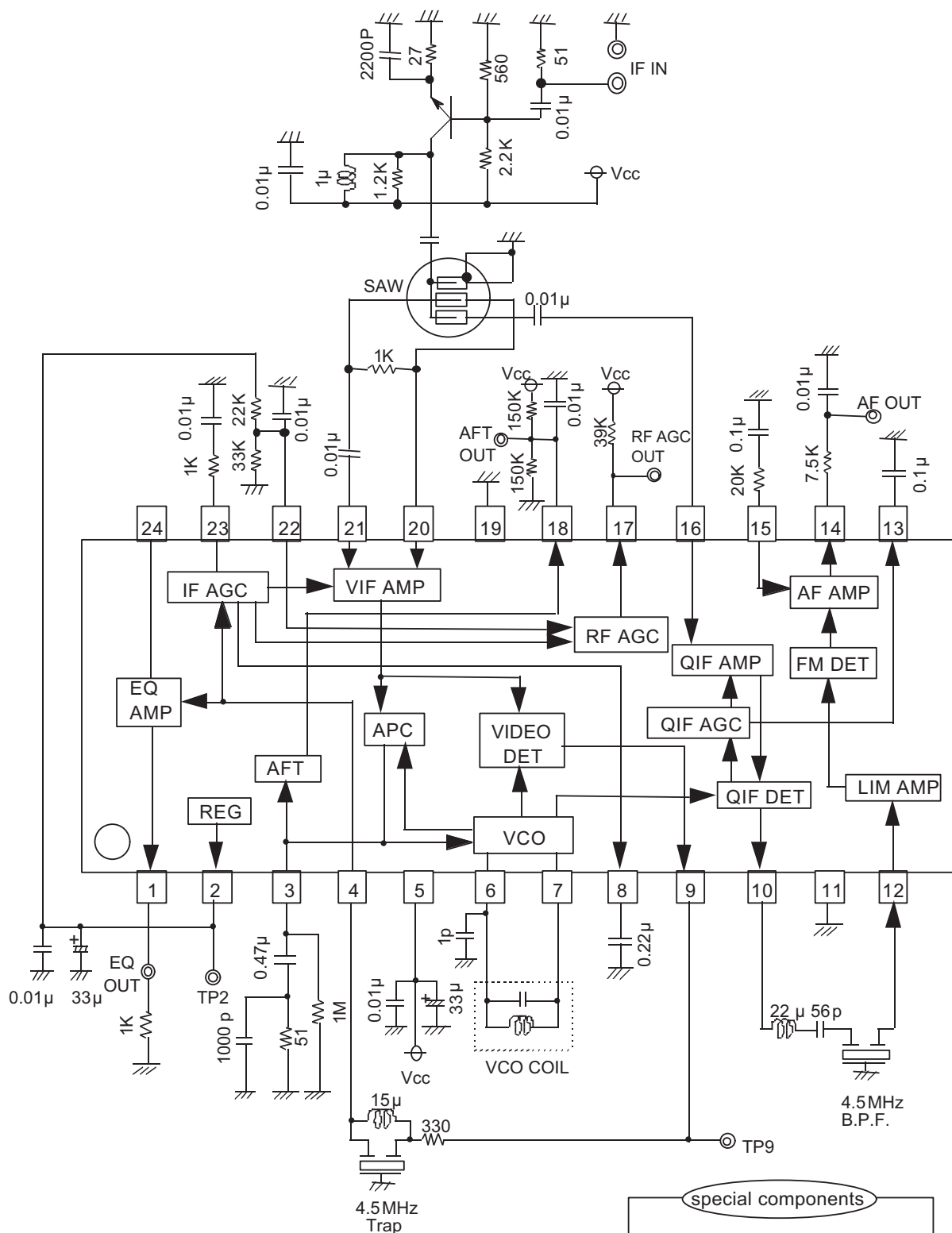
Both the external coil and capacitor determine the frequency response of EQ output .
The series connected resistor is for damping.



Application Example 1



Application Example 2



special components

SAW : SAFW45MCC80Z(MURATA)
 TRAP : TPSRA4M50B00(MURATA)
 B.P.F. : SFSRA4M50EF00(MURATA)
 VCO : 292GCS-5540Z(TOKO)

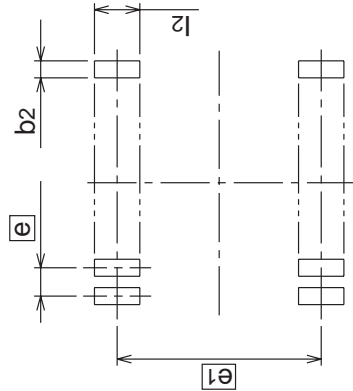
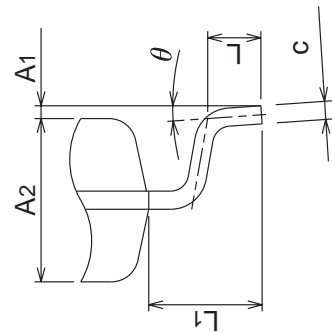
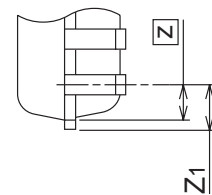
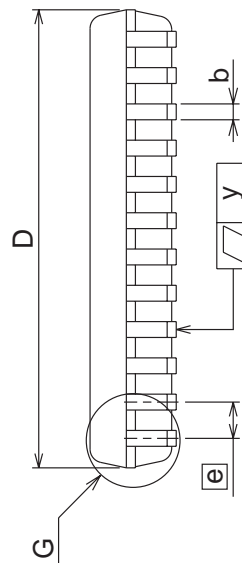
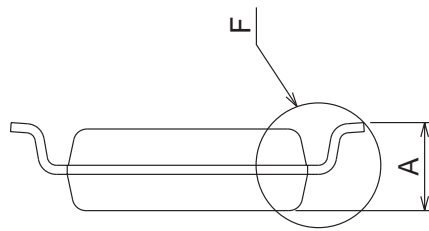
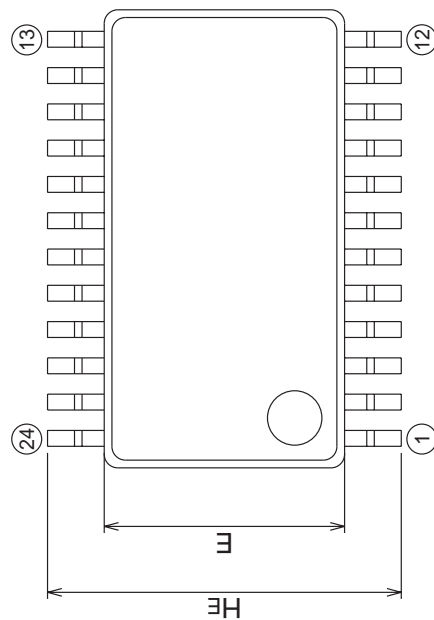
Detailed Diagram Of Package Outline

24P2Q-A

(MMP)

Plastic 24pin 300mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP24-P-300-0.80	—	0.2	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A1	0	0.1	0.2
A2	—	1.8	—
b	0.3	0.35	0.45
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	—	0.8	—
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	—	1.25	—
z	—	0.65	—
Z1	—	—	0.8
y	—	—	0.1
theta	0°	—	8°
b2	—	0.5	—
e1	—	7.62	—
l2	1.27	—	—

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001