

## CompactPCI® Backplane Interface

### Features

- Allows System Cards to be used in any Slot
- Terminates up to ten channels
- Supports hot-swap capability
- Provides a series switch in each channel
- Very low capacitance
- Industrial temperature range
- 28-pin TSSOP package

### Applications

- Redundant System CompactPCI® cards
- Hot-swap CompactPCI cards
- Industrial PCs
- Telecom/Datacom equipment
- Instrumentation
- Computer Telephony
- Real-time machine control

### Product Description

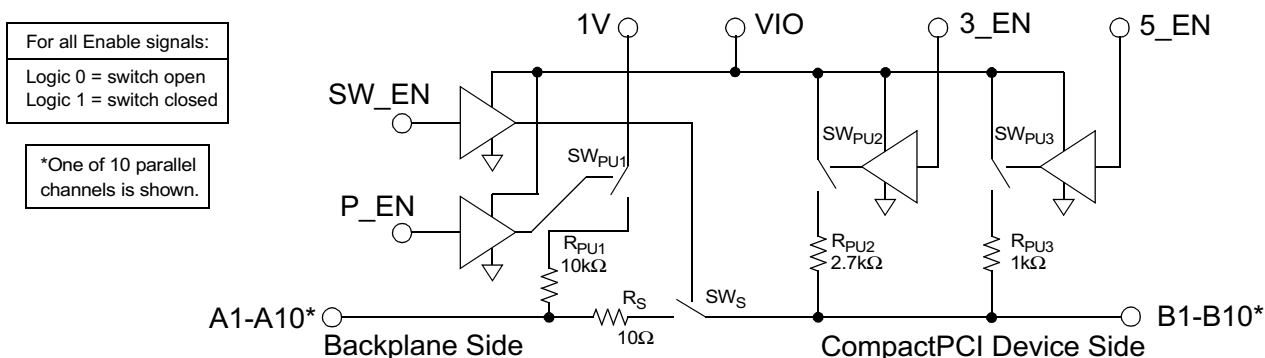
The CMCPCI102A is a 10-channel backplane interface/termination IC specifically designed for CompactPCI redundant system-slot cards. The CMCPCI102A allows CompactPCI boards to interface to the backplane and provides the versatility to use system cards in any slot (system or peripheral). Per the CompactPCI specification, the CMCPCI102A provides a  $10\Omega$  termination resistor for each channel to terminate the transmission line stub on the board. An integral series switch and associated control signal (SW\_EN) permits connection/disconnection of the channel, so that the device side of the circuit may be isolated from the backplane side.

The CompactPCI standard requires system boards to be hot-swappable. To accommodate this requirement, the CMCPCI102A features a switched  $10k\Omega$  resistor connected to the 1V Precharge Supply Voltage. If the precharge enable pin (P\_EN) is asserted, then the  $10k\Omega$  pull-up resistors are connected to precharge the circuits.

In addition, a system board requirement mandates either a  $1.0k\Omega$  pull-up resistor or a  $2.7k\Omega$  resistor connected to VIO. CompactPCI slot cards must work in either 3.3V or 5V systems, hence the need for both  $2.7k\Omega$  and  $1k\Omega$  resistors. If the 3\_EN pin is logic high, the  $2.7k\Omega$  resistor is used as the pull-up. If the 5\_EN pin is logic high, the  $1k\Omega$  resistor is used.

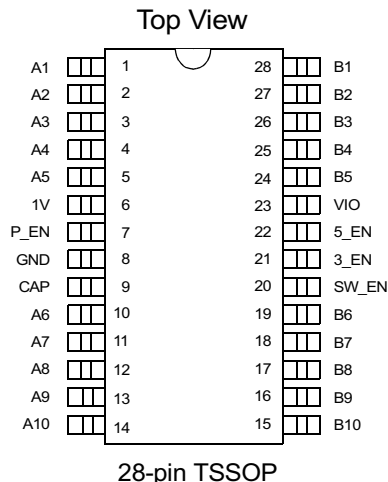
The CMCPCI102A integrates all these functions in a low-profile 28-pin TSSOP package.

### Simplified Electrical Schematic





## PACKAGE / PINOUT DIAGRAM



Note: This drawing is not to scale.

## PIN DESCRIPTIONS

PIN(S)	NAME	DESCRIPTION
1-5	A1 - A5	The backplane-side input signals for channels 1 through 5, respectively.
10-14	A6 - A10	The backplane-side input signals for channels 6 through 10, respectively.
24-28	B1 - B5	The device-side connection for channels 1 through 5, respectively.
15-19	B6 - B10	The device-side connection for channels 6 through 10, respectively.
6	1V	A precharge supply voltage input for all channels. This voltage can be less than or equal to VIO.
7	P_EN	The precharge enable input which controls the precharge pull-up resistors. When this active high control signal is set to '1', the precharge of all channels is enabled.
8	GND	The ground voltage reference for the CMCPCI102A.
9	CAP	A capacitor must be placed from this pin to GND. The recommended value is 0.01μF, 16V. NOTE: This pin is sensitive to ESD.
20	SW_EN	The series switch enable input. When this active high control signal is set to '1', the series switch between the channel's backplane-side terminal and device-side terminal is closed. When this signal is cleared to '0', the switch is open.
21	3_EN	The enable signal for the device-side channel pull-up mechanism when 3.3V is the supply voltage. When this active high control signal is set to '1', the 2.7kΩ pull-up resistor which pulls up the channel to the supply rail is engaged.
22	5_EN	The enable signal for the device-side channel pull-up mechanism when 5V is the supply voltage. When this active high control signal is set to '1', the 1kΩ pull-up resistor which pulls up the channel to the supply rail is engaged.
23	VIO	The positive supply voltage for the CMCPCI102A. Either 3.3V or 5V may be used.



## Ordering Information

PART NUMBERING INFORMATION			
Pins	Package	Ordering Part Number <sup>1</sup>	Part Marking
28	TSSOP	CMCPCI102AT	CMCPCI102ATS

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

## Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
VIO (supply voltage)	-0.5 to +6	V
Pin Voltages		
1V, P_EN, 3_EN, 5_EN, SW_EN	-0.5 to (VIO+0.5)	V
A1-A10	-0.5 to (VIO+0.5)	V
B1-B10	-0.5 to (VIO+0.5)	V
ESD Withstand Voltage		
Human Body Model, MIL-STD-883D, Method 3015 (Notes 1, 2)	$\pm 2$	kV
'CAP' Pin Only	$\pm 500$	V
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range (Ambient)	-40 to +85	°C
DC Power per Resistor	62	mW
Package Power Rating	1	W

Note 1: ESD is applied to input / output pins with respect to GND, one at a time; unused pins are left open.

Note 2: This parameter guaranteed by design.

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
VIO (supply voltage)	3 to 5.5	V
Pin Voltages		
P_EN, 3_EN, 5_EN, SW_EN	0 to VIO	V
A1-A10	0 to VIO	V
B1-B10	0 to VIO	V
Ambient Operating Temperature Range	-40 to +85	°C



## Specifications (Cont'd)

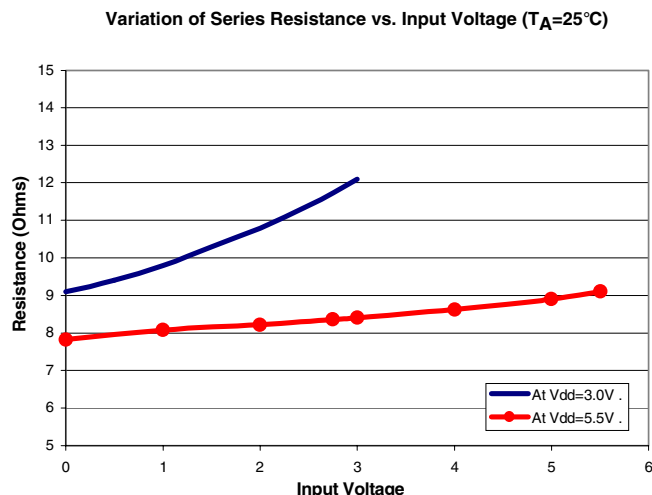
ELECTRICAL OPERATING CHARACTERISTICS						
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R <sub>S1</sub>	Series Resistance through R <sub>S</sub>	A to B; switch SW <sub>S</sub> closed; T <sub>A</sub> =25°C	5	10	15	Ω
R <sub>S2</sub>	Series Resistance through R <sub>S</sub>	A to B; switch SW <sub>S</sub> open; T <sub>A</sub> =25°C	1			MΩ
R <sub>PU1</sub>	Resistance of R <sub>PU1</sub> pull-up	T <sub>A</sub> =25°C	9.5		18	kΩ
TOL <sub>RPU2</sub> TOL <sub>RPU3</sub>	Resistance Tolerance (R <sub>PU2</sub> and R <sub>PU3</sub> )	T <sub>A</sub> =25°C			±5	%
TCR <sub>PU</sub>	Temperature Coefficient of Resistance (R <sub>PU1</sub> , R <sub>PU2</sub> , R <sub>PU3</sub> )			-100		ppm/°C
C <sub>1</sub>	Capacitance on backplane side (A side) of series resistor R <sub>S</sub>	Measured @ 66MHz, 0VDC, SW_EN=0V; Note 1		1.9		pF
C <sub>2</sub>	Capacitance on device side (B side) of series resistor R <sub>S</sub> and series switch SW <sub>S</sub>	Measured @ 66MHz, 0VDC, VIO=5V, 5_EN=5V SW_EN=0V; Note 1		4.2		pF
V <sub>IL</sub>	Logic Low Input Voltage to P_EN, 3_EN, 5_EN, SW_EN		-0.5		[VIO] x 0.3	V
V <sub>IH</sub>	Logic High Input Voltage to P_EN, 3_EN, 5_EN, SW_EN		[VIO] x 0.7		[VIO] + 0.5	V
I <sub>LEAK</sub>	Leakage Current into P_EN, 3_EN, 5_EN, SW_EN	GND < V < VIO		±1	±10	μA
I <sub>GND</sub>	Supply Current for internal circuits (measured at GND pin)			0.25	1	mA
t <sub>PLH</sub>	Switch SW <sub>S</sub> closure delay from the low-to-high transition of SW_EN	Note 1, 'CAP' pin capaci- tor=0.01μF		8		ms
t <sub>PHL</sub>	Switch SW <sub>S</sub> delay from the high-to- low transition of SW_EN	Note 1, 'CAP' pin capaci- tor=0.01μF		150		μs
t <sub>PPU</sub>	Propagation delay for pull-up switches SW <sub>PU1</sub> , SW <sub>PU2</sub> , and SW <sub>PU3</sub> , all transitions	Note 1			10	ns

Note 1: This parameter is guaranteed by design; it is not tested 100%.

## Performance Information

### Resistance Variation with Input Voltage

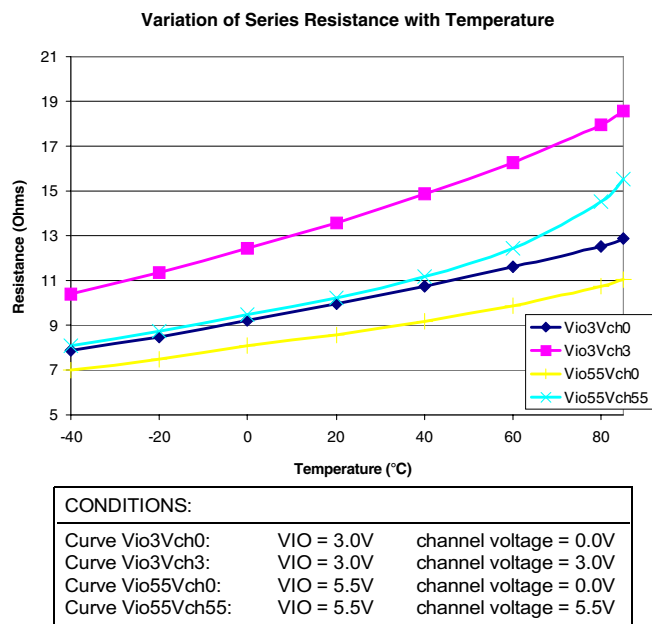
The series resistance  $R_S$  varies with input voltage and supply voltage, as shown in Figure 1.



**Figure 1. Resistance Variation vs. Input Voltage**

### Resistance Variation with Temperature

The series resistance  $R_S$  also varies with temperature, as shown in Figure 2.



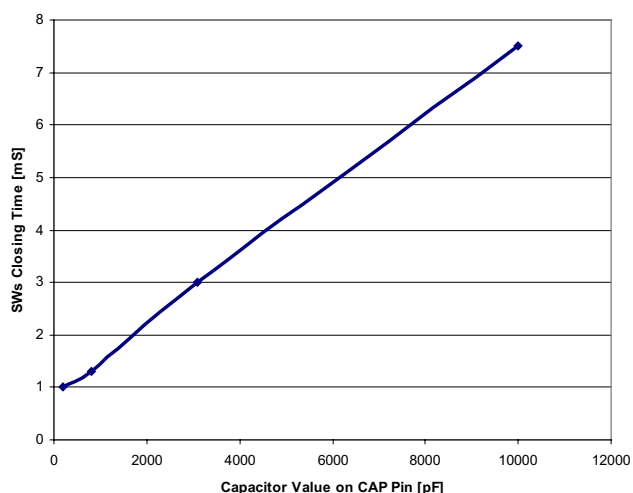
**Figure 2. Resistance Variation vs. Temperature**

### CAP Pin Capacitance

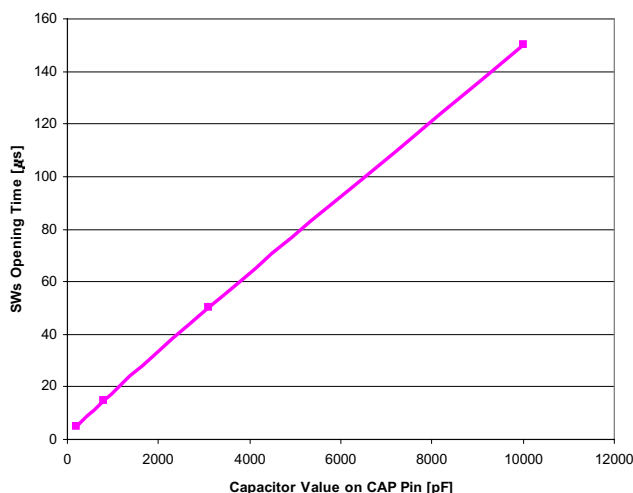
Some external capacitance is necessary to prevent the voltage on the CAP pin from falling during sustained data transfers through the device. This ensures that the logic 1 level does not degrade.

The time required to open and close the series switch, SWs, varies according to how much capacitance is present on the CAP pin.

The minimum usable value is 200pF, placed close to the pins. A 0.01uF, 16V capacitor is recommended. See Figure 3 and Figure 4 for variation of switch on/off times vs. capacitance.



**Figure 3. Switch ON Time vs. CAP Capacitor Value**



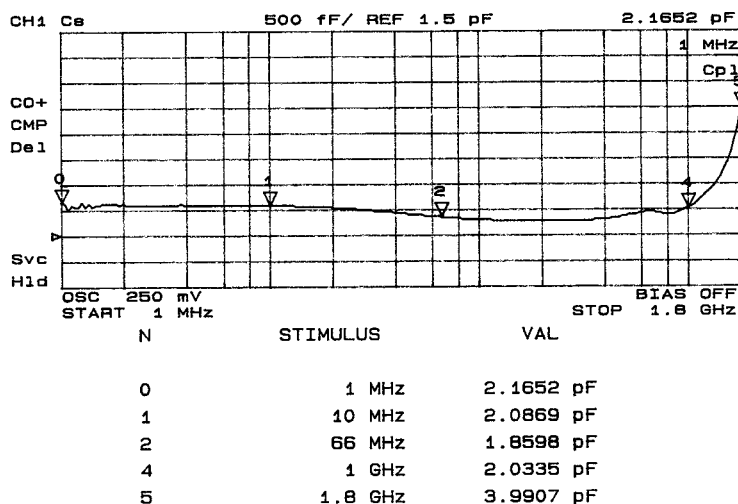
**Figure 4. Switch OFF Time vs. CAP Capacitor Value**

## Performance Information (cont'd)

### Capacitance Variation with Frequency

The A-side and B-side capacitances,  $C_1$  and  $C_2$ , will vary with frequency. The backplane capacitance,  $C_1$ , is very linear over a wide frequency range. [Figure 5](#)

shows a plot of input line A3 (pin 3), measured with SW\_EN=0V and VIO=5V.

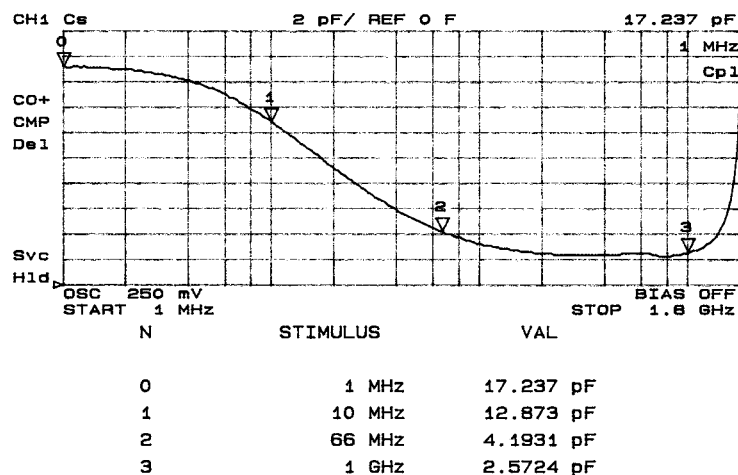


**Figure 5.  $C_1$  (Backplane-side) Capacitance Variation vs. Frequency**

The CompactPCI device side of the CMCPCI102A has a fairly low capacitance ( $C_2$ ) at 66MHz, but it is higher at lower frequencies.

[Figure 6](#) shows a plot of output line B3 (pin 26), measured at the worst-case (for capacitance) conditions of SW\_EN=0V, 5\_EN=0V, 3\_EN=0V and VIO=5V.

The increased capacitance at low frequencies is due to the parasitic capacitance of the switches connected to the pull-up resistors. At high frequencies, this parasitic capacitance is decoupled by the pull-up resistors.



**Figure 6.  $C_2$  (Device-side) Capacitance Variation vs. Frequency**

## Application Information

### Board Layout Recommendations

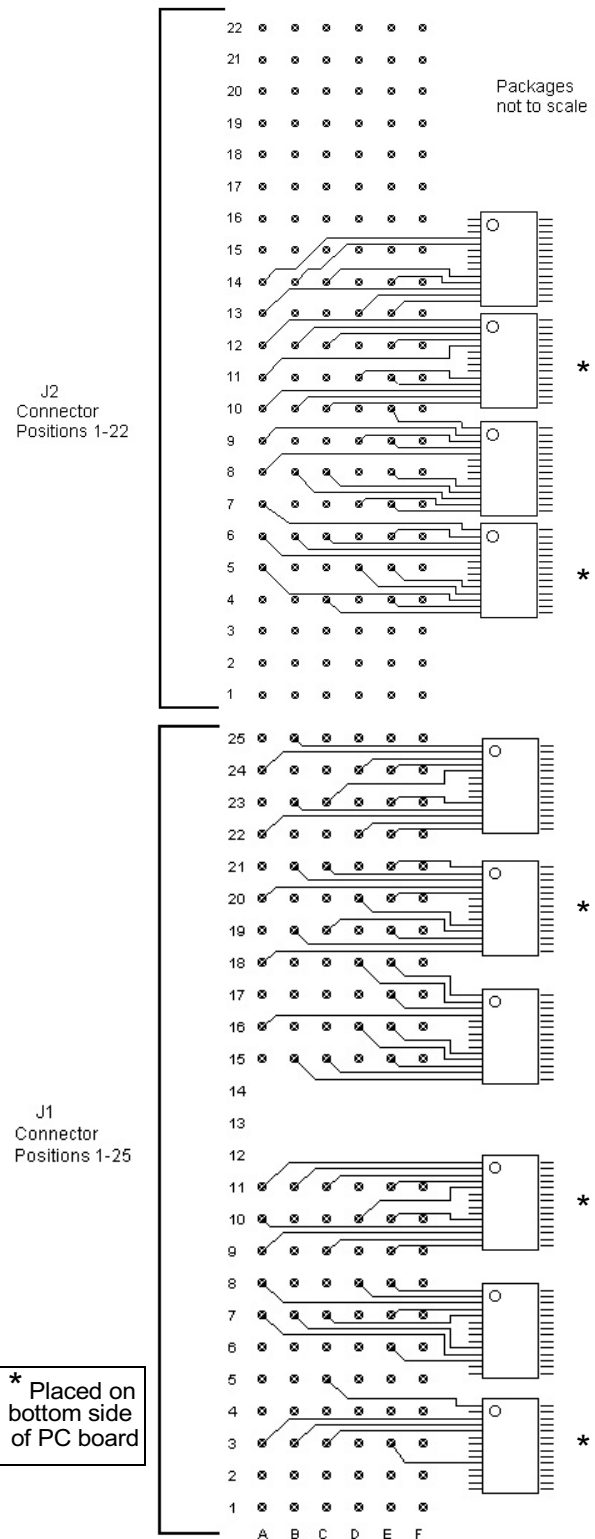
The CMCPCI102A devices should be located on the board as close as possible to the CompactPCI connector. Whether a signal is terminated or not depends upon application, as shown in the following table:

SIGNAL(S)	SYSTEM SLOT BOARDS	
	32-Bit	64-Bit
AD0-AD31	terminate	terminate
C/BE0#-C/BE3#	terminate	terminate
PAR	terminate	terminate
FRAME#	terminate	terminate
IRDY#	terminate	terminate
TRDY#	terminate	terminate
STOP#	terminate	terminate
LOCK#	terminate	terminate
DEVSEL#	terminate	terminate
PERR#	terminate	terminate
SERR#	terminate	terminate
RST#	terminate	terminate
REQ64#	terminate	terminate
ACK64#	terminate	terminate
INTA#, INTB#, INTC#, INTD# (if used)	terminate	terminate
AD32-AD63	N/A	terminate
C/BE4#-C/BE7	N/A	terminate
PAR64	N/A	terminate

Figure 7 shows a 64-bit system board connection between the CMCPCI102A termination and the CompactPCI 5-row connector (2 mm pitch) labeled A to E (row F is Ground). The System slot should have signal lengths not exceeding 63.5 mm (2.5 inches). To minimize trace length, it is recommended that the CMCPCI102As be placed on alternate sides of the PC board. The configuration shown illustrates a fully-terminated 64-bit board utilizing 10 CMCPCI102A devices. Some applications (e.g. 32-bit boards) do not require all lines to be terminated, per the above table.

The CMCPCI102A resistors have a very low TCR (typically -100ppm/°C) so that resistance will not fluctuate over temperature. Buffers are implemented on P\_EN, 5\_EN and 3\_EN inputs to ensure that switches turn on and off completely.

A typical system slot card may use 10 CMCPCI102A devices to replace 10 10-bit FET bus switches and 76 4-resistor packs (0805 form factor), thus providing significant reduction in both component count and assembly costs. At the same time this highly integrated solution improves reliability and manufacturing efficiency, saves board area for space-critical designs, and satisfies CompactPCI height requirements.



**Figure 7. Schematic for 64-bit System Board**



## Mechanical Details

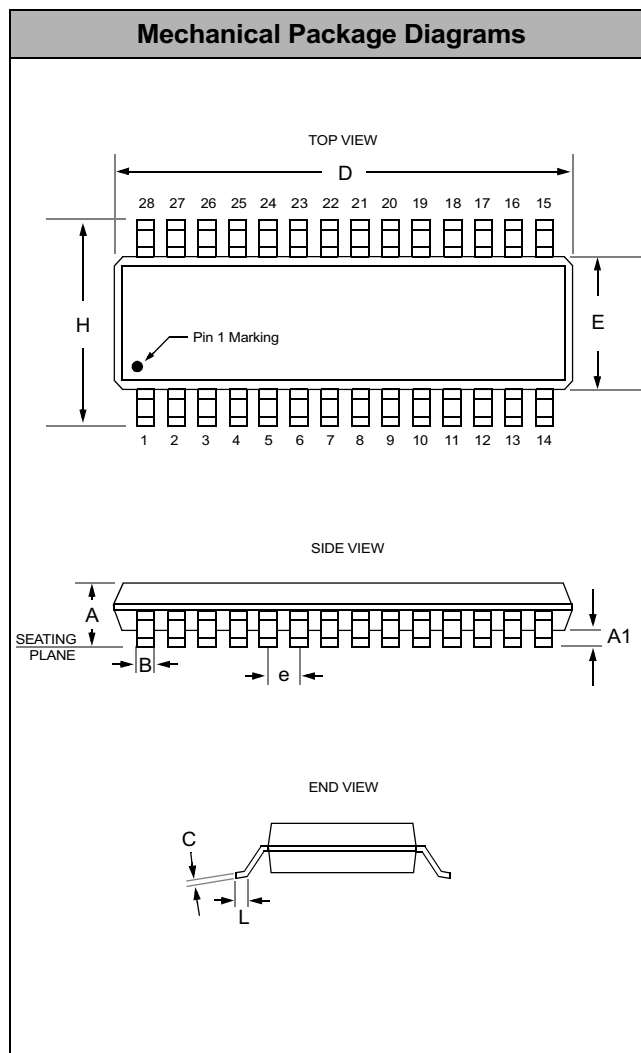
### TSSOP Mechanical Specifications

CMCPCI102A devices are packaged in 28-pin TSSOP packages. Dimensions are presented below.

For complete information on the TSSOP-28 package, see the California Micro Devices TSSOP Package Information document.

PACKAGE DIMENSIONS				
Package	TSSOP			
Pins	28			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	—	1.10	—	0.0433
A1	0.05	0.15	0.002	0.006
B	0.19	0.30	0.0075	0.0118
C	0.09	0.20	0.0035	0.0079
D	9.60	9.80	0.378	0.386
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.0256 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
# per tube	50 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: millimeters				

\* This is an approximate number which may vary.



Package Dimensions for TSSOP-28