24-bit 192kHz Stereo Audio DAC

DESCRIPTION

The AV2636 is a high performance, low power stereo audio digital to analog converter (DAC). It is designed for high performance audio applications such as CD player, DVD player, home theater systems, digital TVs and set top boxes. Based on the state of the art multi-bit Δ−Σ modulator, it also includes the digital interpolation filters, digital volume control, digital de-emphasis and analog low pass filters. It has no linearity drift due to time and temperature. It also has high tolerance to clock jitter.

The device has a serial audio interface that accepts 16/18/20/24 digital data in I^2S, Right-justified or DSP mode. It can work at auto-detect mode or programmable mode with a two-wire serial command interface. Audio sample rates from 8kHz to 192kHz are supported.

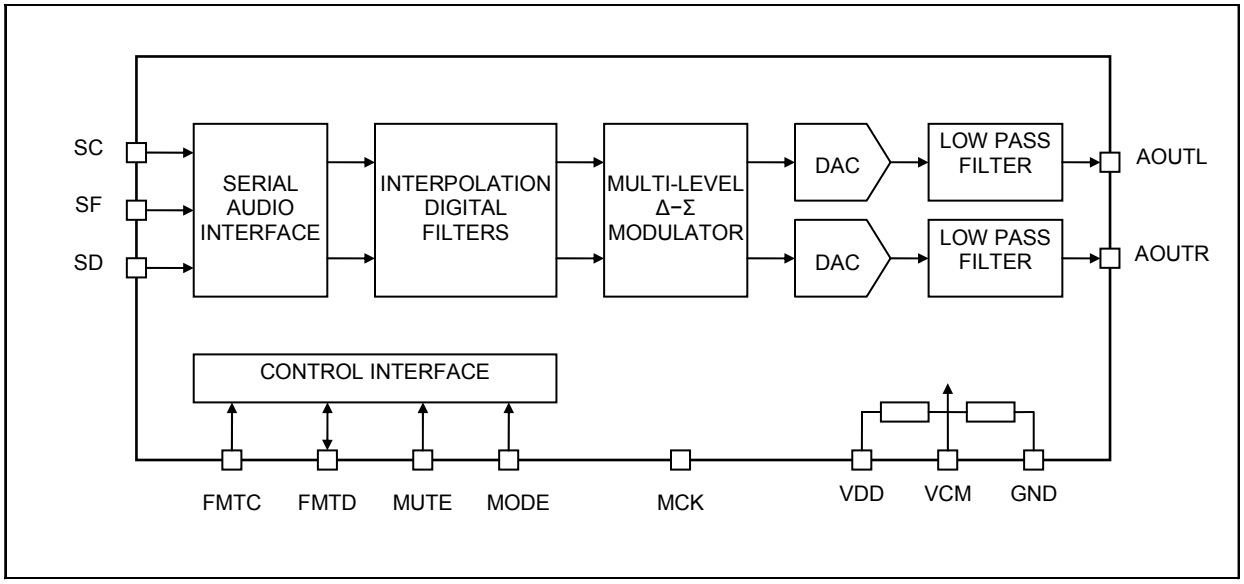
FEATURES

- SNR: 102 dB
- THD+N: -90 dB
- Input Sample rate: 8kHz – 192kHz
- Input data resolution: 16/18/20/24 bits
- Digital De-Emphasis for 32k/44.1k/48kHz
- Digital Volume Control
- Mute Control
- Single Power Supply 2.2V – 3.6V
- Low Clock Jitter Sensitivity
- Small 14-pin SOIC Package

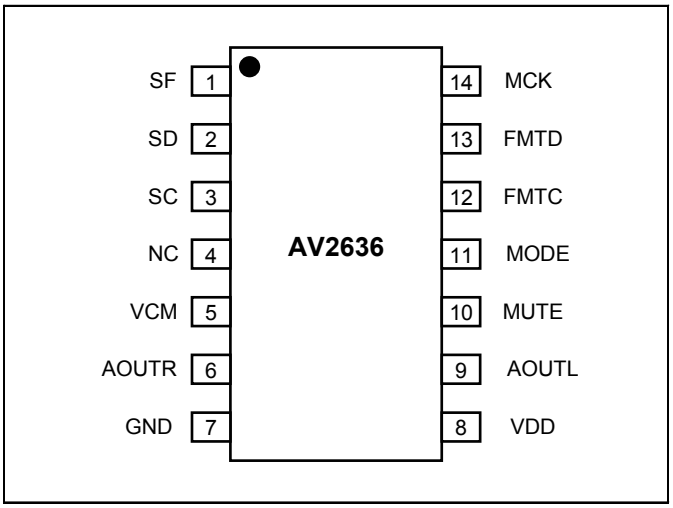
APPLICATIONS

- DVD/CD Player
- Home Theatre Systems
- Digital TV and Set-Top Boxes
- Electronic Music Instrument

CHIP BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Pin	Type	Description
SF	1	Digital Input	Sample rate frame clock input.
SD	2	Digital Input	Audio data input. It can be 16/18/20/24 bit in 2's complement format.
SC	3	Digital Input	Serial audio data bit clock input.
(NC)	4	-	No Connection
VCM	5	Analog Output	Common mode voltage output. Connect to 10uF cap in parallel with 0.1uF cap.
AOUTR	6	Analog Output	Right channel analog audio signal output.
GND	7	Supply	Ground supply. Need a solid ground plane.
VDD	8	Supply	Power supply. Need a clean power supply.
AOUTL	9	Analog Output	Left channel analog audio signal output.
MUTE	10	Digital Input	Mute control with internal pull down. High = Mute on. Low = Mute off.
MODE	11	Digital Input	Chip operation mode selection with internal pull down. High = Programmable mode. Low = Auto-detect mode.
FMTC	12	Digital Input	Dual functional pin. Its function is controlled by the MODE pin. Internal pull up. When MODE = High, FMTC = Serial clock in control interface. When MODE = Low, FMTC = De-Emphasis: On (high) / Off (low).
FMTD	13	Digital I/O	Dual functional pin. Its function is controlled by the MODE pin. Internal pull up. Needs an external 4.7kΩ to VDD. When MODE = High, FMTD = Serial data in control interface. When MODE = Low, FMTD = Data input format select: High = 16-24 bit I2S or 16 bit DSP 'early' Low = 16 bit right justified or 16 bit DSP 'late'
MCK	14	Digital Input	External master clock input. The clock frequency depends on the audio sample rate.

ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
AV2636	14 pin SOIC	-25˚C — +85˚C

ELECTROSTATIC DISCHARGE SENSITIVITY

The device of integrated circuits is manufactured on CMOS process. It can be damaged by ESD. AVS Technology recommends that the device be handled with appropriate ESD precautions. Improper handling and installation procedures can cause damage to the device.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are the limiting values of the stress. Operation beyond these limits may cause permanent damage to the device. Normal operation is not guaranteed at these limits.

Symbol	Characteristics	Min	Max	Units
VDD	Power supply voltage (Measured to GND)	-0.3	+3.6	V
Vi	Digital input voltage range	GND – 0.3	VDD + 0.3	V
Ai	Digital input forced current	-100	+100	mA
T_A	Ambient operating temperature range	-25	+125	˚C
Tstg	Storage temperature range	-65	+150	˚C
Tj	Junction temperature (Plastic package)	-65	+150	˚C
Tsol	Lead soldering temperature (10 sec., ¼” from pin)		+240	˚C
Tvsol	Vapor phase soldering (1 minute)		+220	˚C

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Typical	Max	Units
VDD	Power supply voltage	2.2	3.3	3.6	V
GND	Ground		0		V
MCK	Master clock frequency			75	MHz
T_A	Ambient operating temperature range	-25		85	˚C

ELECTRICAL CHARACTERISTICS

(Test conditions: VDD = 3.3V, GND = 0V, T_A = +25˚C, fs = 48kHz, MCK = 256fs unless otherwise stated. The measurement bandwidth is from 20Hz to 20kHz.)

PARAMETERS		SYMBOL	MIN	TYP	MAX	UNITS
DC Electrical Characteristics						
Supply current (VDD = 3.3V)		I_{DD}		10		mA
Supply current (VDD = 2.5V)		I_{DD}		7		mA
Digital I/O Levels (TTL Level)						
Digital input high level		V_{IH}	2.0			V
Digital input low level		V_{IL}			0.8	V
Digital output high level (I_{OH} = 2mA)		V_{OH}	VDD–0.2			V
Digital output low level (I_{OL} = 2mA)		V_{OL}			GND+0.2	V
Analog Characteristics						
Reference voltage		VCM		VDD/2		V
Full scale analog output level		AOUT		VDD/3.3		Vrms
Minimum resistive load		R_L	10			kΩ
Maximum capacitive load		C_L			100	pF
Output DC level				VDD/2		V
DAC Analog Output Performance (Test load R_L = 10kΩ, C_L = 10pF)						
VDD = 3.3V	SNR			102		dB
	THD+N (1kHz, 0dBFs input)			-90		dB
	Dynamic Range (1kHz, -60dBFs input)			98		dB
VDD = 2.5V	SNR			100		dB
	THD+N (1kHz, 0dBFs input)			-90		dB
	Dynamic Range (1kHz, -60dBFs input)			96		dB
Channel separation (1kHz)				-95		dB
Interchannel gain mismatch				0.1		dB
Program gain range			-∞		+6	dB

Notes:

1. SNR is measured as the ratio of output level with 1kHz full scale signal, to output level with all zero signal into the digital input. The measurement is over 20Hz to 20kHz bandwidth with a 'A-weight' filter.
2. THD is measured at the output with 1kHz full scale signal into the digital input. The measurement is over 20Hz to 20kHz bandwidth.
3. Dynamic Range is the ratio of maximum output over minimum output. It is normally measured by THD+N at the output with an input signal that is 60dB below full scale. The 60dB is then added back to the THD+N value for the final result.
4. Channel separation is also known as channel cross talk. It is measured by sending a 1kHz full scale signal into one channel and measuring the output value at the other channel.
5. All measurements are done with a 20kHz low pass filter. Fail to use the filter will result in reduced performance reading.
6. The VCM pin should be decoupled with a 10uF capacitor in parallel with a 0.1uF capacitor. Smaller value may result in reduced performance.

OPERATING MODE

The AV2636 can operate at two modes. They are auto-detect mode and programmable mode. The 'MODE' pin status (High/Low) determines which mode the device will be operated. If MODE = Low (pull to GND or not connected using internal pull down), the device will be operated at auto-detect mode. If MODE = High (pull to VDD), the device will be operated at programmable mode. The basic functions of the two modes are described as follows:

- *Auto-detect mode:* The relation between sample rate and master clock frequency is auto detected. De-emphasis and serial interface mode are determined by FMTC and FMTD pins.
- *Programmable mode:* The device operation will be set by on chip control registers that can be accessed through a two-wire command interface.

AUDIO DATA SAMPLE RATE AND MASTER CLOCK FREQUENCY

The AV2636 supports various audio data sample rate (fs) from 8kHz to 192kHz. The typical audio sample rates are 32kHz, 44.1kH, 48kHz, 96kHz and 192kHz. The master clock (MCK) can be of 64fs to 384fs depending on the operation mode. MCK is an input clock that operates the internal digital filters. Other on chip clocks are also derived from MCK.

The on-chip master clock detection circuit automatically determines the relationship of master clock frequency and audio sample rate. The counting error is set to be ±8 master clock cycles. If the error is larger than the threshold, the DAC output will be shut down and auto muted.

The master clock has to be synchronized with the serial audio data frame signal 'SF'. SF is also called left and right data frame signal. The phase difference and clock jitters can be tolerated.

Sample Rate (fs)	**Master Clock Frequency MCK (MHz)**					
	64fs	**96fs**	**128fs**	**192fs**	**256fs**	**384fs**
32 kHz	N/A	N/A	N/A	N/A	8.192	12.288
44.1 kHz	N/A	N/A	N/A	N/A	11.2896	16.9344
48 kHz	N/A	N/A	N/A	N/A	12.288	18.432
88.2 kHz	N/A	N/A	11.1896	16.9344	22.5792	33.8688
96 kHz	N/A	N/A	12.288	18.432	24.576	36.864
192 kHz	12.288	18.432	24.576	36.864	49.152*	73.728*

Note:

* Only available at programmable mode.

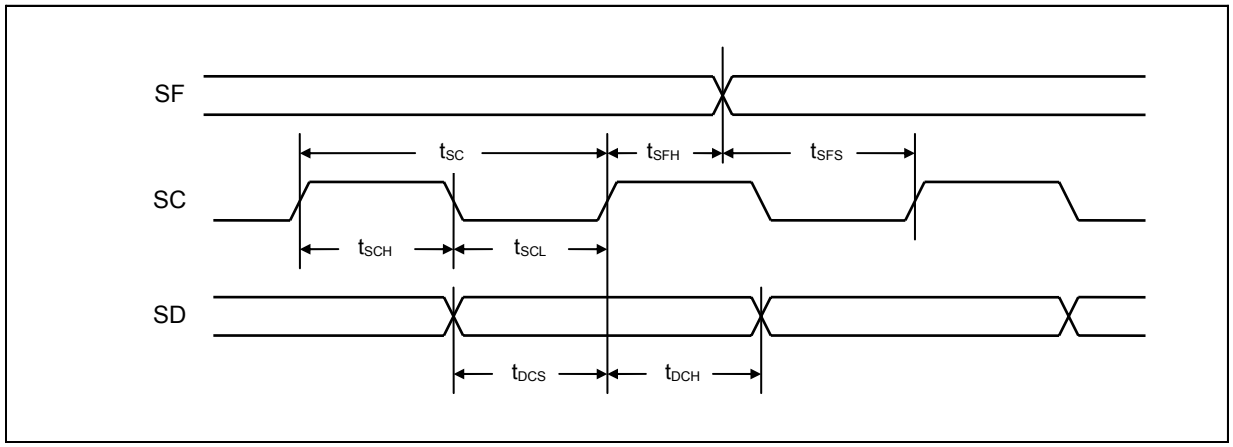
DIGITAL AUDIO DATA INTERFACE

The serial audio data is send to the device through a three-wire interface. The interface consists of three input pins that are serial clock (SC), serial data (SD) and sync-frame (SF). The sync-frame is also a left/right channel indicator. Three interface formats are supported.

- I^2S mode
- Right justified mode
- DSP mode

All formats send MSB first. The audio data is in 2's complement format. The mode selection can be either in auto-detect mode or programmable mode.

The three-wire digital audio data interface timing specification is shown at the following diagram.



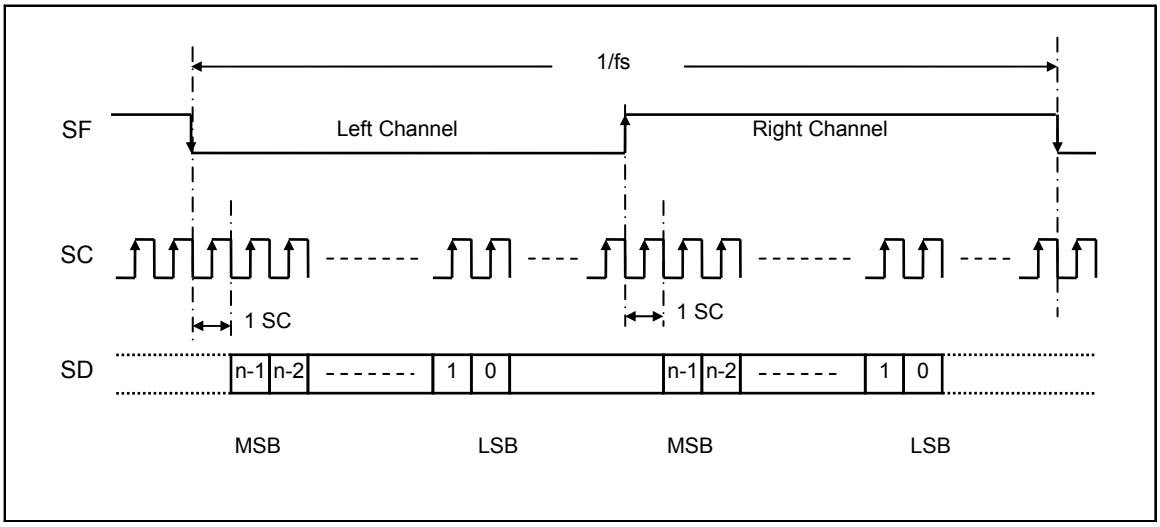
The timing characteristics are shown at the following table.

Symbol	Description	Min	Max	Units
t_{SC}	SC clock cycle time	50		ns
t_{SCH}	SC pulse width high	20		ns
t_{SCL}	SC pulse width low	20		ns
t_{DCS}	SD data setup time relative to SC rising edge	10		ns
t_{DCH}	SD data hold time relative to SC rising edge	10		ns
t_{SFH}	SF hold time relative to SC rising edge	10		ns
t_{SFS}	SF setup time relative to SC rising edge	10		ns

I^2S MODE

In I^2S mode, the serial interface accepts input data at SD pin and frame input at SF pin. The serial data is time multiplexed with the frame signal SF indicating left and right channel data. SF is low during left channel data and high during right channel data. The SF is also a timing signal for the start of each word of left and right channel.

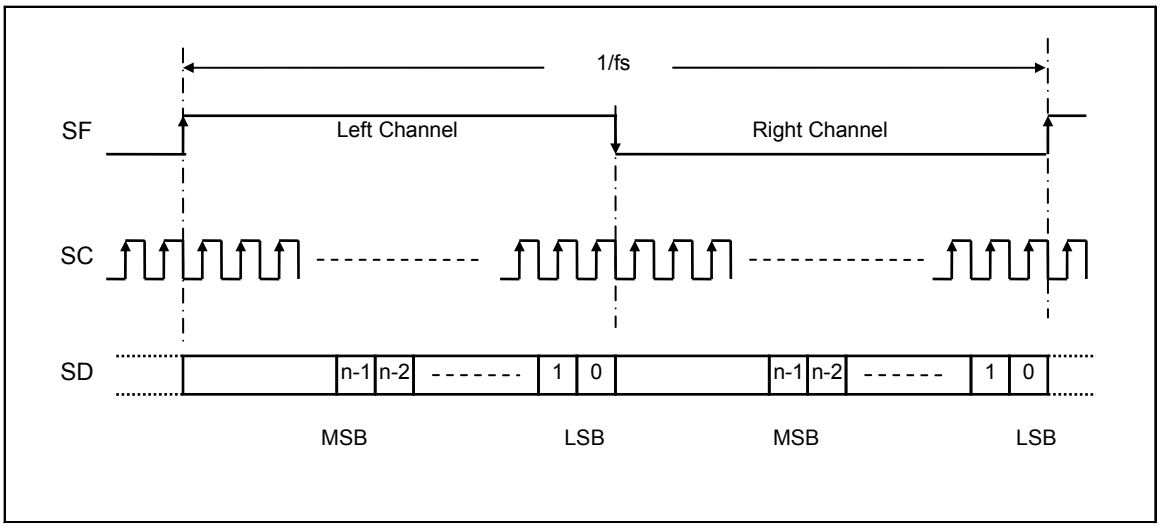
The MSB of the audio data SD is sampled on the second rising edge of SC following SF transition. Word lengths of 16/18/20/24 bits are supported.



RIGHT JUSTIFIED MODE

In right justified mode, the serial interface accepts input data at SD pin and frame input at SF pin. The serial data is time multiplexed with the frame signal SF indicating left and right channel data. SF is high during left channel data and low during right channel data. The SF is also a timing signal for the end of each word of left and right channel.

The MSB is received first and LSB is aligned with the transition of frame signal SF. Data is sampled at the rising edge of SC. Word lengths of 16/18/20/24 bits are supported.

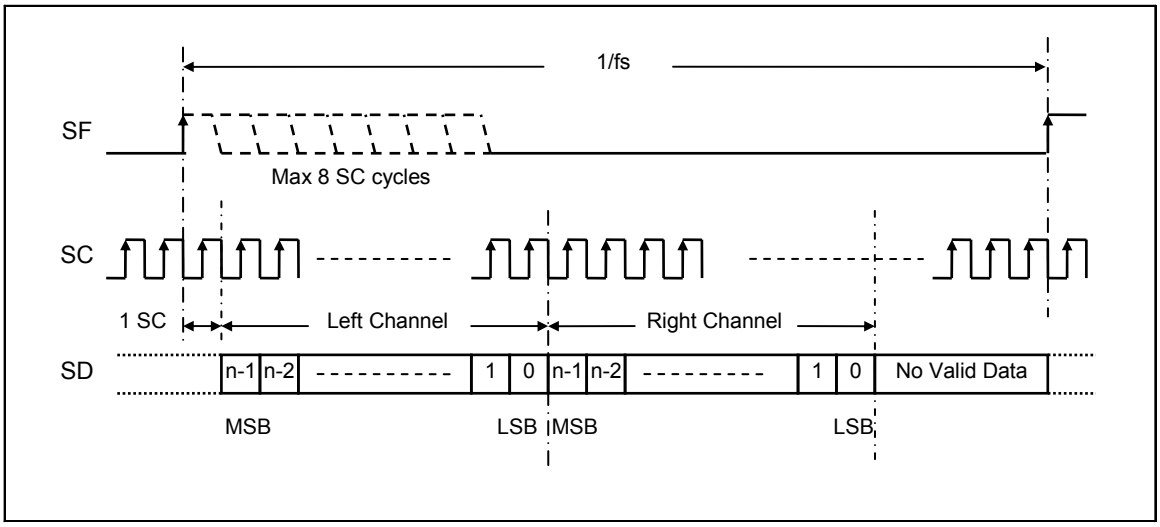


DSP MODE

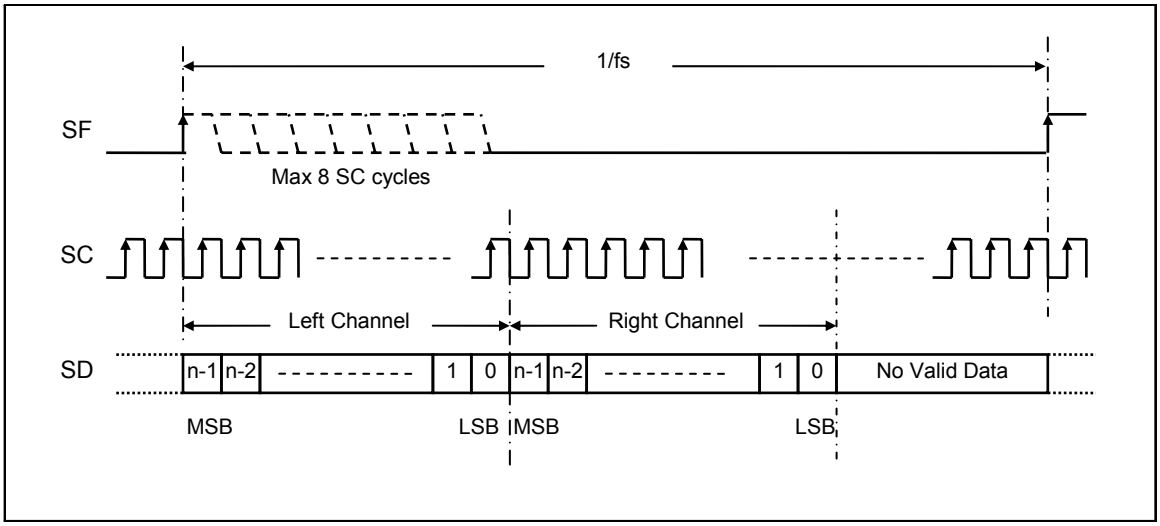
In DSP mode, the serial interface accepts input data at SD pin and frame input at SF pin. Audio data SD is time multiplexed with left channel first followed by right channel data. Frame sync SF appears every 1/fs time. Minimum SF pulse high is 1 SC cycle and maximum SF pulse high is 8 SC cycles. Both DSP 'early' mode and 'late' mode are supported.

The MSB is received first. Data is sampled at the rising edge of SC. Word lengths of 16/18/20/24 bits are supported.

DSP ‘early’ mode:



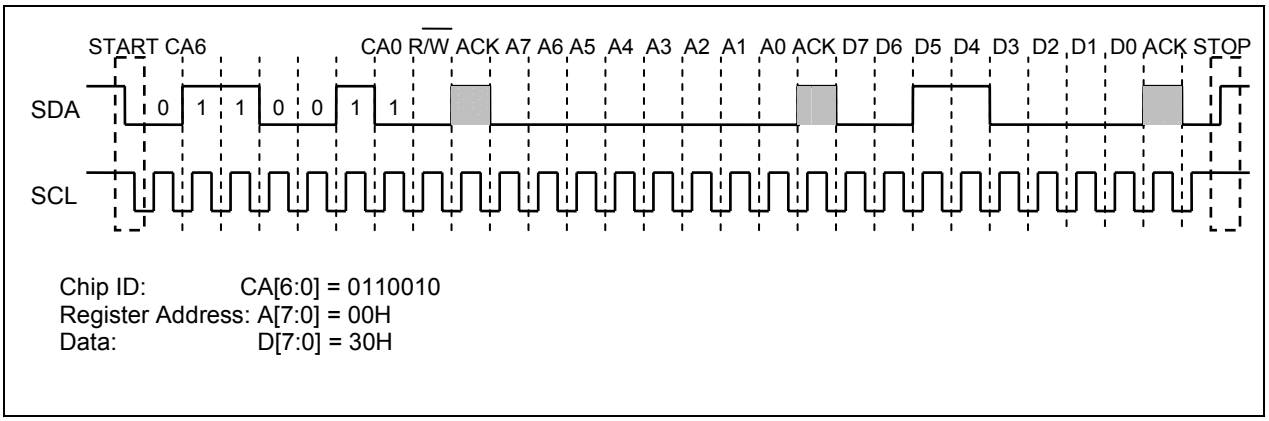
DSP ‘late’ mode:



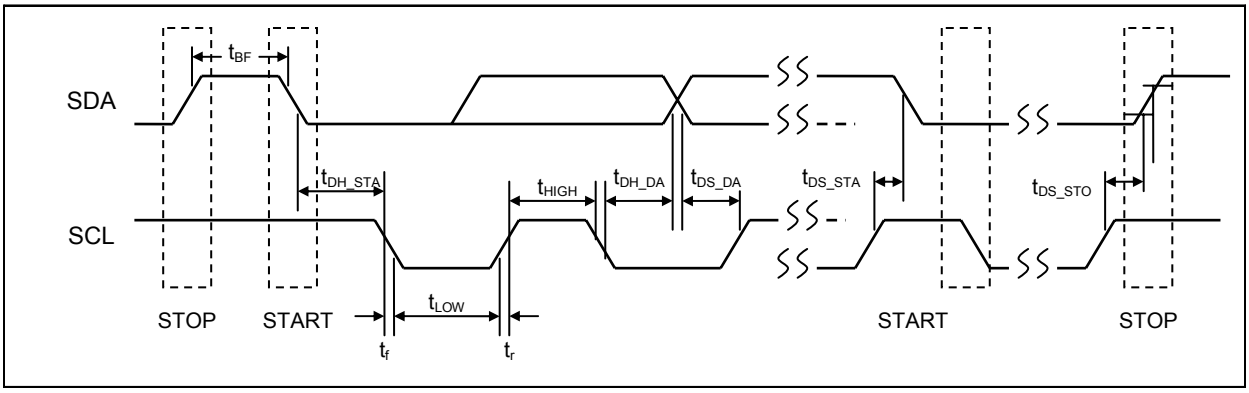
SERIAL CONTROL INTERFACE

The AV2636 supports a 2-wire I^2C compatible serial control interface. When MODE pin is externally pulled high, the FMTC and FMTD pins function as SCL and SDA. Where SCL is serial clock input and SDA is serial data input and output. The internal control registers can be programmed through the interface.

The chip ID for the AV2636 is a 7-bit hexadecimal number “32hex”. The protocol for write operation consists of sending 3 bytes of data to the AV2636 at SDA pin. Following each byte is the acknowledge bit generated by the AV2636. The first byte is the 7-bit chip ID followed by the read/write bit (read is logic high and write is logic low). The second byte is control register address. The third byte is control register data. The following diagram shows a “write” sequence and timing of control register address 00H and data 30H.



Timing specifications



Symbol	Descriptions	Min	Max	Units
f_{SC}	SCL clock frequency		100	kHz
t_{DS_STA}	START condition SDA setup time	4.7		µs
t_{DH_STA}	START condition SDA hold time	4.0		µs
t_{DS_STO}	STOP condition SDA setup time	4.0		µs
t_{LOW}	SCL low pulse time	4.7		µs
t_{HIGH}	SCL high pulse time	4.0		µs
tr	SCL and SDA rise time		1.0	µs
tf	SCL and SDA fall time		0.3	µs
t_{DS_DA}	Data setup time	250		ns
t_{DH_DA}	Data hold time	0		ns
t_{BF}	Bus free time	4.7		µs

PROGRAMMABLE CONTROL REGISTER ASSIGNMENT

There are 4 programmable control registers in AV2636. Their function and address assignment are described in the following tables. All the contents of the programmable control registers can be read back through the serial control interface.

Address (7-bit hex)	Register	Default Value (hex)	Function Description
0	CREG0[7:0]	7F	Volume control for both left and right channel
1	CREG1[7:0]	00	Device control
2	CREG2[7:0]	00	Serial audio interface mode control
3	CREG3[7:0]	00	Clock and sample rate settings

Volume Control Register (CREG0[7:0])

Address 7'h00	CREG0[7:0]							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	VOLUME[7:0]							
Default Value	0	1	1	1	1	1	1	1

Device Control Register (CREG1[7:0])

Address 7'h01	CREG1[7:0]							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	StdBy	DeEmp	Reserved					Mute
Default Value	0	0	0	0	0	0	0	0

StdBy: Stand-By Control
0: disable Stand-By (default)
1: enable Stand-By for power saving
(Notes: Mute should be enabled when StdBy is enabled.)

DeEmp: De-emphasis control
0: by-pass de-emphasis filter (default)
1: enable de-emphasis filter

Mute: Software mute control
0: do not mute the left and right channel DACs (default)
1: mute the left and right channel DACs simultaneously

Serial Audio Interface Control Register (CREG2[7:0])

Address 7'h02	CREG2[7:0]							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	Reserved		SFJ	SCJ	SAIM[1:0]		Format[1:0]	
Default Value	0	0	0	0	0	0	0	0

SFJ: Sync Frame Adjustment
0: do not delay SF signal by 1 SC clock cycle (default)
1: delay SF signal by 1 SC clock cycle

SCJ: Serial Clock Adjustment
0: do not invert SC clock (default)
1: invert SC clock

SAIM[1:0]: Serial Audio Interface Mode Control
- 00: I^2S mode
- 01: DSP 'early' mode
- 10: right justified mode
- 11: DSP 'late' mode

Format[1:0]: Serial Audio Interface Data Resolution
- 00: 24-bit resolution (default)
- 01: 20-bit resolution
- 10: 18-bit resolution
- 11: 16-bit resolution

Master Clock and Sample Rate Setting Register (CREG3[7:0])

Address 7'h03	CREG3[7:0]							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	Reserved				CKSET[3:0]			
Default Value	0	0	0	0	0	0	0	0

CKSET[3:0]: The internal operation of AV2636 is affected by the relations between MCK frequency and input audio sample rate. The correct setting of these 4-bit based on the relations ensures the correct operation of the device. The following table shows the values of the 4-bit.

CKSET[3:0] For Various Clock and Sample Rate

Sample Rate (kHz)		MCK (MHz)		CKSET[3:0]			
1X Speed	32/44.1/48	8.192/11.2896/12.288	256fs	0	0	0	0
	32/44.1/48	12.288/16.934/18.432	384fs	1	0	0	0
2X Speed	88.2/96	11.2896/12.288	128fs	0	0	0	1
	88.2/96	16.9344/18.432	192fs	1	0	0	1
	88.2/96	22.5792/24.576	256fs	0	0	1	0
	88.2/96	33.8688/36.864	384fs	1	0	1	0
4X Speed	192	12.288	64fs	0	0	1	1
	192	18.432	96fs	1	0	1	1
	192	24.576	128fs	0	1	0	0
	192	36.864	192fs	1	1	0	0
	192	49.152	256fs	0	1	0	1
	192	73.728	384fs	1	1	0	1

DIGITAL FILTER CHARACTERISTICS

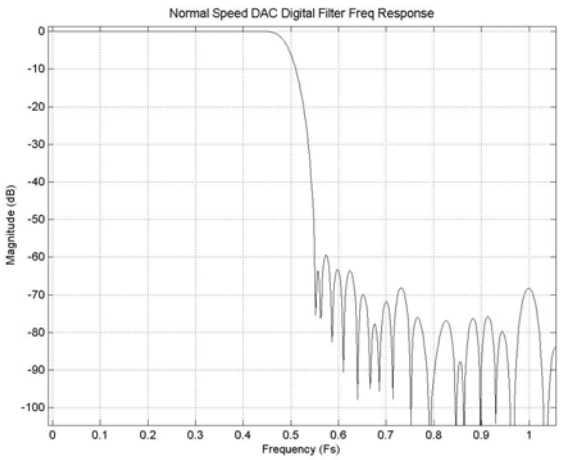
The digital interpolation filters have small passband ripples and large stopband attenuations. There are three types of filters that are implemented for different sample mode (1X/2X/4X) and MCK relations. The selection of the filters depends on the operation mode of the device, auto-detect mode or programmable mode.

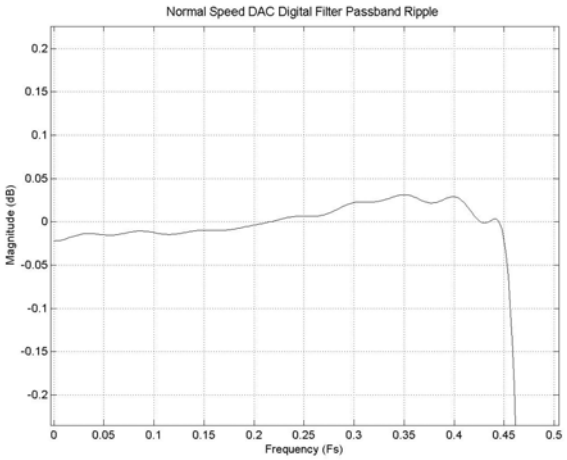
Programmable mode: filter selection is shown in the following table. 20kHz audio passband is assumed.

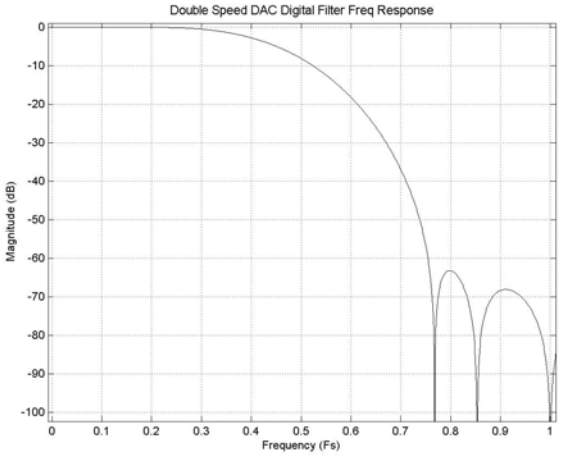
Sample Mode	Parameter	Condition	Min	Max	Unit
Normal (1X)	Passband Ripple	F < 0.45fs		±0.03	dB
	Stopband Attenuation	F > 0.55fs	60		dB
Double (2X)	Passband Ripple	F < 0.225fs		±0.03	dB
	Stopband Attenuation	F > 0.775fs	60		dB
Quad (4X)	Passband Ripple	F < 0.1125fs		±0.03	dB
	Stopband Attenuation	F > 0.8875fs	53		dB

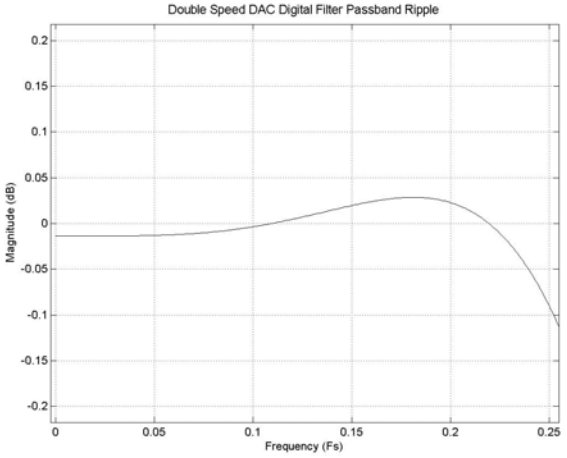
Auto-detect mode: filter type is automatically selected based on the detected sample mode and MCK relations.

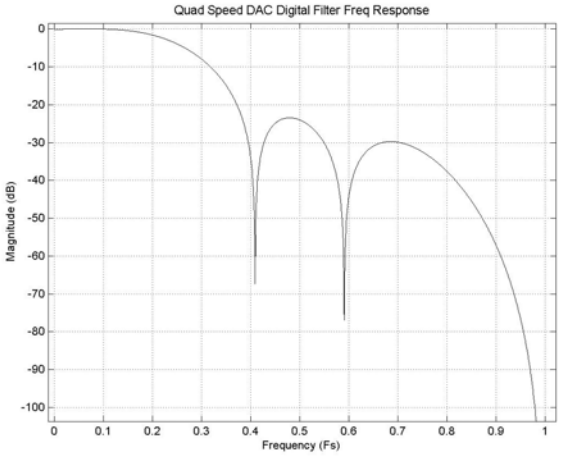
The following plots show the digital filter response and closer look of the passband ripple for normal speed mode (1X), double speed mode (2X) and quad speed (4X).

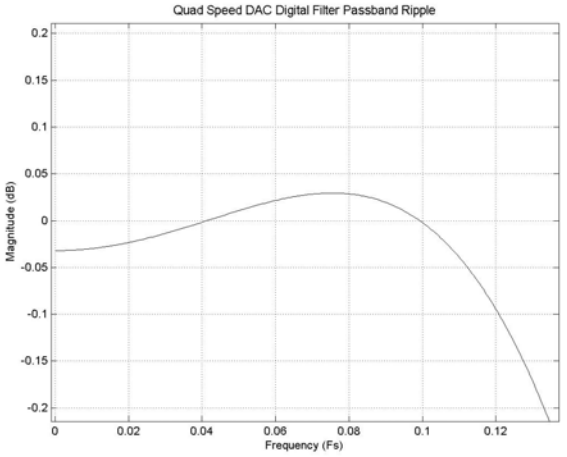

Normal Speed DAC Digital Filter Freq Response
Magnitude (dB)
Frequency (Fs)


Normal Speed DAC Digital Filter Passband Ripple
Magnitude (dB)
Frequency (Fs)


Double Speed DAC Digital Filter Freq Response
Magnitude (dB)
Frequency (Fs)

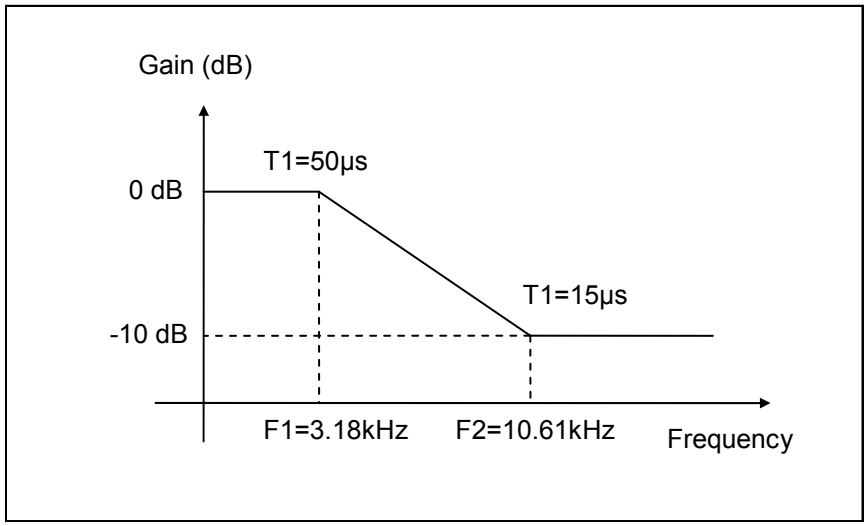

Double Speed DAC Digital Filter Passband Ripple
Magnitude (dB)
Frequency (Fs)


Quad Speed DAC Digital Filter Freq Response
Magnitude (dB)
Frequency (Fs)


Quad Speed DAC Digital Filter Passband Ripple
Magnitude (dB)
Frequency (Fs)

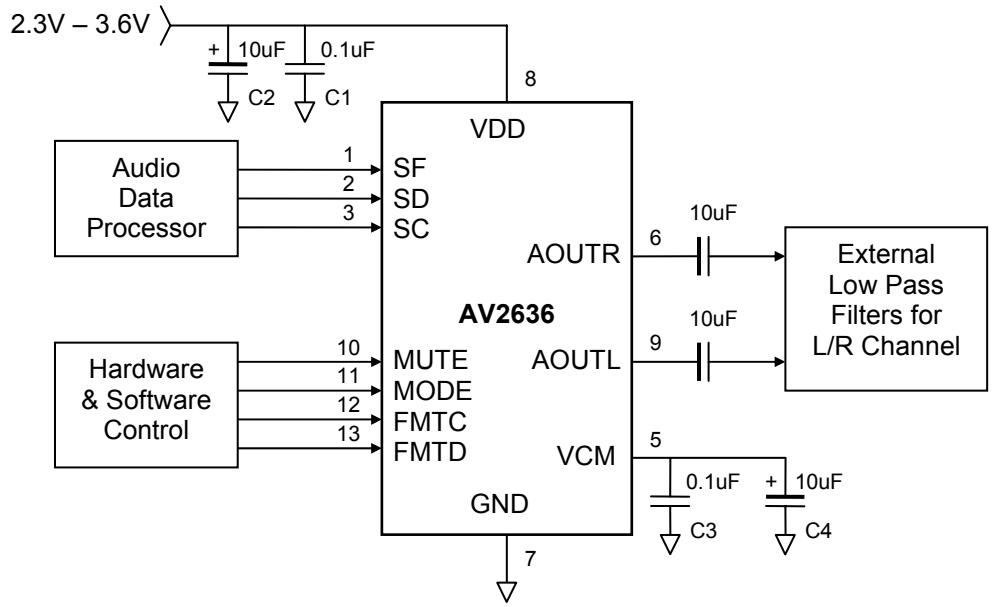
DIGITAL DE-EMPHASIS CHARACTERISTIC

The device has a build in digital de-emphasis filter that can be utilized or bypassed in either auto-detect mode or programmable mode. The characteristic of the filter for 44.1kHz sample frequency is shown as follows:



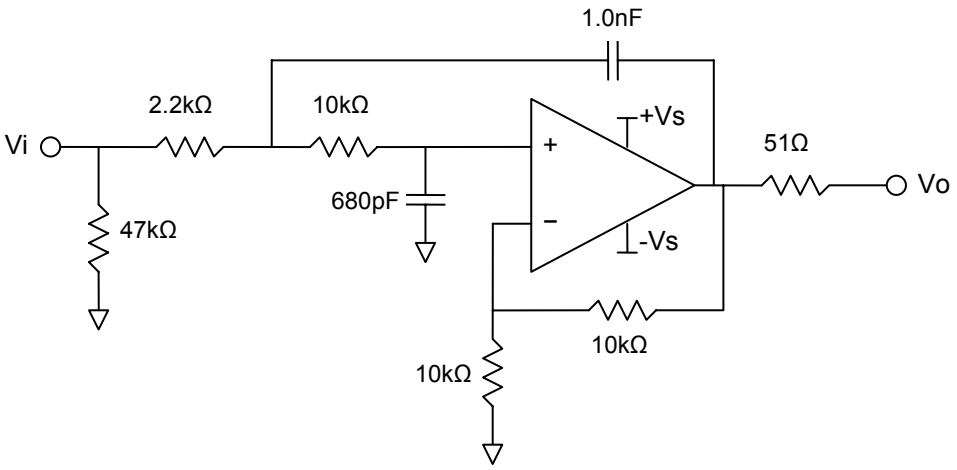
The filter response scales with sample frequency fs and is only applied to 1X sample speed mode.

RECOMMENDED APPLICATION CONNECTIONS

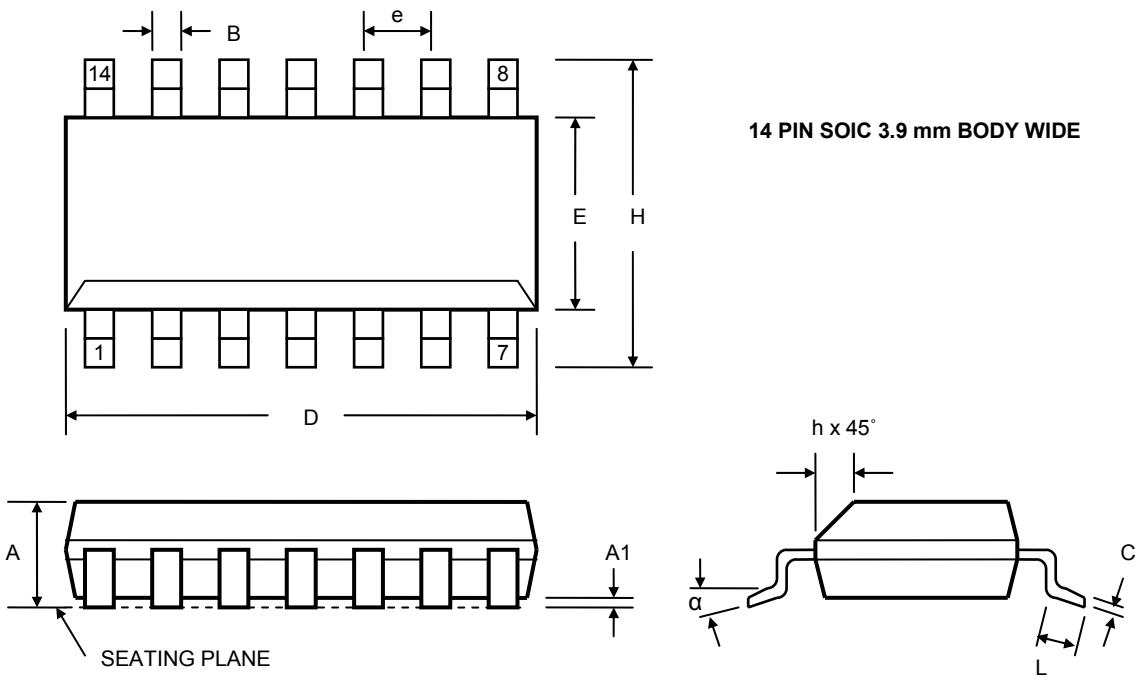


Notes:
1. Power supply VDD should be a clean analog power that separated from system digital power.
2. C1 and C3 should be placed as close to the AV2636 as possible.
3. Use low ESR capacitors for better performance.

RECOMMENDED EXTERNAL LOW PASS FILTER



PACKAGE INFORMATION



14 PIN SOIC 3.9 mm BODY WIDE

Symbols	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	8.55	8.75	0.3367	0.3444
E	3.80	4.00	0.1497	0.1574
e	1.27 BSC		0.05 BSC	
H	5.8	6.2	0.2284	0.2440
h	0.25	0.5	0.0099	0.0196
L	0.40	1.27	0.0160	0.0500
α	0˚	8˚	0˚	8˚

Note:

The package meets JEDEC.95, MS-012. Refer it for further details.