

## Revision History

### Revision 1 ( Dec. 2001 )

- 1.Fister release.

### Revision 2 ( Apr. 2002 )

1. Changed module current specification.
2. Add Performance range.
3. Changed AC Characteristics.
4. Changed typo size on module PCB in package dimensions.

## General Description

The ADD8616A8A are four-bank Double Data Rate(DDR) Synchronous DRAMs organized as 4,194,304 words x 16 bits x 4 banks, Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Data outputs occur at both rising edges of CK and /CK.

Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth high performance memory system applications

## Features

- 2.5V for VDDQ power supply
- SSTL\_2 interface
- MRS Cycle with address key programs
  - CAS Latency (2, 2.5)
  - Burst Length (2,4 &8)
  - Burst Type (sequential & Interleave)
- 4 banks operation
- Differential clock input (CK, /CK) operation
- Double data rate interface
- Auto & Self refresh
- 8192 refresh cycle
- DQM for masking
- Package:66-pins 400 mil TSOP-Type II

## Ordering Information.

| Part No.        | Frequency             | Interface | Package             |
|-----------------|-----------------------|-----------|---------------------|
| VDD8608A8A-75BA | 133Mhz(7.5ns /CL=2)   | SSTL_2    | 400mil 66pin TSOPII |
| ADD8616A8A-75B  | 133Mhz(7.5ns /CL=2.5) |           |                     |

## Pin Assignment

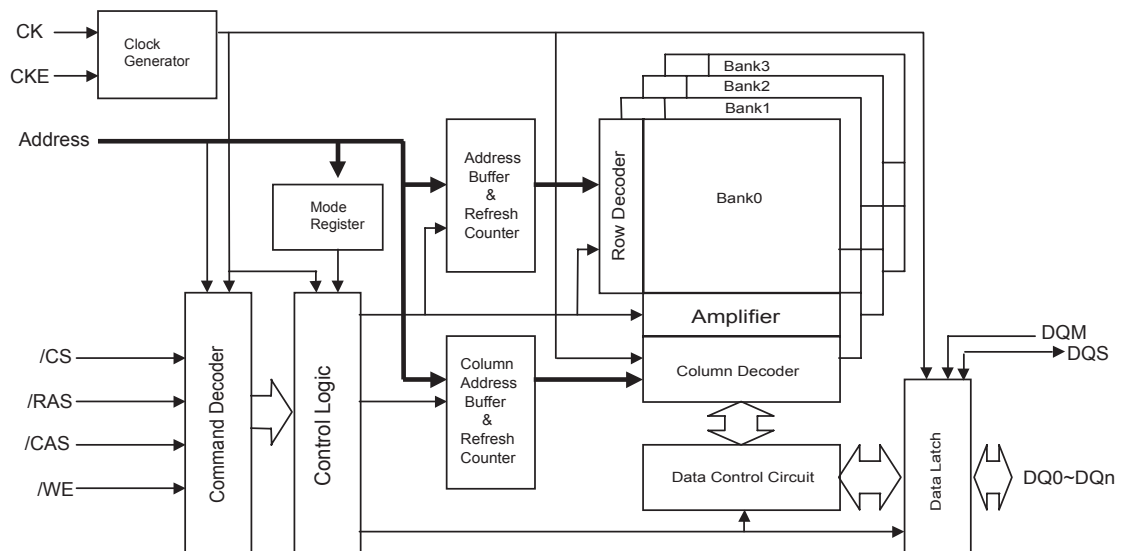
|                  |    |    |                  |
|------------------|----|----|------------------|
| V <sub>DD</sub>  | 1  | 66 | V <sub>SS</sub>  |
| DQ0              | 2  | 65 | DQ7              |
| V <sub>DDQ</sub> | 3  | 64 | V <sub>SSQ</sub> |
| NC               | 4  | 63 | NC               |
| DQ1              | 5  | 62 | DQ6              |
| V <sub>SSQ</sub> | 6  | 61 | V <sub>DDQ</sub> |
| NC               | 7  | 60 | NC               |
| DQ2              | 8  | 59 | DQ5              |
| V <sub>DDQ</sub> | 9  | 58 | V <sub>SSQ</sub> |
| NC               | 10 | 57 | NC               |
| DQ3              | 11 | 56 | DQ4              |
| V <sub>SSQ</sub> | 12 | 55 | V <sub>DDQ</sub> |
| NC               | 13 | 54 | NC               |
| NC               | 14 | 53 | NC               |
| V <sub>DDQ</sub> | 15 | 52 | V <sub>SSQ</sub> |
| NC               | 16 | 51 | DQS              |
| NC               | 17 | 50 | NC               |
| V <sub>DD</sub>  | 18 | 49 | V <sub>REF</sub> |
| NC               | 19 | 48 | V <sub>SS</sub>  |
| NC               | 20 | 47 | DM               |
| WE               | 21 | 46 | CK               |
| CAS              | 22 | 45 | CK               |
| RAS              | 23 | 44 | CKE              |
| CS               | 24 | 43 | NC               |
| NC               | 25 | 42 | NC               |
| BA0              | 26 | 41 | A11              |
| BA1              | 27 | 40 | A9               |
| A10/AP           | 28 | 39 | A8               |
| A0               | 29 | 38 | A7               |
| A1               | 30 | 37 | A6               |
| A2               | 31 | 36 | A5               |
| A3               | 32 | 35 | A4               |
| VDD              | 33 | 34 | V <sub>SS</sub>  |

66-pin plastic TSOP II 400 mil

### Pin Description

| PIN       | NAME                     | FUNCTION                                                                                                                                                                     |
|-----------|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK, /CK   | System Clock             | Differential clock input.                                                                                                                                                    |
| CKE       | Clock Enable             | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby |
| /CS       | Chip Select              | Disables or Enables device operation by masking or enabling all input except CK, CKE and DQ                                                                                  |
| A0~A12    | Address                  | Row / Column address are multiplexed on the same pins.<br>Row address : A0~A12<br>Column address : A0~A9                                                                     |
| BS0~BS1   | Banks Select             | Selects bank to be activated during row address latch time.<br>Selects bank for read / write during column address latch time.                                               |
| DQ0~DQ15  | Data                     | Data inputs / outputs are multiplexed on the same pins.                                                                                                                      |
| /RAS      | Row Address Strobe       | Latches row addresses on the positive edge of the CLK with /RAS low                                                                                                          |
| /CAS      | Column Address Strobe    | Latches Column addresses on the positive edge of the CLK with /CAS low                                                                                                       |
| /WE       | Write Enable             | Enables write operation and row recharge.                                                                                                                                    |
| VDD/VSS   | Power Supply/Ground      | Power and Ground for the input buffers and the core logic.                                                                                                                   |
| VDDQ/VSSQ | Data Output Power/Ground | Power supply for output buffers.                                                                                                                                             |
| VREF      | Reference Voltage        | Reference voltage for inputs for SSTL interface.                                                                                                                             |
| NC        | No Connection            | This pin is recommended to be left No Connection on the device.                                                                                                              |

### Block Diagram



## Absolute Maximum Ratings

| Parameter                             | Symbol                             | Value           | Unit |
|---------------------------------------|------------------------------------|-----------------|------|
| Voltage on any pin relative to Vss    | V <sub>IN</sub> , V <sub>out</sub> | -0.3 ~ VDDQ+0.3 | V    |
| Voltage on VDD supply relative to Vss | VDD, VDDQ                          | -0.3 ~ 3.6      | V    |
| Storage temperature                   | T <sub>STG</sub>                   | -55 ~ +150      | °C   |
| Power dissipation                     | P <sub>D</sub>                     | 1               | W    |
| Short circuit current                 | I <sub>OUT</sub>                   | 50              | mA   |

**Note** : Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC Operating Condition

Voltage referenced to Vss = 0V, T<sub>A</sub> = 0 to 70 °C

| Parameter                           | Symbol           | Min        | Max        | Unit | Note |
|-------------------------------------|------------------|------------|------------|------|------|
| Supply voltage                      | VDD              | 2.3        | 2.7        | V    |      |
| Supply voltage                      | VDDQ             | 2.3        | VDD        |      | 1    |
| Input logic high voltage            | V <sub>IH</sub>  | VREF+0.15  | VDDQ+0.3   | V    |      |
| Input logic low voltage             | V <sub>IL</sub>  | -0.3       | VREF-0.15  | V    | 2    |
| Differential Clock DC Input voltage | V <sub>ICK</sub> | -0.3       | VDDQ+0.3   | V    |      |
| Input Differential CLK&/CLK voltage | V <sub>ID</sub>  | 0.7        | VDDQ+0.6   | V    |      |
| Input leakage current               | I <sub>IL</sub>  | -5         | 5          | uA   | 3    |
| Output leakage current              | I <sub>OL</sub>  | -5         | 5          | uA   | 4    |
| Reference Voltage                   | VREF             | 0.49* VDDQ | 0.51* VDDQ | V    |      |
| Termination Voltage                 | V <sub>TT</sub>  | VREF-0.04  | VREF+0.04  | V    | 5    |

**Note** : 1. VDDQ must not exceed the level of VDDQ.

2. V<sub>IL</sub>(min)=-0.9V with a pulse width ≤ 5ns .

3. Any input 0V ≤ V<sub>IN</sub> ≤ 3.6V, all other pins are not under test = 0V.

4. Dout is disabled, 0V ≤ V<sub>OUT</sub> ≤ 2.7V.

5. VREF is expected to be equal to 0.5\* VDDQ of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on VREF may not exceed ±2% of the DC value.

## AC Test Condition

Voltage referenced to  $V_{SS} = 0V$ ,  $T_A = 0$  to  $70^\circ C$

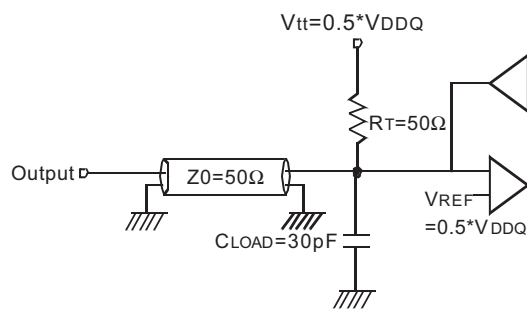
| Parameter                                     | Symbol      | Value                | Unit | Note |
|-----------------------------------------------|-------------|----------------------|------|------|
| AC input high level voltage                   | $V_{IH}$    | $V_{REF}+0.31$       | V    |      |
| AC input low level voltage                    | $V_{IL}$    | $V_{REF}-0.31$       | V    |      |
| Input Reference Voltage                       | $V_{REF}$   | $0.5 \times V_{DDQ}$ | V    |      |
| Termination Voltage                           | $V_{TT}$    | $0.5 \times V_{DDQ}$ | V    |      |
| Input Signal Peak to Peak Swing               | $V_{SWING}$ | 1.0                  | V    |      |
| Input Difference Voltage. CLK and /CLK Inputs | $V_{ID}$    | 1.5                  | V    |      |

## Capacitance

$T_A=25^\circ C$ ,  $f=1MHz$

| Parameter                       | Pin                                          | Symbol | Min | Max | Unit |
|---------------------------------|----------------------------------------------|--------|-----|-----|------|
| Input capacitance               | CK, /CK                                      | CI1    | 2   | 3.0 | pF   |
|                                 | A0~A12,BS0,BS1,CKE,/CS,/RAS,<br>/CAS,/WE,DQM | CI2    | 2   | 3.0 | pF   |
| Data input / output capacitance | DQM                                          | CI/O   | 4   | 5   | pF   |

## Output load circuit



**Output Load Circuit (SSTL\_2)**

### DC Characteristics II

| Parameter                                        | Symbol | Test condition                                                                                                               | Speed       | Unit | Note |
|--------------------------------------------------|--------|------------------------------------------------------------------------------------------------------------------------------|-------------|------|------|
|                                                  |        |                                                                                                                              | -75BA/ -75B |      |      |
| Operating Current                                | IDD1   | Burst length=2, One bank active<br>$T_{rc}=t_{RC}(\min)$ , $I_{OUT}=0mA$                                                     | 110         | mA   | 1    |
| Precharge standby current in power down mode     | IDD2P  | $CKE \leq V_{IL}(\max)$ , $t_{CK}=\min$                                                                                      | 20          | mA   |      |
| Precharge standby current in Non power down mode | IDD2N  | $CKE \geq V_{IH}(\min)$ , $/CS \geq V_{IH}(\min)$ ,<br>$t_{CK}=t_{CK} \min$ input signals are changed one time during 2clks. | 40          | mA   |      |
| Active standby current in power down mode        | IDD3P  | $CKE \leq V_{IL}(\max)$ , $t_{CK}=t_{CK} \min$                                                                               | 20          | mA   |      |
| Active standby current in Non power down mode    | IDD3N  | $CKE \geq V_{IH}(\min)$ , $/CS \geq V_{IH}(\min)$ ,<br>$t_{CK}=\min$ input signals are changed one time during 2clks.        | 65          | mA   |      |
| Burst mode operating current                     | IDD4R  | $t_{CK} \geq t_{CK}(\min)$ , $I_{OUT}=0 mA$<br>All banks active                                                              | 155         | mA   | 1    |
| Auto refresh current                             | IDD5   | $t_{RRC} \geq t_{RRC}(\min)$ , All banks active                                                                              | 190         | mA   | 2    |
| Self refresh current                             | IDD6   | $CKE \leq 0.2V$                                                                                                              | 3           | mA   |      |

**Note:** 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.

2. Min. of  $t_{RRC}$  is shown at AC characteristics.

## AC Characteristics

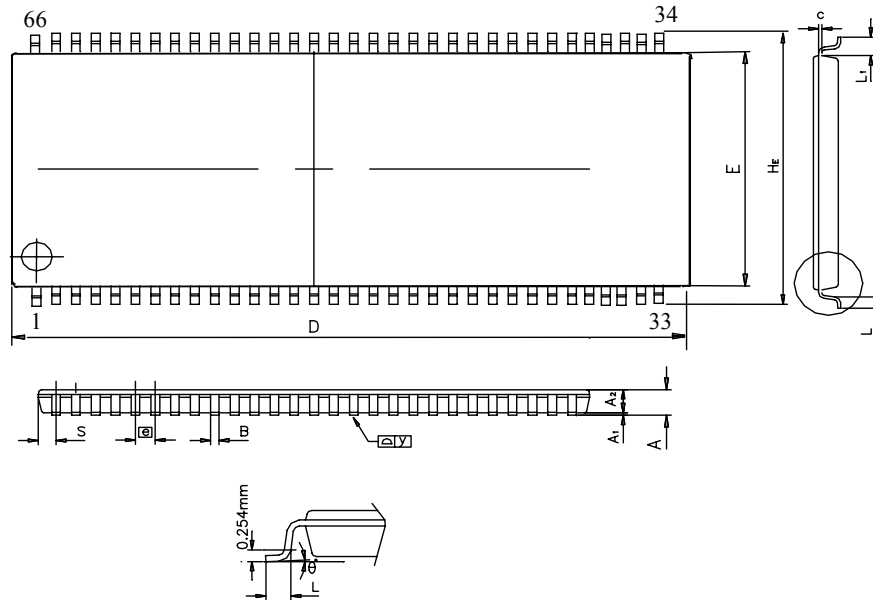
| Parameter                               |                    | Symbol | -75BA |      | -75B  |      | Unit |
|-----------------------------------------|--------------------|--------|-------|------|-------|------|------|
|                                         |                    |        | Min   | Max  | Min   | Max  |      |
| System clock                            | /CAS Latency = 2.5 | tCK2.5 | 7.5   | 12   | 7.5   | 12   | ns   |
| Cycle time                              | /CAS Latency = 2   | tCK2   | 7.5   | 12   | 10    | 12   |      |
| Clock high pulse width                  |                    | tCHW   | 0.45  | 0.55 | 0.45  | 0.55 | CLK  |
| Clock low pulse width                   |                    | tCLW   | 0.45  | 0.55 | 0.45  | 0.55 | CLK  |
| Access time form CK to /CK              |                    | tAC    | -0.75 | 0.75 | -0.75 | 0.75 | ns   |
| Data strobe edge to clock edge          |                    | tDQSCK | -0.75 | 0.75 | -0.75 | 0.75 | ns   |
| Clock to first rising edge of DQS delay |                    | tDQSS  | 0.75  | 1.25 | 0.75  | 1.25 | CLK  |
| /RAS cycle time                         |                    | tRC    | 65    | -    | 65    | -    | ns   |
| /RAS to /CAS delay                      |                    | tRCD   | 20    | -    | 20    | -    | ns   |
| /RAS active time                        |                    | tRAS   | 45    | 120K | 45    | 120K | ns   |
| /RAS precharge time                     |                    | tRP    | 20    | -    | 20    | -    | ns   |
| /RAS to /RAS bank active delay          |                    | tRRD   | 15    | -    | 15    | -    | ns   |
| /CAS to /CAS delay                      |                    | tCCD   | 1     | -    | 1     | -    | CLK  |
| Data-in setup time (to DQS)             |                    | tDS    | 0.5   | -    | 0.5   | -    | ns   |
| Data-in hold time (to DQS)              |                    | tDH    | 0.5   | -    | 0.5   | -    | ns   |
| DQS Falling Edge to CLK Setup Time      |                    | tDSS   | 0.2   | -    | 0.2   | -    | CLK  |
| DQS Falling Edge Hold Time from CLK     |                    | tDSH   | 0.2   | -    | 0.2   | -    | CLK  |
| Input setup time                        |                    | tIS    | 0.9   | -    | 0.9   | -    | ns   |
| Input hold time                         |                    | tIH    | 0.9   | -    | 0.9   | -    | ns   |
| DQS-in high level width                 |                    | tDSH   | 0.35  | -    | 0.35  | -    | CLK  |
| DQS-in low level width                  |                    | tDSL   | 0.35  | -    | 0.35  | -    | CLK  |
| Clock to DQS write preamble setup time  |                    | tWPRES | 0     | -    | 0     | -    | ns   |
| Write preamble                          |                    | tWPST  | 0.4   | 06   | 0.4   | 06   | CLK  |
| Data strobe edge to output data edge    |                    | tDQSQ  |       | 0.5  |       | 0.5  | ns   |
| Mode register set cycle time            |                    | tMRD   | 15    |      | 15    |      |      |
| DQS read preamble                       |                    | tRPRE  | 0.9   | 1.1  | 0.9   | 1.1  | CLK  |

### Command Truth-Table

| SYM.  | Command                   |         |   | CKEn-1 | CKEn | /CS | /RAS | /CAS | /WE | DM | ADDR | A10/AP | BS |
|-------|---------------------------|---------|---|--------|------|-----|------|------|-----|----|------|--------|----|
| MRS   | Mode Register Set         |         |   | H      | X    | L   | L    | L    | L   | X  | CA   | CA     | L  |
| NOP   | No Operation              |         |   | H      | X    | L   | H    | H    | H   | X  | X    |        |    |
| ACT   | Bank Active               |         |   | H      | X    | L   | L    | H    | H   | X  | V    |        | V  |
| READ  | Read                      |         |   | H      | X    | L   | H    | L    | H   | X  | V    | L      | V  |
| READA | Read with Auto Precharge  |         |   |        |      |     |      |      |     |    |      | H      |    |
| WRIT  | Write                     |         |   | H      | X    | L   | H    | L    | L   | X  | V    | L      | V  |
| WRITA | Write with Auto Precharge |         |   |        |      |     |      |      |     |    |      | H      |    |
| PREA  | Precharge All Bank        |         |   | H      | X    | L   | L    | H    | L   | X  | X    | H      | X  |
| BST   | Burst Stop                |         |   | H      | X    | L   | H    | H    | L   | X  | X    |        |    |
| AREF  | Auto Refresh              |         |   | H      | H    | L   | L    | L    | H   | X  | X    |        |    |
| SELF  | Self Refresh              | Entry   | H | L      | L    | L   | L    | H    | X   | X  |      |        |    |
| SELEX |                           | Exit    | L | H      | H    | X   | X    | X    | X   |    |      |        |    |
|       |                           |         |   |        | L    | H   | H    | H    |     |    |      |        |    |
| PD    | Precharge<br>Power down   | Entry   | H | L      | H    | X   | X    | X    | X   | X  |      |        |    |
| L     |                           |         |   |        | H    | H   | H    |      |     |    |      |        |    |
| PDEX  |                           | Exit    | L | H      | H    | X   | X    | X    | X   |    |      |        |    |
|       |                           |         |   |        | L    | H   | H    | X    |     |    |      |        |    |
| WDE   | Data write                | Enable  | H | X      | X    | X   | X    | X    | L   | X  |      |        |    |
| WDD   |                           | Disable | H | X      | X    | X   | X    | X    | H   |    |      |        |    |



## Package Information



| SYMBOL         | MILLIMETER |       |       | INCH      |        |        |
|----------------|------------|-------|-------|-----------|--------|--------|
|                | MIN.       | NOM.  | MAX.  | MIN.      | NOM.   | MAX.   |
| A              |            |       | 1.20  |           |        | 0.047  |
| A1             | 0.05       |       | 0.15  | 0.002     |        | 0.006  |
| A2             | 0.95       | 1.00  | 1.05  | 0.037     | 0.039  | 0.041  |
| B              | 0.17       | 0.24  | 0.32  | 0.007     | 0.009  | 0.013  |
| c              | 0.09       | 0.145 | 0.2   | 0.004     | 0.0006 | 0.008  |
| D              | 22.62 BSC  |       |       | 0.891 BSC |        |        |
| H <sub>E</sub> | 11.74      | 11.76 | 11.78 | 0.462     | 0.463  | 0.464  |
| E              | 10.15      | 10.16 | 10.17 | 0.3996    | 0.400  | 0.4004 |
| e              | 0.65 BSC   |       |       | 0.026     |        |        |
| L              | 0.40       | 0.50  | 0.60  | 0.016     | 0.020  | 0.024  |
| L1             | 0.80 REF   |       |       | 0.031 REF |        |        |
| S              | 0.71 REF   |       |       | 0.028 REF |        |        |
| θ              | 0 °        | -     | 8 °   | 0 °       | -      | 8 °    |

400mil 66pin TSOP II Package