Ultrafast 3.3 V Single-Supply Comparators

Preliminary Technical Data

ADCMP572/ADCMP573

FEATURES

3.3 V/5.2 V single-supply operation
150 ps propagation delay
15 ps overdrive and slew rate dispersion
8 GHz equivalent input risetime bandwidth
80 ps minimum pulse width
35 ps typical output rise/fall
10 ps deterministic jitter (DJ)
200 fs random jitter (RJ)
On-chip terminations at both input pins
Robust inputs with no output phase reversal
Resistor programmable hysteresis
Differential latch control
Power supply rejection > 70 dB

FUNCTIONAL BLOCK DIAGRAM

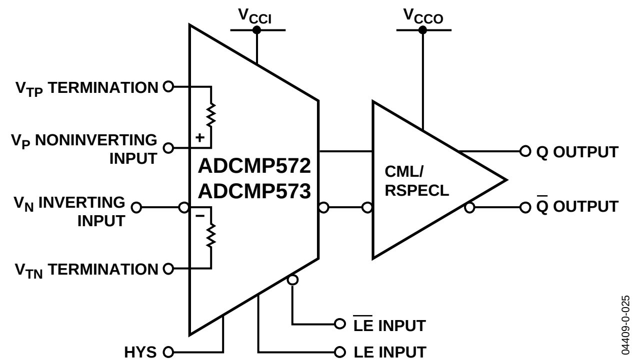

Figure 1.

APPLICATIONS

Automatic test equipment (ATE)
High speed instrumentation
Pulse spectroscopy
Medical imaging and diagnostics
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Clock and data signal restoration

GENERAL DESCRIPTION

The ADCMP572/ADCMP573 are ultrafast comparators fabricated on Analog Devices, Inc.'s proprietary XFCB3 Silicon Germanium (SiGe) bipolar process. The ADCMP572 features CML output drivers, and the ADCMP573 features reduced swing PECL (RSPECL) output drivers.

Both devices offer 150 ps propagation delay and 100 ps minimum pulse width for 10 Gbps operation with 200 fs RMS random jitter (RJ). Overdrive and slew rate dispersion is typically less than 15 ps.

A flexible power supply scheme allows either device to operate with a single +3.3 V positive supply and a −0.2 V to +1.2 V input signal range, or with split input/output supplies to support a wider −0.2 V to +3.2 V input signal range and an independent range of output levels. 50 Ω on-chip termination resistors are provided at both inputs with the optional capability to leave open (on an individual pin basis) for applications requiring high impedance inputs.

The CML output stage is designed to directly drive 400 mV into 50 Ω transmission lines terminated to between 3.3 V to 5.2 V. The RSPECL output stage is designed to drive 400 mV into 50 Ω terminated to V_{CCO} − 2 V and is compatible with several commonly used PECL logic families. The comparator input stage offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. High speed latch and programmable hysteresis features are also provided.

The ADCMP572/ADCMP573 are available in a 16-lead LFCSP package.

Rev. PrB

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REVISION HISTORY

6/04—Revision PrB: Preliminary Version

2/04—Revision PrA: Preliminary Version

ELECTRICAL CHARACTERISTICS

$V_{CCI} = V_{CCO} = 3.3$ V, $T_A = 25$°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Input Voltage Range	V_P, V_N	$V_{CCI} = 3.3$ V, $V_{CCO} = 3.3$ V	−0.2		+1.2	V
		$V_{CCI} = 5.2$ V, $V_{CCO} = 3.3$ V	−0.2		+3.2	V
Input Differential Voltage			−1.2		+1.2	V
Input Offset Voltage	V_{OS}		−5.0	±2.0	+5.0	mV
Offset Voltage Tempco	$\Delta V_{OS}/dT$			10.0		µV/°C
Input Bias Current	I_P, I_N	Open termination	−50.0	−25.0	0.0	µA
Input Bias Current Tempco				50.0		nA/°C
Input Offset Current			−5.0	±2.0	+5.0	µA
Input Capacitance	C_P, C_N			TBD		pF
Input Impedance			47.5	50	52.5	Ω
Input Resistance, Differential Mode		Open termination		50		kΩ
Input Resistance, Common Mode		Open termination		500		kΩ
Active Gain	A_V			54		dB
Common-Mode Rejection	CMRR	$V_{CCI} = 3.3$ V, $V_{CCO} = 3.3$ V, $V_{CM} = 0.0$ V to 1.0 V		50		dB
		$V_{CCI} = 5.2$ V, $V_{CCO} = 3.3$ V, $V_{CM} = 0.0$ V to 3.0 V		40		dB
Hysteresis		$R_{HYS} = \infty$		±1		mV
LATCH ENABLE CHARACTERISTICS						
ADCMP572						
Latch Enable Input Range			2.8		V_{CCO}+0.2	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	$V_{OD} = 100$ mV		15		ps
Latch Hold Time	t_H	$V_{OD} = 100$ mV		0		ps
ADCMP573						
Latch Enable Input Range			1.8		V_{CCO}−0.6	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	$V_{OD} = 100$ mV		0		ps
Latch Hold Time	t_H	$V_{OD} = 100$ mV		50		ps
Latch Enable Input Impedance			47.5	50.0	52.5	Ω
Latch to Output Delay	t_{PLOH}, t_{PLOL}	$V_{OD} = 100$ mV		150		ps
Latch Minimum Pulse Width	t_{PL}	$V_{OD} = 100$ mV		100		ps
DC OUTPUT CHARACTERISTICS						
ADCMP572 (CML)						
Output Impedance	Z_{OUT}	−8 mA < I_{OUT} < 8 mA	47.5	50.0	52.5	Ω
Output Voltage High Level	V_{OH}	50 Ω terminate to V_{CCO}	V_{CCO}−0.10	V_{CCO}−0.05	V_{CCO}	V
Output Voltage Low Level	V_{OL}	50 Ω terminate to V_{CCO}	V_{OH}−0.45	V_{OH}−0.40	V_{OH}−0.35	V
Output Voltage Differential		50 Ω terminate to V_{CCO}	350	400	450	mV
Temperature Coefficient, V_{OH}	$\Delta V_{OH}/dT$	50 Ω terminate to V_{CCO}		TBD		mV/°C
Temperature Coefficient, V_{OL}	$\Delta V_{OL}/dT$	50 Ω terminate to V_{CCO}		TBD		mV/°C
ADCMP573 (RSPECL)						
Output Voltage High Level	V_{OH}	50 Ω terminate to V_{CCO}−2.0	V_{CCO}−0.90	V_{CCO}−0.80	V_{CCO}−0.70	V
Output Voltage Low Level	V_{OL}	50 Ω terminate to V_{CCO}−2.0	V_{OH}−0.45	V_{OH}−0.40	V_{OH}−0.35	V
Output Voltage Differential		50 Ω terminate to V_{CCO}−2.0	350	400	450	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AC PERFORMANCE						
Propagation Delay	t_{PD}	V_{CCI} = 3.3 V, V_{OD} = 200 mV		150		ps
		V_{CCI} = 3.3 V, V_{OD} = 20 mV		165		ps
		V_{CCI} = 5.2 V, V_{OD} = 200 mV		145		ps
Propagation Delay Tempco	$\Delta t_{PD}/dT$			0.5		ps/°C
Prop Delay Skew—Rising Transition to Falling Transition		V_{OD} = 200 mV, 5 V/ns		10		ps
Overdrive Dispersion		50 mV < V_{OD} < 1.0 V, 5 V/ns		10		ps
		10 mV < V_{OD} < 1.0 V, 5 V/ns		15		ps
Slew Rate Dispersion		2 V/ns to 10 V/ns		15		ps
Pulse Width Dispersion		100 ps to 5 ns		5		ps
Duty Cycle Dispersion		V_{CCI} = 3.3 V, 1 V/ns, V_{CM} = 0 V		5		ps
		V_{CCI} = 5.2 V, 1 V/ns, V_{CM} = 0 V		10		
Common-Mode Dispersion		V_{OD}=0.4V, 0.0 V < V_{CM} < 1.0 V		5		ps/V
Equivalent Input Bandwidth[1]	BW_{EQ}	0.0 V to 400 mV input		8.0		GHz
		$t_R = t_F$ = 25 ps, 20/80				
Toggle Rate		> 50% Output Swing		12.5		Gbps
Deterministic Jitter	DJ	V_{OD} = 200 mV, 5 V/ns, $PRBS^{31}-1$ NRZ, 4 Gbps		10		ps
Deterministic Jitter	DJ	V_{OD} = 200 mV, 5 V/ns, $PRBS^{31}-1$ NRZ, 10 Gbps		TBD		ps
RMS Random Jitter	RJ	V_{OD} = 200 mV, 5 V/ns, 1.25 GHz		0.2		ps
Minimum Pulse Width	PW_{MIN}	$\Delta t_{PD}/\Delta PW$ < 5 ps		100		ps
Minimum Pulse Width	PW_{MIN}	$\Delta t_{PD}/\Delta PW$ < 10 ps		80		ps
Rise Time	t_R	20/80		35		ps
Fall Time	t_F	20/80		35		ps
POWER SUPPLY						
Input Supply Voltage Range	V_{CCI}		3.1		5.4	V
Output Supply Voltage Range	V_{CCO}		3.1		5.4	V
Positive Supply Differential	$V_{CCI} - V_{CCO}$		−0.2		+2.3	V
ADCMP572 (CML)						
Positive Supply Current	$I_{VCCI} + I_{VCCO}$	V_{CCI} = 3.3 V, V_{CCO} = 3.3 V, terminate 50 Ω to V_{CCO}		44	52	mA
		V_{CCI} = 5.2 V, V_{CCO} = 5.2 V, terminate 50 Ω to V_{CCO}		44	52	
Power Dissipation	P_D	V_{CCI} = 3.3 V, V_{CCO} = 3.3 V, terminate 50 Ω to V_{CCO}		145	160	mW
		V_{CCI} = 5.2 V, V_{CCO} = 5.2 V, terminate 50 Ω to V_{CCO}		240	265	
ADCMP573 (RSPECL)						
Positive Supply Current	$I_{VCCI} + I_{VCCO}$	V_{CCI} = 3.3 V, V_{CCO} = 3.3 V, 50 Ω to V_{CCO} − 2 V		66	74	mA
		V_{CCI} = 5.2 V, V_{CCO} = 5.2 V, 50 Ω to V_{CCO} − 2V		68	76	
Power Dissipation	P_D	V_{CCI} = 3.3 V, V_{CCO} = 3.3 V, 50 Ω to V_{CCO} − 2 V		145	160	mW
		V_{CCI} = 5.2 V, V_{CCO} = 5.2 V, 50 Ω to V_{CCO} − 2 V		175	195	
Power Supply Rejection—V_{CCI}	PSR_{VCCI}	V_{CCI} = 3.3 V ±5%, V_{CCO} = 3.3 V		74		dB

[1] Equivalent Input Bandwidth assumes a simple first-order response and is calculated with the following formula: $BW_{EQ} = 0.22/\sqrt{(tr_{COMP}^2 - tr_{IN}^2)}$, where tr_{IN} is the 20/80 transition time of a quasi-Gaussian signal applied to the comparator input and tr_{COMP} is the effective transition time digitized by the comparator.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
SUPPLY VOLTAGES	
Input Supply Voltage (V_{CCI} to GND)	−0.5 V to +6.0 V
Output Supply Voltage (V_{CCO} to GND)	−0.5 V to +6.0 V
Positive Supply Differential (V_{CCI} − V_{CCO})	−0.5 V to +3.5 V
INPUT VOLTAGES	
Input Voltage	−0.5 V to V_{CCI} + 0.5 V
Differential Input Voltage	±(V_{CCI} + 0.5 V)
Input Voltage, Latch Enable	−0.5 V to V_{CCO} + 0.5 V
HYSTERESIS CONTROL PIN	
Applied Voltage (HYS to GND)	−0.5 V to +1.5 V
Maximum Input/Output Current	±1 mA
OUTPUT CURRENT	
ADCMP572 (CML)	±20 mA
ADCMP573 (RSPECL)	−35 mA
TEMPERATURE	
Operating Temperature, Ambient	−40°C to +85°C
Operating Temperature, Junction	125°C
Storage Temperature Range	−65°C to +150°C

Thermal Considerations

The ADCMP572/ADCMP573 LFCSP 16-lead package has a θ_{JA} (junction to ambient thermal resistance) of 70°C/W in still air.

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

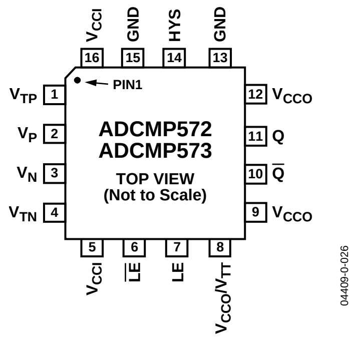

Figure 2. ADCMP572/ADCMP573 Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{TP}	Termination Resistor Return Pin for V_P Input.
2	V_P	Noninverting Analog Input.
3	V_N	Inverting Analog Input.
4	V_{TN}	Termination Resistor Return Pin for V_N Input.
5, 16	V_{CCI}	Positive Supply Voltage for Input Stage.
6	$\overline{LE}$	Latch Enable Input Pin, Inverting Side. In compare mode ($\overline{LE}$ = low), the output tracks changes at the input of the comparator. In latch mode ($\overline{LE}$ = high), the output reflects the input state just prior to the comparator's being placed in latch mode. $\overline{LE}$ must be driven in compliment with LE.
7	LE	Latch Enable Input Pin, Noninverting Side. In compare mode (LE = high), the output tracks changes at the input of the comparator. In latch mode (LE = low), the output reflects the input state just prior to the comparator's being placed in latch mode. LE must be driven in compliment with $\overline{LE}$.
8	V_{CCO}/V_{TT}	Termination Return Pin for the LE/$\overline{LE}$ Input Pins. For the ADCMP572 (CML output stage), this pin should be connected to the positive V_{CCO} supply. For the ADCMP573 (RSPECL output stage), this pin should be connected to the V_{CCO} – 2 V termination potential.
13, 15	GND	Ground.
9, 12	V_{CCO}	Positive Supply Voltage for the CML/RSPECL Output Stage.
10	$\overline{Q}$	Inverting Output. $\overline{Q}$ is at logic low if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided the comparator is in compare mode. See the LE/$\overline{LE}$ description (Pins 6 and 7) for more information.
11	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input V_P is greater than the analog voltage at the inverting input, V_N, provided the comparator is in compare mode. See the LE/$\overline{LE}$ description (Pins 6 and 7) for more information.
14	HYS	Hysteresis Control Pin. Leave this pin disconnected for zero hysteresis. Connect to GND with a suitably sized resistor to add the desired amount of hysteresis. Refer to Figure 7 for proper sizing of R_{HYS} hysteresis control resistor.
Heatsink	N/C	The metallic back surface of the package is not electrically connected to any part of the circuit, and it can be left floating for best electrical isolation between the package handle and the substrate of the die. But it can also be soldered to the application board if improved thermal and/or mechanical stability is desired.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CCI} = V_{CCO} = 3.3$ V, $T_A = 25°C$, unless otherwise noted.

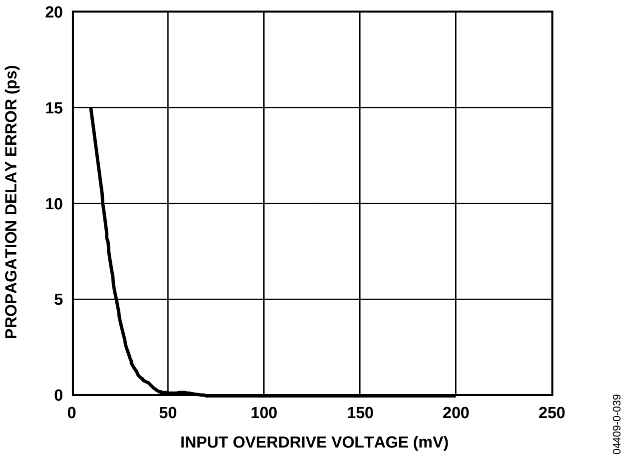

Figure 3. Propagation Delay vs. Input Overdrive

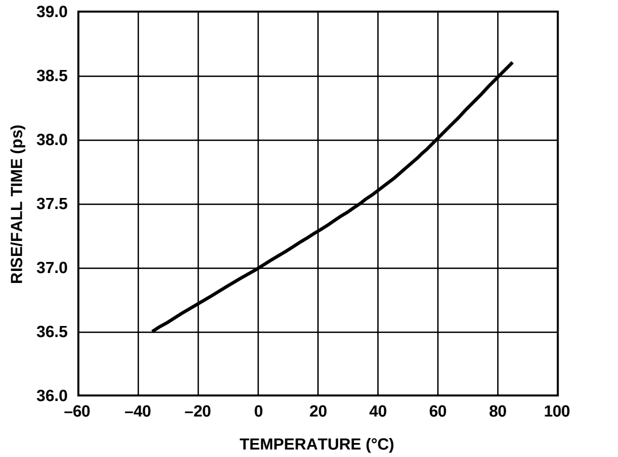

Figure 6. Rise/Fall Time vs. Temperature

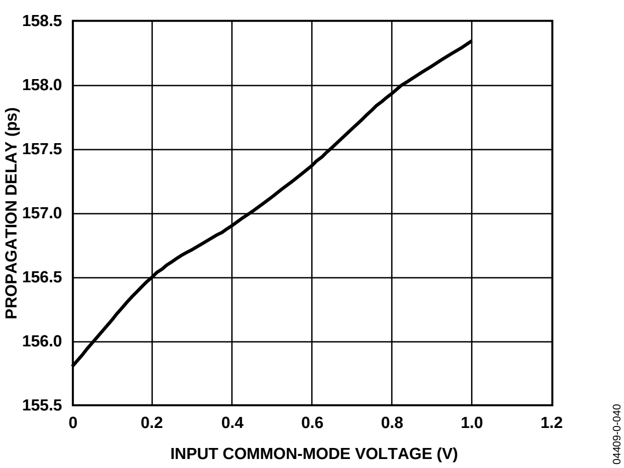

Figure 4. Propagation Delay vs. Input Common Mode

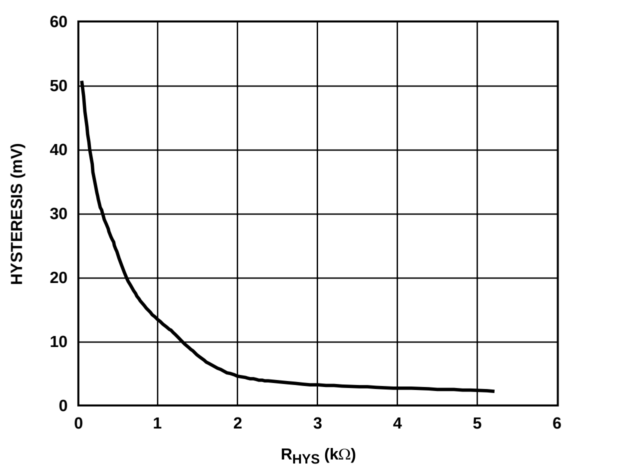

Figure 7. Hysteresis vs. R_{HYS} Control Resistor

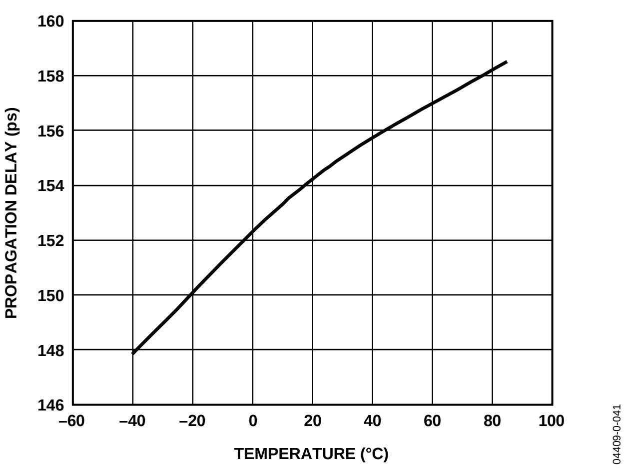

Figure 5. Propagation Delay vs. Temperature

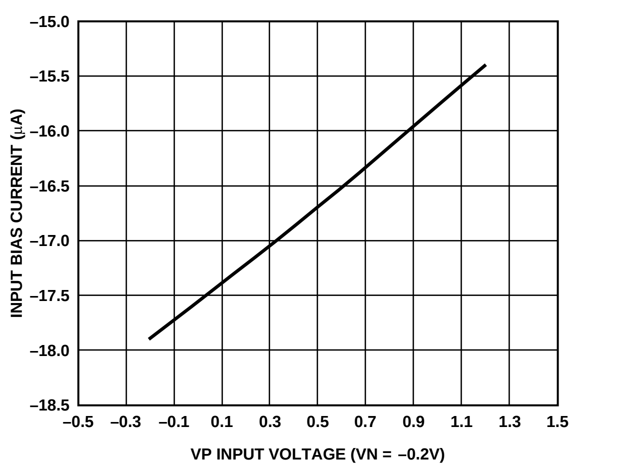

Figure 8. Input Bias Current vs. Input Differential

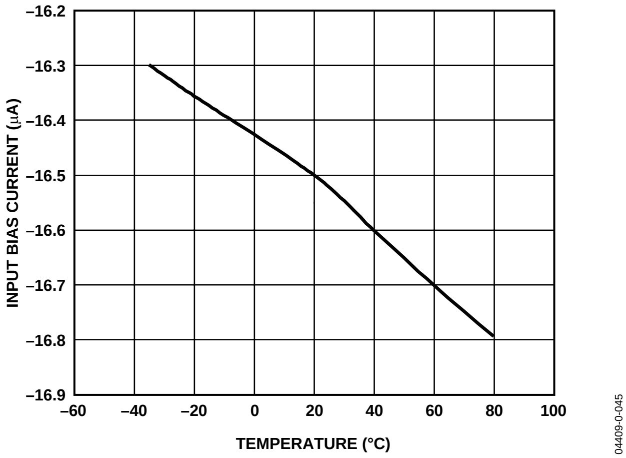

Figure 9. Input Bias Current vs. Temperature

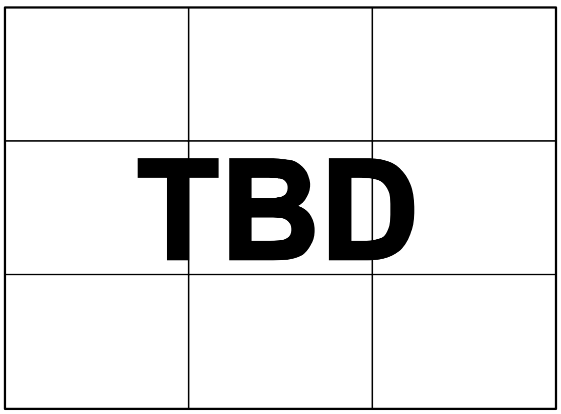

Figure 10. Input Offset Voltage vs. Temperature

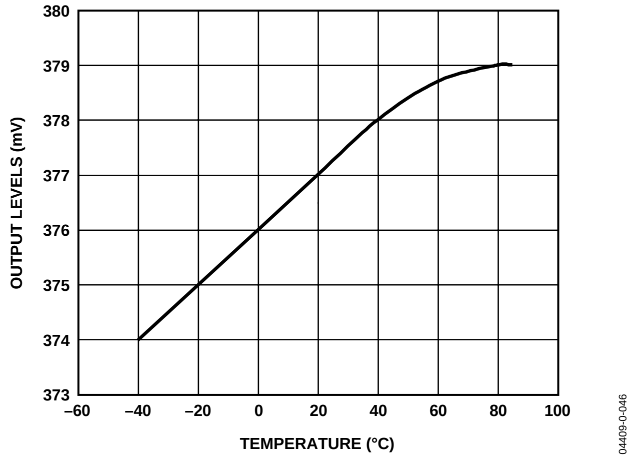

Figure 11. Output Levels vs. Temperature

APPLICATION INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCMP572/ADCMP573 comparators are very high speed SiGe devices. Consequently, it is essential to use proper high speed design techniques to achieve the specified performance. Of critical importance is the use of low impedance supply planes, particularly the output supply plane (V_{CCO}) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. A 1 μF electrolytic bypass capacitor should be placed within several inches of each power supply pin to ground. In addition, multiple high quality 0.1 μF bypass capacitors should be placed as close as possible to each of the V_{CCI} and V_{CCO} supply pins and should be connected to the GND plane with redundant vias. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should also be strictly avoided to maximize the effectiveness of the bypass at high frequencies.

If the input and output supplies are connected separately such that $V_{CCI} \neq V_{CCO}$, then care should be taken to bypass each of these supplies separately to the GND plane. A bypass capacitor should not be connected between them. It is recommended that the GND plane separate the V_{CCI} and V_{CCO} planes when the circuit board layout is designed to minimize coupling between the two supplies and to take advantage of the additional bypass capacitance from each respective supply to the ground plane. This enhances the performance when split input/output supplies are used. If the input and output supplies are connected together for single-supply operation such that $V_{CCI} = V_{CCO}$, then coupling between the two supplies is unavoidable; however, every effort should be made to keep the supply plane adjacent to the GND plane to maximize the additional bypass capacitance this arrangement provides.

CML/RSPECL OUTPUT STAGE

Specified propagation delay dispersion performance can be achieved only by using proper transmission line terminations. The outputs of the ADCMP572 are designed to directly drive 400 mV into 50 Ω cable or microstrip and/or stripline transmission lines properly terminated to the V_{CCO} supply plane. The CML output stage is shown in the simplified schematic diagram of Figure 12. The outputs are each back-terminated with 50 Ω for best transmission line matching. The RSPECL outputs of the ADCMP573 are illustrated in Figure 13 and should be terminated to V_{CCO} − 2 V. As an alternative, Thevenin equivalent termination networks may also be used in either case if the direct termination voltage is not readily available. If high speed output signals must be routed more than a centimeter, microstrip or stripline techniques are essential to ensure proper transition times and to prevent output ringing and pulse-width dependant propagation delay dispersion. For the most timing critical applications where transmission line reflections pose the greatest risk to performance, the ADCMP572 provides the best match to 50 Ω output transmission paths.

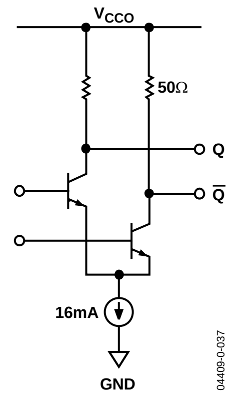

Figure 12. Simplified Schematic Diagram of the ADCMP572 CML Output Stage

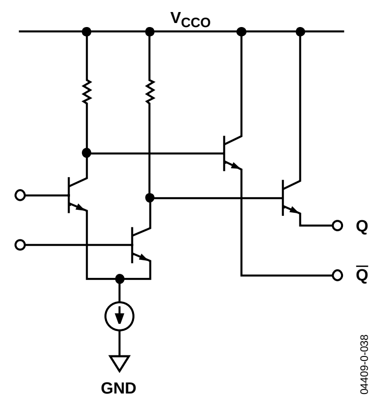

Figure 13. Simplified Schematic Diagram of the ADCMP573 RSPECL Output Stage

USING/DISABLING THE LATCH FEATURE

The latch inputs (LE/$\overline{\text{LE}}$) are active low for latch mode, and are internally terminated with 50 Ω resistors to Pin 8. This corresponds to the V_{CCO} supply for the ADCMP572 and the V_{TT} pin for the ADCMP573. All V_{CCO} pins should be connected to the supply plane for maximum performance, and the V_{TT} pin should be connected externally to V_{CCO} − 2 V, preferably to its own low inductance plane. When using the ADCMP572, the latch function can be disabled by connecting the $\overline{\text{LE}}$ pin to GND with an external pull-down resistor and leaving the LE pin unconnected. To prevent excessive power dissipation, the resistor should be 750 Ω when V_{CCO} = 3.3 V, and 1.2 kΩ when V_{CCO} = 5.2 V. When using the ADCMP573 comparator, the latch can be disabled by connecting the LE pin to V_{CCO} with an external 500 Ω resistor, and leaving the $\overline{LE}$ pin disconnected. In this case, the resistor value does not depend on the chosen V_{CCO} supply voltage, assuming the V_{TT} pin is properly connected to V_{CCO} – 2 V.

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential to obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and can often cause oscillation. Discontinuities along input and output transmission lines can also severely limit the specified pulse-width dispersion performance.

For applications working in a 50 Ω environment, input and output matching has a significant impact on data dependant (or deterministic) jitter (DJ) and pulse-width dispersion performance. The ADCMP572/ADCMP573 comparators provide internal 50 Ω termination resistors for both V_P and V_N inputs, and the ADCMP572 provides 50 Ω back terminated outputs. The return side for each input termination is pinned out separately with the V_{TP} and V_{TN} pins, respectively. If a 50 Ω termination is desired at one or both of the V_P/V_N inputs, then the V_{TP} and V_{TN} pins can be connected (or disconnected) to (from) the desired termination potential as required. The termination potential should be carefully bypassed using high quality bypass capacitors as discussed above to prevent undesired aberrations on the input signal due to parasitic inductance in the circuit board layout. If a 50 Ω input termination is not desired, either one or both of the V_{TP}/V_{TN} termination pins can be left disconnected. In this case, the pins should be left floating with no external pull-downs or bypassing capacitors.

It should be understood that when leaving an input termination disconnected, the internal resistor acts as a small stub on the input transmission path and can cause problems for very high speed inputs. Reflections should then be expected from the comparator inputs because they no longer provide a matched impedance to the input path leading to the device. It then becomes important to back-match the drive source impedance to the input transmission path to minimize multiple reflections. For applications in which the comparator is very close to the driving signal source, the source impedance should be minimized. High source impedance in combination with parasitic input capacitance of the comparator could cause an undesirable degradation in bandwidth at the input, thus degrading the overall response. Although the ADCMP572/ ADCMP573 comparators have been designed to minimize input capacitance, some parasitic capacitance is inevitable. It is therefore recommended that the drive source impedance be no more than 50 Ω for best high speed performance.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP572/ADCMP573 comparators are designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV to 500 mV. Propagation delay dispersion is a variation in propagation delay that results from a change in the degree of overdrive or slew rate (how far or how fast the input signal exceeds the switching threshold).

Propagation delay dispersion is a specification that becomes important in high speed time critical applications such as data communication, automatic test and measurement, instrumentation, and event-driven applications such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (Figure 14 and Figure 15). For the ADCMP572/ADCMP573, dispersion is typically <15 ps because the overdrive is varied from 10 mV to 500 mV, and the input slew rate is varied from 2 V/ns to 10 V/ns. This specification applies for both positive and negative signals since the ADCMP572/ADCMP573 has substantially equal delays for either positive-going or negative-going inputs.

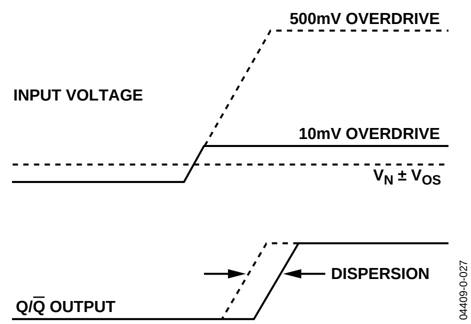

Figure 14. Propagation Delay—Overdrive Dispersion

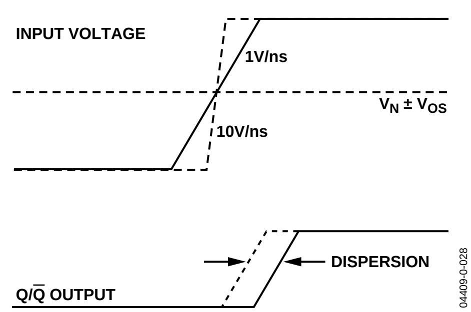

Figure 15. Propagation Delay—Slew Rate Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often desirable in a noisy environment or when the differential input amplitudes are relatively small or slow moving. The transfer function for a comparator with hysteresis is shown in Figure 16. If the input voltage approaches the threshold (0.0 V in this example) from the negative direction, the comparator switches from a low to a high when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in the high state until the threshold $-V_H/2$ is crossed from the positive direction. In this manner, noise centered on 0.0 V input does not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

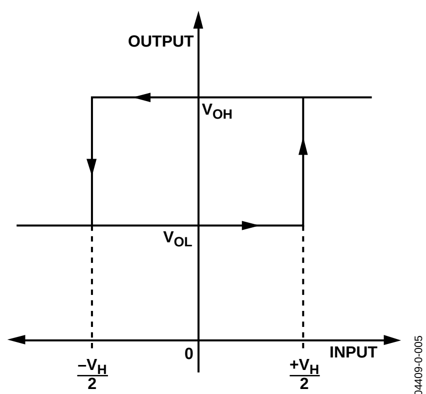

Figure 16. Comparator Hysteresis Transfer Function

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. A limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high speed performance, and can even induce oscillation in some cases.

The ADCMP572/ADCMP573 comparators offer a programmable hysteresis feature that can significantly improve the accuracy and stability of the desired hysteresis. By connecting an external pull-down resistor from the HYS pin to GND, a variable amount of hysteresis can be applied. Leaving the HYS pin disconnected disables the feature, and hysteresis is then less than 1 mV as specified. The maximum hysteresis that can be applied using this method is approximately ±25 mV. Figure 17 illustrates the amount of hysteresis applied as a function of external resistor value. The advantages of applying hysteresis in this manner are improved accuracy, stability, and reduced component count. An external bypass capacitor is not recommended on the HYS pin because it would likely degrade the jitter performance of the device.

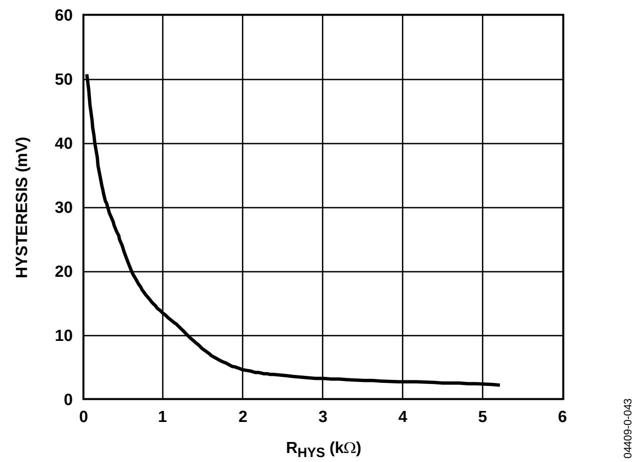

Figure 17. Hysteresis vs. R_{HYS} Control Resistor

MINIMUM INPUT SLEW RATE REQUIREMENT

As with all high speed comparators, a minimum slew rate requirement must be met to ensure that the device does not oscillate as the input signal crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator and the feedback parasitics inherent in the package. Analog Devices recommends a minimum slew rate of 50 V/μs to ensure a clean output transition from the ADCMP572/ ADCMP573 comparators unless hysteresis is programmed as discussed previously.

TYPICAL APPLICATION CIRCUITS

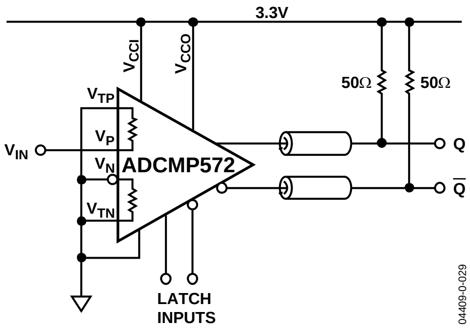

Figure 18. Zero-Crossing Detector with 3.3 V CML Outputs

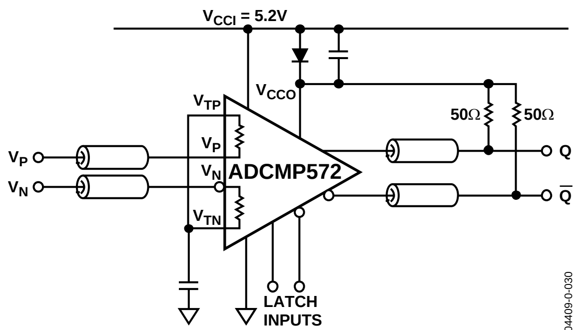

Figure 19. LVDS to50 Ω Back-Terminated (RS)PECL Receiver

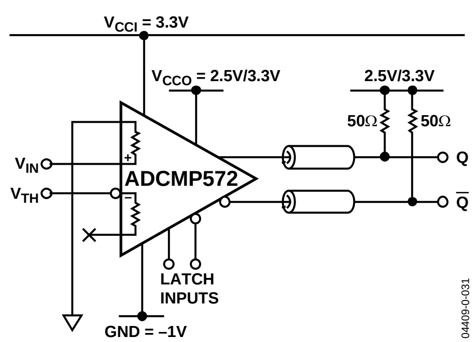

Figure 20. Comparator with ±1 V Input Range and 2.5 V or 3.3 V CML Outputs

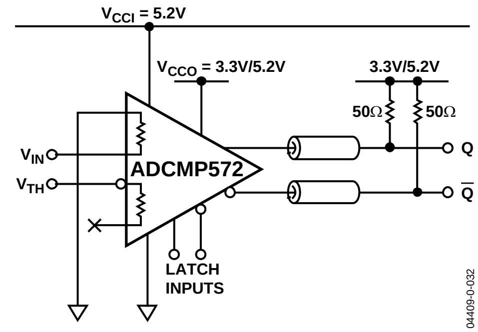

Figure 21. Comparator with 0 V to 3 V Input Range and 3.3 V or 5.2 V Positive CML Outputs

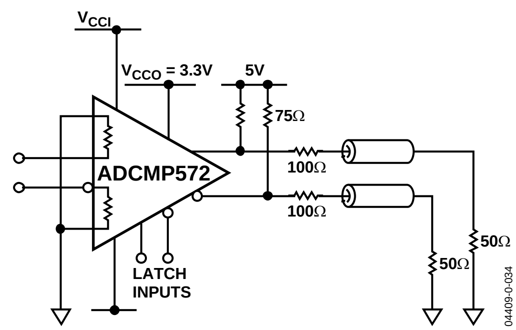

Figure 22. Interfacing 3.3 V CML to a 50 Ω Ground Terminated Instrument

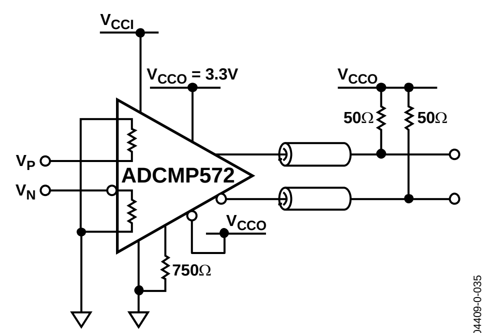

Figure 23. Disabling the Latch Feature

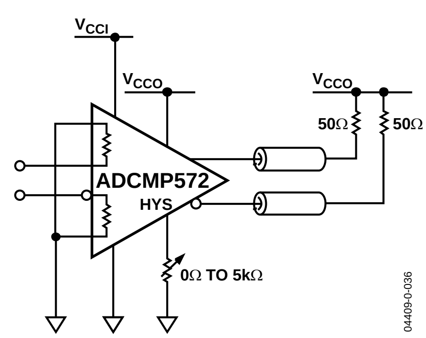

Figure 24. Adding Hysteresis Using the HYS Control Pin

TIMING INFORMATION

Figure 25 illustrates the ADCMP572/ADCMP573 compare and latch timing relationships. Table 4 provides definitions of the terms shown in the figure.

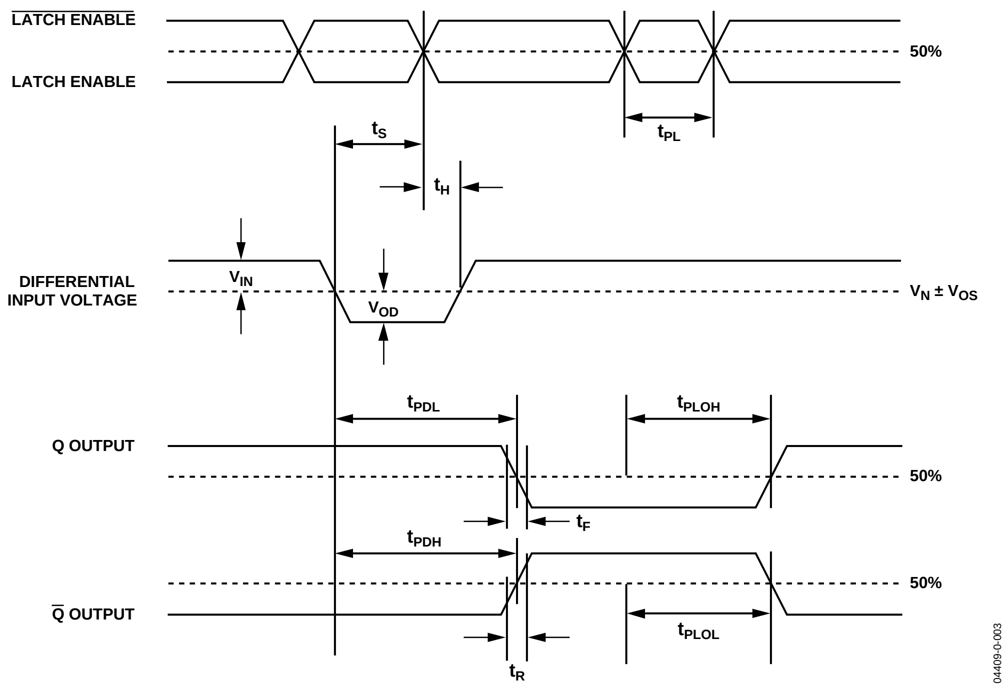

Figure 25. System Timing Diagram

Table 4. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch enable to output high delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch enable to output low delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum hold time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum latch enable pulse width	Minimum time that the latch enable signal must be high to acquire an input signal change.
t_S	Minimum setup time	Minimum time before the negative transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs.
t_R	Output rise time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output fall time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_{OD}	Voltage overdrive	Difference between the input voltages V_A and V_B.

OUTLINE DIMENSIONS

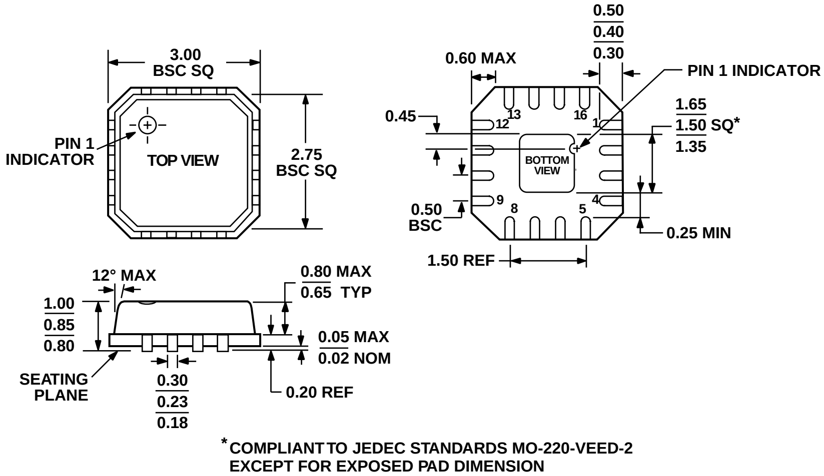

Figure 26. 16-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADCMP572BCP	–40°C to 85°C	LFCSP-16	CP-16
ADCMP573BCP	–40°C to 85°C	LFCSP-16	CP-16

NOTES

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