

74LVC3G34

Triple buffer gate

Rev. 03 — 31 January 2005

Product data sheet

1. General description

The 74LVC3G34 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device as translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC3G34 provides three buffers.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C.

PHILIPS

3. Quick reference data

Table 1: Quick reference data

$GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL} , t_{PLH}	propagation delay input nA to output nY	$V_{CC} = 1.8\text{ V}$; $C_L = 30\text{ pF}$; $R_L = 1\text{ k}\Omega$	-	3.8	-	ns
		$V_{CC} = 2.5\text{ V}$; $C_L = 30\text{ pF}$; $R_L = 500\text{ }\Omega$	-	2.4	-	ns
		$V_{CC} = 2.7\text{ V}$; $C_L = 50\text{ pF}$; $R_L = 500\text{ }\Omega$	-	2.5	-	ns
		$V_{CC} = 3.3\text{ V}$; $C_L = 50\text{ pF}$; $R_L = 500\text{ }\Omega$	-	2.2	-	ns
		$V_{CC} = 5.0\text{ V}$; $C_L = 50\text{ pF}$; $R_L = 500\text{ }\Omega$	-	1.9	-	ns
C_I	input capacitance		-	2.5	-	pF
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3\text{ V}$	[1] [2]	14	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[2] The condition is $V_i = GND$ to V_{CC} .

4. Ordering information

Table 2: Ordering information

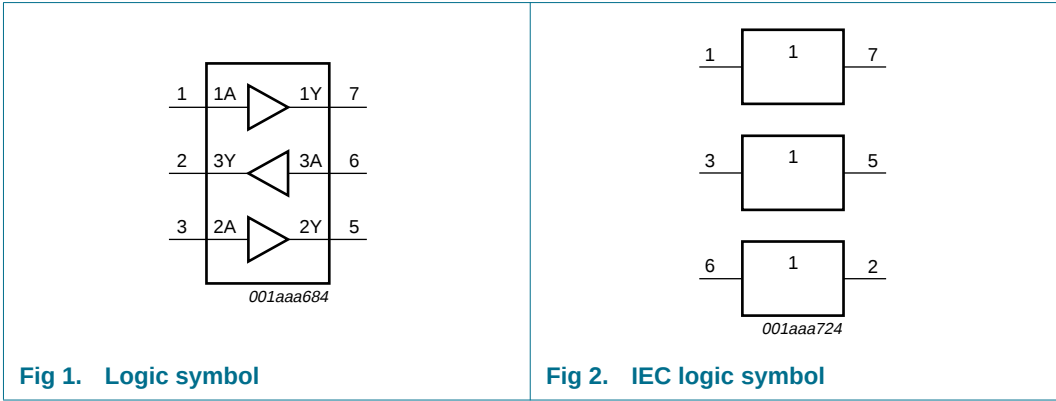
Type number	Package			
	Temperature range	Name	Description	Version
74LVC3G34DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3G34DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC3G34GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $1 \times 1.95 \times 0.5\text{ mm}$	SOT833-1

5. Marking

Table 3: Marking codes

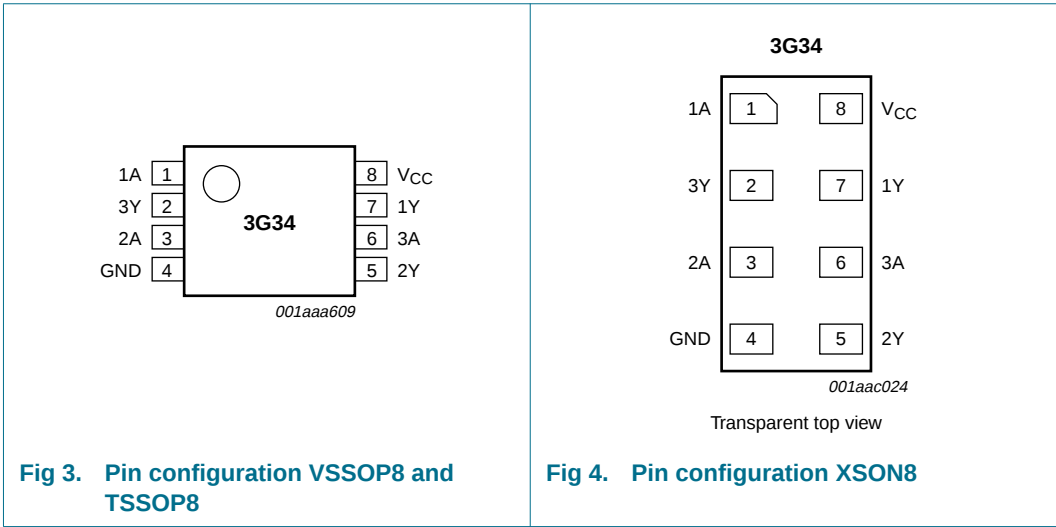
Type number	Marking code
74LVC3G34DP	V34
74LVC3G34DC	Y34
74LVC3G34GT	Y34

6. Functional diagram



7. Pinning information

7.1 Pinning



7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
1A	1	data input
3Y	2	data output
2A	3	data input
GND	4	ground (0 V)
2Y	5	data output
3A	6	data input
1Y	7	data output
V _{CC}	8	supply voltage

8. Functional description

Table 5: Function table [\[1\]](#)

Input nA	Output nY
L	L
H	H

[1] H = HIGH voltage level;
L = LOW voltage level.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage		[1] -0.5	+6.5	V
V_O	output voltage	active mode	[1] [2] -0.5	$V_{CC} + 0.5$	V
		Power-down mode	[1] [2] -0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V	-	-50	mA
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
I_O	output source or sink current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40$ °C to +125 °C	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

10. Recommended operating conditions

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	active mode	0	-	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.65$ V to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	0	-	10	ns/V

11. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = –100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} – 0.1	-	-	V
		I _O = –4 mA; V _{CC} = 1.65 V	1.2	-	-	V
		I _O = –8 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = –12 mA; V _{CC} = 2.7 V	2.2	-	-	V
		I _O = –24 mA; V _{CC} = 3.0 V	2.3	-	-	V
		I _O = –32 mA; V _{CC} = 4.5 V	3.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	V
I _{LI}	input leakage current	V _{CC} = 5.5 V; V _I = 5.5 V or GND	-	±0.1	±5	µA
I _{off}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	µA
I _{CC}	quiescent supply current	V _{CC} = 5.5 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	µA
ΔI _{CC}	additional quiescent supply current per pin	V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} – 0.6 V; I _O = 0 A	-	5	500	µA
C _I	input capacitance		-	2.5	-	pF
T_{amb} = –40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V

Table 8: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\ \mu\text{A}$; $V_{CC} = 1.65\ \text{V}$ to $5.5\ \text{V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\ \text{mA}$; $V_{CC} = 1.65\ \text{V}$	0.95	-	-	V
		$I_O = -8\ \text{mA}$; $V_{CC} = 2.3\ \text{V}$	1.7	-	-	V
		$I_O = -12\ \text{mA}$; $V_{CC} = 2.7\ \text{V}$	1.9	-	-	V
		$I_O = -24\ \text{mA}$; $V_{CC} = 3.0\ \text{V}$	2.0	-	-	V
		$I_O = -32\ \text{mA}$; $V_{CC} = 4.5\ \text{V}$	3.4	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\ \mu\text{A}$; $V_{CC} = 1.65\ \text{V}$ to $5.5\ \text{V}$	-	-	0.1	V
		$I_O = 4\ \text{mA}$; $V_{CC} = 1.65\ \text{V}$	-	-	0.70	V
		$I_O = 8\ \text{mA}$; $V_{CC} = 2.3\ \text{V}$	-	-	0.45	V
		$I_O = 12\ \text{mA}$; $V_{CC} = 2.7\ \text{V}$	-	-	0.60	V
		$I_O = 24\ \text{mA}$; $V_{CC} = 3.0\ \text{V}$	-	-	0.80	V
		$I_O = 32\ \text{mA}$; $V_{CC} = 4.5\ \text{V}$	-	-	0.80	V
I_{LI}	input leakage current	$V_{CC} = 5.5\ \text{V}$; $V_I = 5.5\ \text{V}$ or GND	-	-	± 20	μA
I_{off}	power-off leakage current	$V_{CC} = 0\ \text{V}$; V_I or $V_O = 5.5\ \text{V}$	-	-	± 20	μA
I_{CC}	quiescent supply current	$V_{CC} = 5.5\ \text{V}$; $V_I = V_{CC}$ or GND; $I_O = 0\ \text{A}$	-	-	40	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_{CC} = 2.3\ \text{V}$ to $5.5\ \text{V}$; $V_I = V_{CC} - 0.6\ \text{V}$; $I_O = 0\ \text{A}$	-	-	5000	μA

[1] All typical values are measured at $T_{amb} = 25\ ^\circ\text{C}$.

12. Dynamic characteristics

Table 9: Dynamic characteristicsGND = 0 V; test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\ ^\circ\text{C}$ to $+85\ ^\circ\text{C}$ [1]						
t_{PHL} , t_{PLH}	propagation delay input nA to output nY	see Figure 5				
		$V_{CC} = 1.65\ \text{V}$ to $1.95\ \text{V}$	1.0	3.8	8.6	ns
		$V_{CC} = 2.3\ \text{V}$ to $2.7\ \text{V}$	0.5	2.4	4.4	ns
		$V_{CC} = 2.7\ \text{V}$	0.5	2.5	5.0	ns
		$V_{CC} = 3.0\ \text{V}$ to $3.6\ \text{V}$	0.5	2.2	4.1	ns
		$V_{CC} = 4.5\ \text{V}$ to $5.5\ \text{V}$	0.5	1.9	3.2	ns
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3\ \text{V}$ [2] [3]	-	14	-	pF

Table 9: Dynamic characteristics ...continuedGND = 0 V; test circuit see [Figure 6](#).

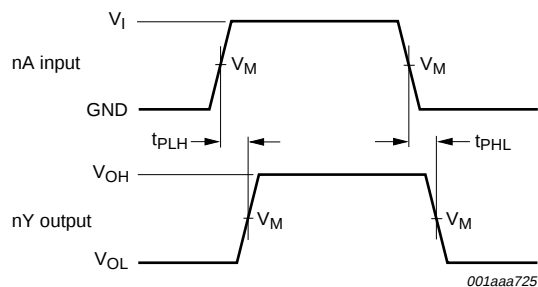
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
t _{PHL} , t _{PLH}	propagation delay input nA to output nY	see Figure 5				
		V _{CC} = 1.65 V to 1.95 V	1.0	-	10.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	-	5.5	ns
		V _{CC} = 2.7 V	0.5	-	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	-	5.1	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	-	4.0	ns

[1] All typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:f_i = input frequency in MHz;f_o = output frequency in MHz;C_L = output load capacitance in pF;V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.[3] The condition is V_I = GND to V_{CC}.

13. AC waveforms

Measurement points are given in [Table 10](#).Logic levels: V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.**Fig 5. Input nA to output nY propagation delay times****Table 10: Measurement points**

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V _{CC}	0.5 × V _{CC}

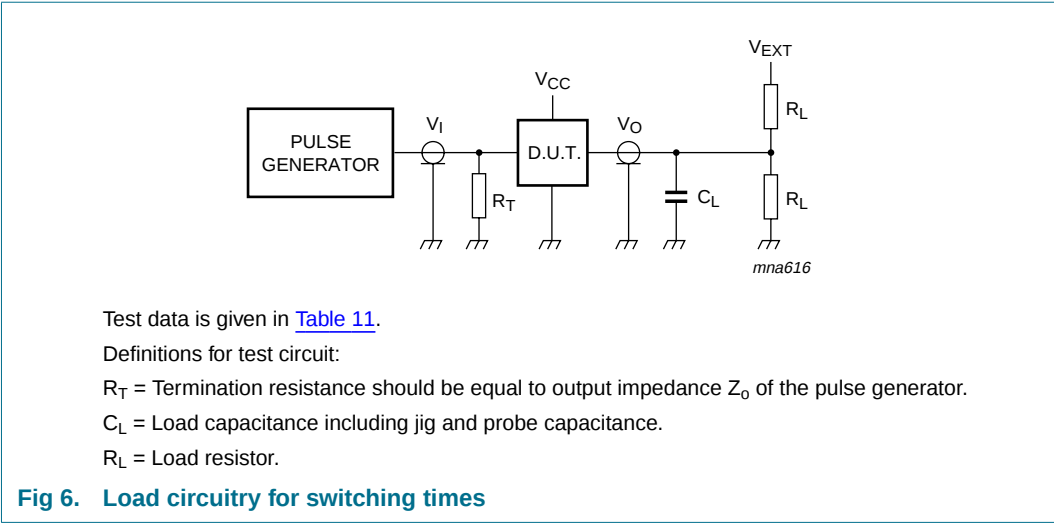


Table 11: Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	$\leq 2.0 \text{ ns}$	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	$\leq 2.0 \text{ ns}$	30 pF	500 Ω	open
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open

14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

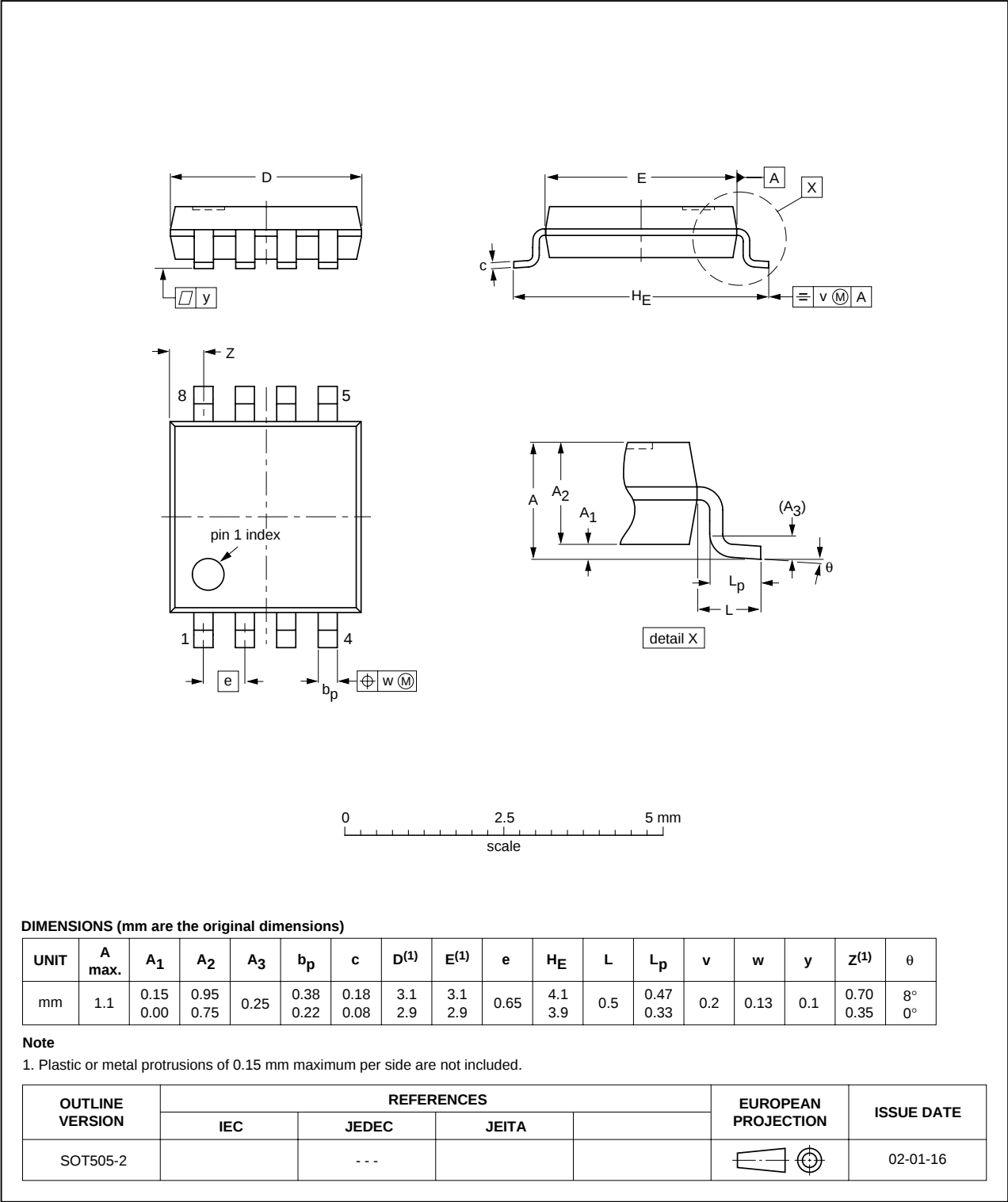
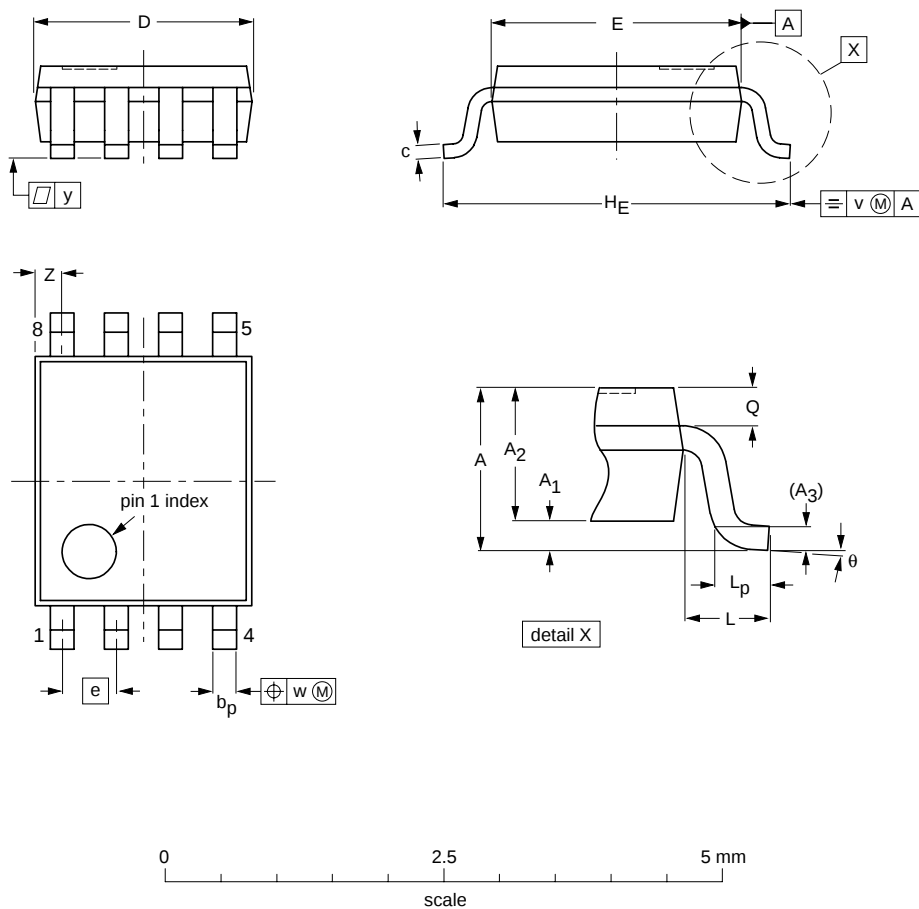


Fig 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

- Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 8. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm SOT833-1

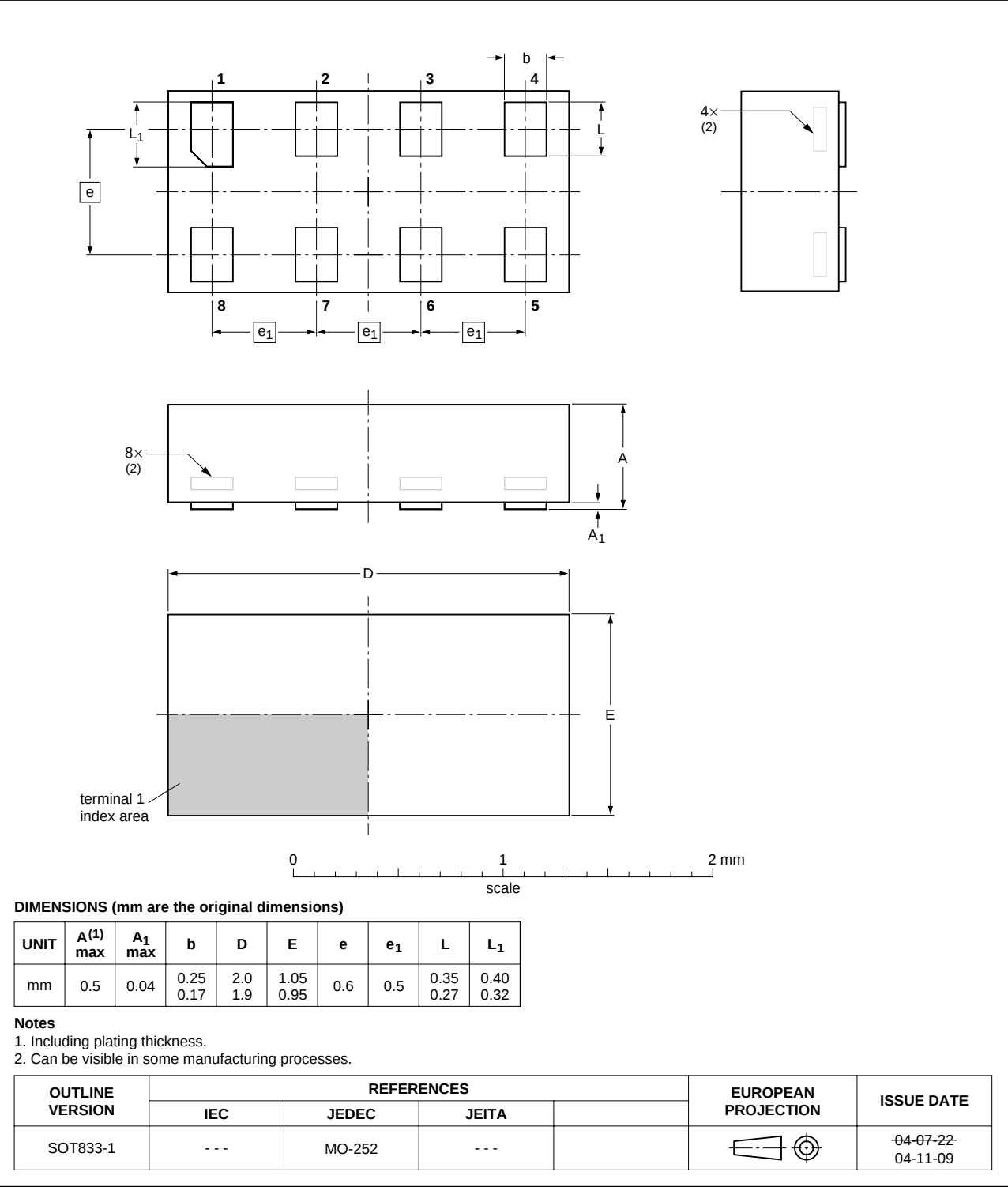


Fig 9. Package outline SOT833-1 (XSON8)

15. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC3G34_3	20050131	Product data sheet	-	9397 750 14545	74LVC3G34_2
Modifications: • Changed: type number 74LVC3G34GT.					
74LVC3G34_2	20041027	Product data sheet	-	9397 750 13794	74LVC3G34_1
74LVC3G34_1	20040429	Product data sheet	-	9397 750 13076	-

16. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 31 January 2005
Document number: 9397 750 14545

Published in The Netherlands