

ULN2003AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

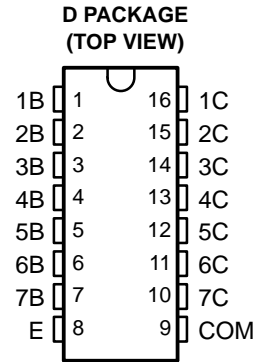
SLRS054 – JULY 2003

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

description/ordering information

The ULN2003AI is a high-voltage, high-current Darlington transistor array. This device consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULN2003AI has a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

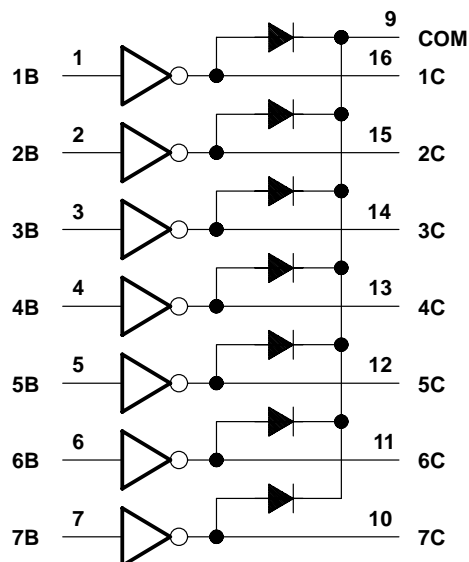


ORDERING INFORMATION

T _A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	SOIC (D)	Tube of 40	ULN2003AID
		Reel of 2500	ULN2003AIDR
			ULN2003AI

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

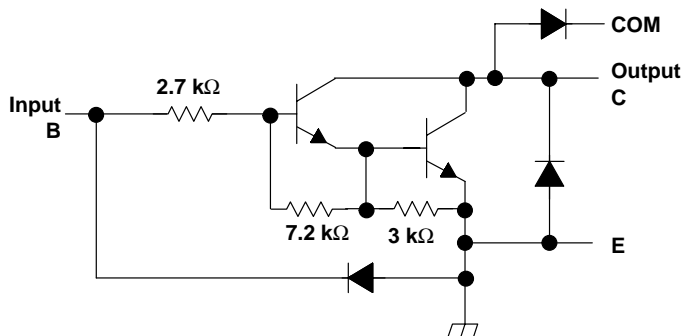
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schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)[†]

Collector-emitter voltage	50 V
Clamp diode reverse voltage (see Note 1)	50 V
Input voltage, V_I (see Note 1)	30 V
Peak collector current (see Notes 2 and 4)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	–2.5 A
Operating free-air temperature range, T_A	–40°C to 105°C
Package thermal impedance, θ_{JA} (see Notes 2 and 3)	73°C/W
Operating virtual junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

2. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(on)}$ On-state input voltage	5	$V_{CE} = 2\text{ V}$			2.4	V
					2.7	
					3	
$V_{CE(sat)}$ Collector-emitter saturation voltage	4	$I_I = 250\text{ }\mu\text{A}$, $I_C = 100\text{ mA}$		0.9	1.1	V
		$I_I = 350\text{ }\mu\text{A}$, $I_C = 200\text{ mA}$		1	1.3	
		$I_I = 500\text{ }\mu\text{A}$, $I_C = 350\text{ mA}$		1.2	1.6	
I_{CEX} Collector cutoff current	1	$V_{CE} = 50\text{ V}$, $I_I = 0$			50	μA
V_F Clamp forward voltage	7	$I_F = 350\text{ mA}$		1.7	2	V
$I_{I(off)}$ Off-state input current	2	$V_{CE} = 50\text{ V}$, $I_C = 500\text{ }\mu\text{A}$	50	65		μA
I_I Input current	3	$V_I = 3.85\text{ V}$		0.93	1.35	mA
I_R Clamp reverse current	6	$V_R = 50\text{ V}$			50	μA
C_i Input capacitance		$V_I = 0$, $f = 1\text{ MHz}$		15	25	pF



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electrical characteristics, $T_A = -40^\circ\text{C}$ to 105°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{I(on)}	On-state input voltage	5	V _{CE} = 2 V	I _C = 200 mA			2.7	V
				I _C = 250 mA			2.9	
				I _C = 300 mA			3	
V _{CE(sat)}	Collector-emitter saturation voltage	4	I _I = 250 μA, I _C = 100 mA			0.9	1.2	V
			I _I = 350 μA, I _C = 200 mA			1	1.4	
			I _I = 500 μA, I _C = 350 mA			1.2	1.7	
I _{CEX}	Collector cutoff current	1	V _{CE} = 50 V, I _I = 0				100	μA
V _F	Clamp forward voltage	7	I _F = 350 mA			1.7	2.3	V
I _{I(off)}	Off-state input current	2	V _{CE} = 50 V, I _C = 500 μA			65		μA
I _I	Input current	3	V _I = 3.85 V			0.93	1.35	mA
I _R	Clamp reverse current	6	V _R = 50 V				100	
C _i	Input capacitance		V _I = 0, f = 1 MHz			15	25	pF

switching characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	See Figure 8		0.25	1	μs
t_{PHL} Propagation delay time, high- to low-level output	See Figure 8		0.25	1	μs
V_{OH} High-level output voltage after switching	$V_S = 50\text{ V}$, See Figure 9 $I_O \approx 300\text{ mA}$,	$V_S - 20$			mV

switching characteristics, $T_A = -40^\circ\text{C}$ to 105°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	See Figure 8		1	10	μs
t_{PHL} Propagation delay time, high- to low-level output	See Figure 8		1	10	μs
V_{OH} High-level output voltage after switching	$V_S = 50\text{ V}$, See Figure 9 $I_O \approx 300\text{ mA}$,	$V_S - 50$			mV

PARAMETER MEASUREMENT INFORMATION

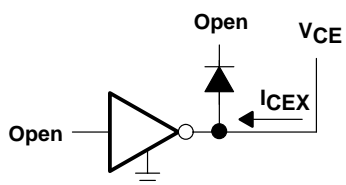


Figure 1. I_{CEX} Test Circuit

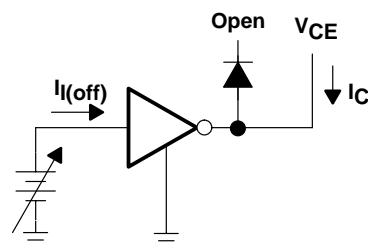


Figure 2. $I_{I(off)}$ Test Circuit

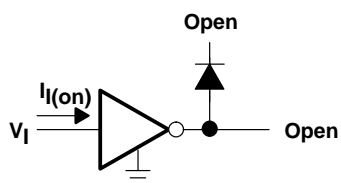
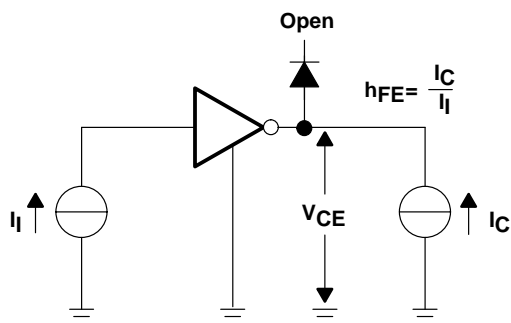


Figure 3. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

Figure 4. h_{FE} , $V_{CE(sat)}$ Test Circuit

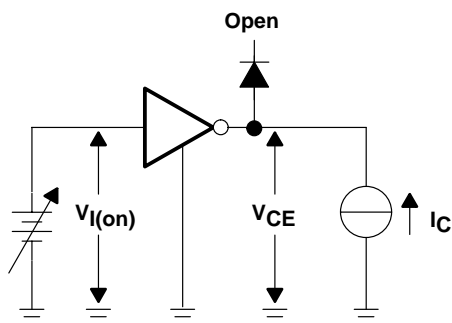


Figure 5. $V_{I(on)}$ Test Circuit

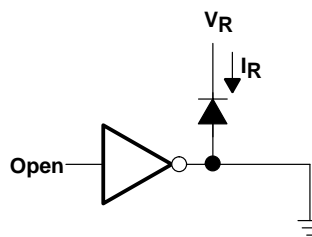


Figure 6. I_R Test Circuit

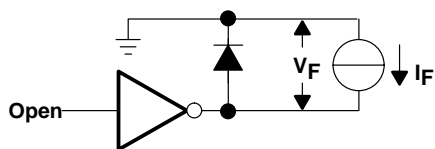


Figure 7. V_F Test Circuit

PARAMETER MEASUREMENT INFORMATION

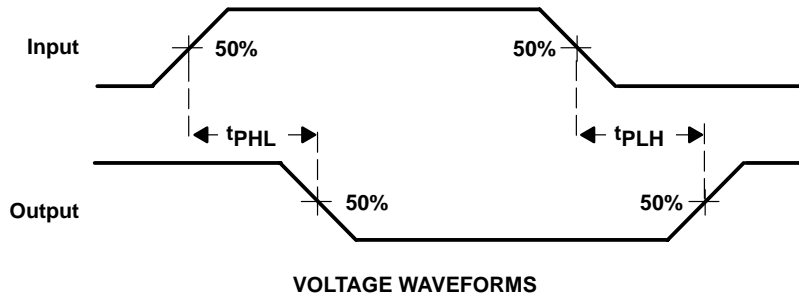
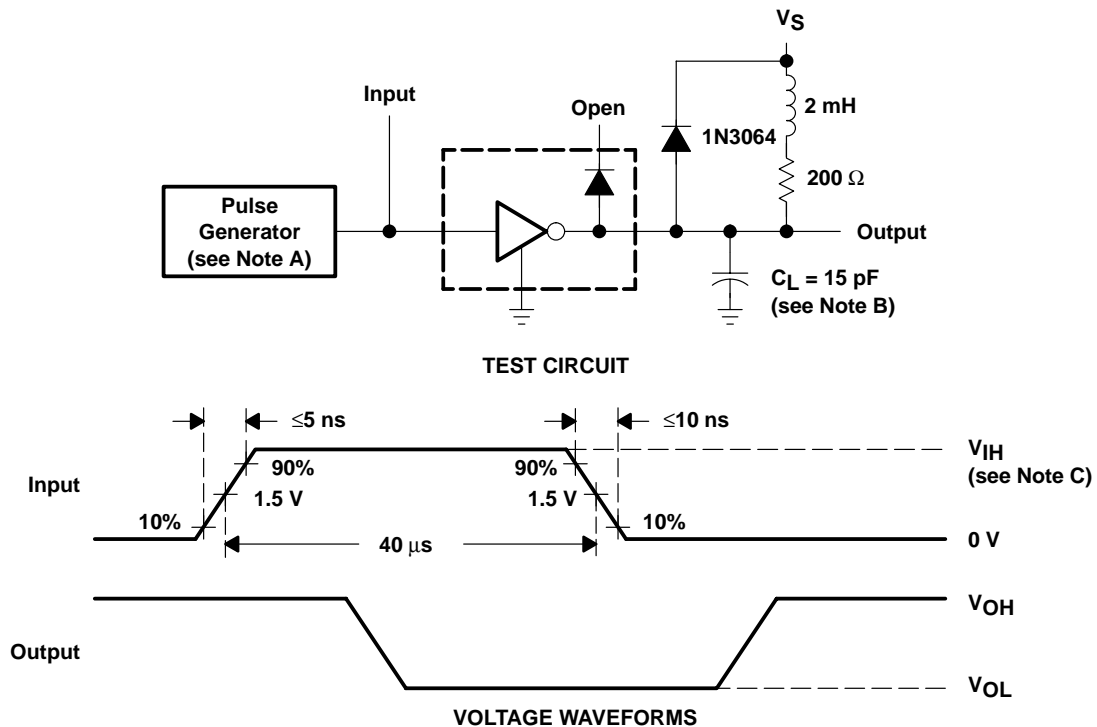


Figure 8. Propagation Delay-Time Waveforms



- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.
C. For testing, $V_{IH} = 3 \text{ V}$.

Figure 9. Latch-Up Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
COLLECTOR CURRENT
(ONE DARLINGTON)

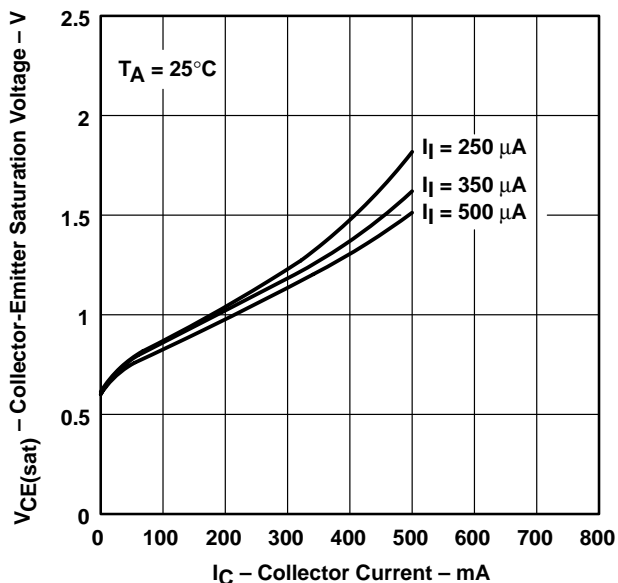


Figure 10

COLLECTOR-EMITTER
SATURATION VOLTAGE
vs
TOTAL COLLECTOR CURRENT
(TWO DARLINGTONS IN PARALLEL)

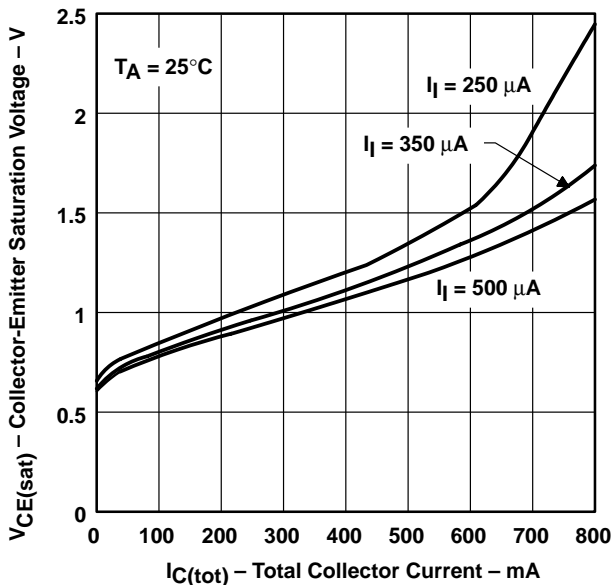


Figure 11

COLLECTOR CURRENT
vs
INPUT CURRENT

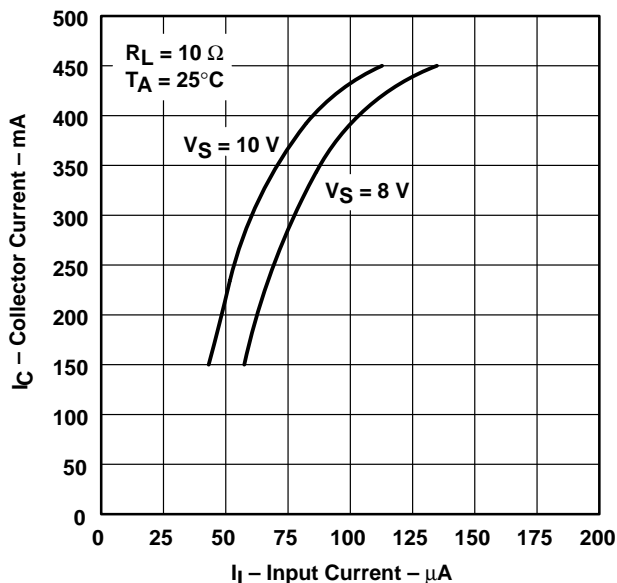


Figure 12

APPLICATION INFORMATION

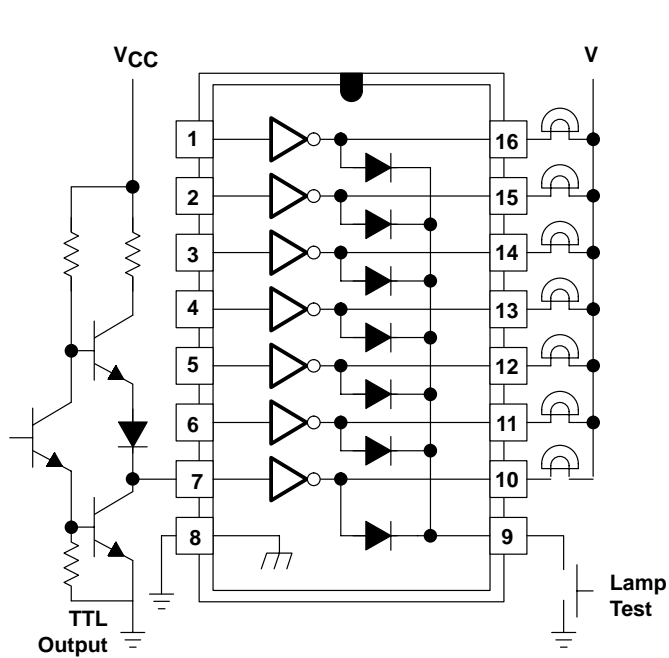
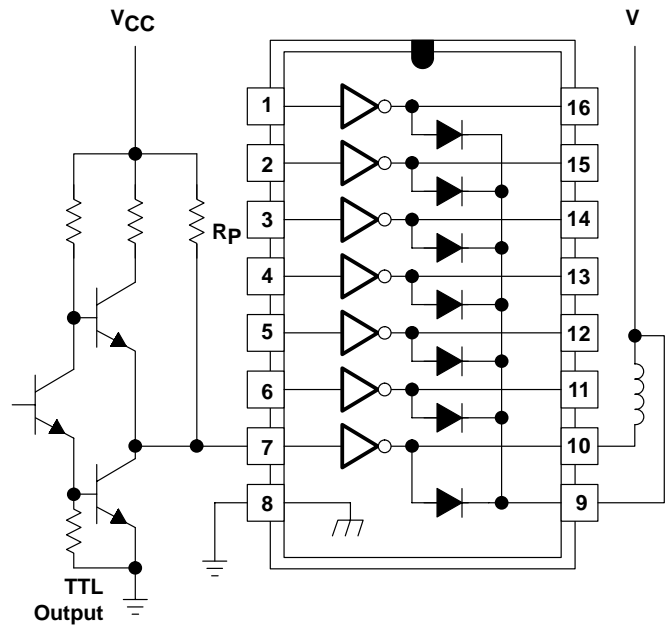
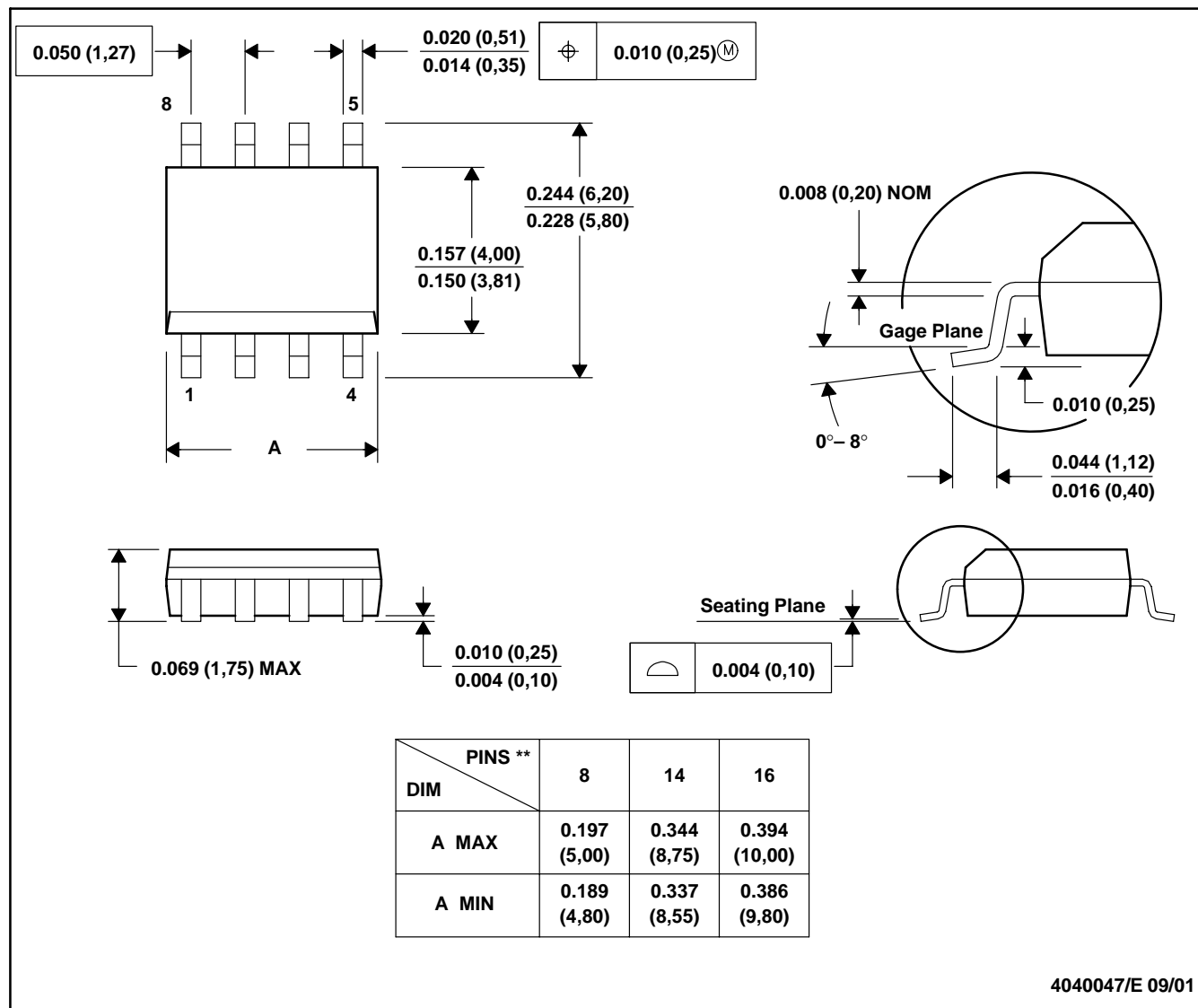


Figure 13. TTL to Load



**Figure 14. Use of Pullup Resistors
to Increase Drive Current**

D (R-PDSO-G)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

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