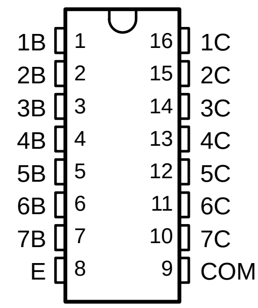
- **500-mA-Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay-Driver Applications**

D PACKAGE
(TOP VIEW)



description/ordering information

The ULN2003AI is a high-voltage, high-current Darlington transistor array. This device consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

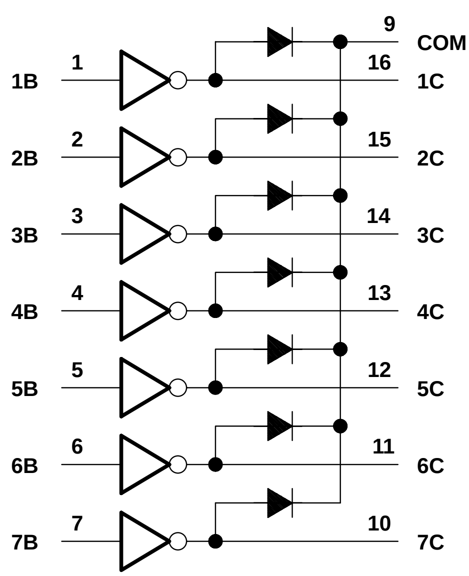
The ULN2003AI has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	SOIC (D)	Tube of 40	ULN2003AID	ULN2003AI
		Reel of 2500	ULN2003AIDR	

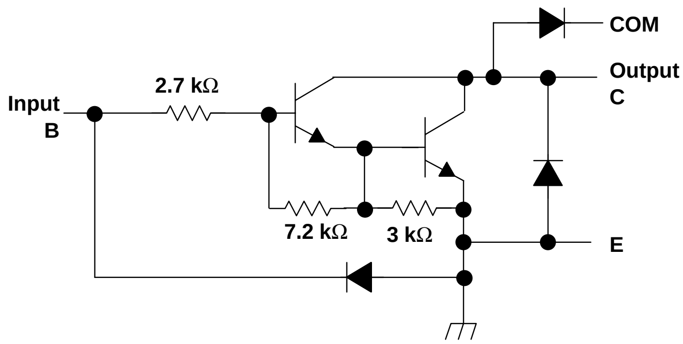
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage . . . . 50 V
Clamp diode reverse voltage (see Note 1) . . . . 50 V
Input voltage, V_I (see Note 1) . . . . 30 V
Peak collector current (see Notes 2 and 4) . . . . 500 mA
Output clamp current, I_{OK} . . . . 500 mA
Total emitter-terminal current . . . . –2.5 A
Operating free-air temperature range, T_A . . . . –40°C to 105°C
Package thermal impedance, θ_{JA} (see Notes 2 and 3) . . . . 73°C/W
Operating virtual junction temperature, T_J . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V	I_C = 200 mA			2.4	V
				I_C = 250 mA			2.7	
				I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	4	I_I = 250 µA,	I_C = 100 mA		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50	µA
V_F	Clamp forward voltage	7	I_F = 350 mA			1.7	2	V
$I_{I(off)}$	Off-state input current	2	V_{CE} = 50 V,	I_C = 500 µA,	50	65		µA
I_I	Input current	3	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	6	V_R = 50 V				50	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

electrical characteristics, T_A = –40°C to 105°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V	I_C = 200 mA			2.7	V
				I_C = 250 mA			2.9	
				I_C = 300 mA			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	4	I_I = 250 µA,	I_C = 100 mA		0.9	1.2	V
			I_I = 350 µA,	I_C = 200 mA		1	1.4	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.7	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			100	µA
V_F	Clamp forward voltage	7	I_F = 350 mA			1.7	2.3	V
$I_{I(off)}$	Off-state input current	2	V_{CE} = 50 V,	I_C = 500 µA		65		µA
I_I	Input current	3	V_I = 3.85 V			0.93	1.35	mA
I_R	Clamp reverse current	6	V_R = 50 V				100	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25	pF

switching characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 8		0.25	1	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 8		0.25	1	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA, See Figure 9	V_S–20			mV

switching characteristics, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 8		1	10	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 8		1	10	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA, See Figure 9	V_S–50			mV

PARAMETER MEASUREMENT INFORMATION

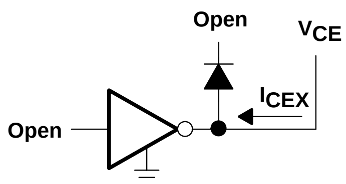


Figure 1. I_{CEX} Test Circuit

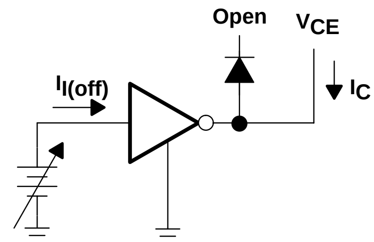


Figure 2. $I_{I(off)}$ Test Circuit

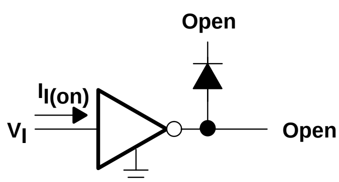
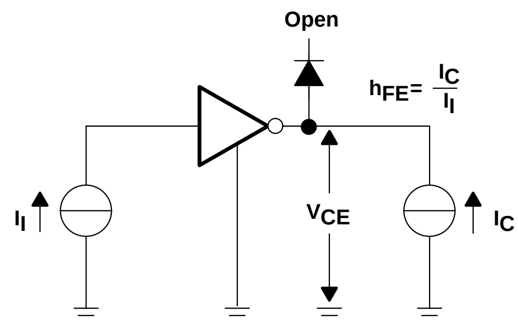


Figure 3. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 4. h_{FE}, $V_{CE(sat)}$ Test Circuit

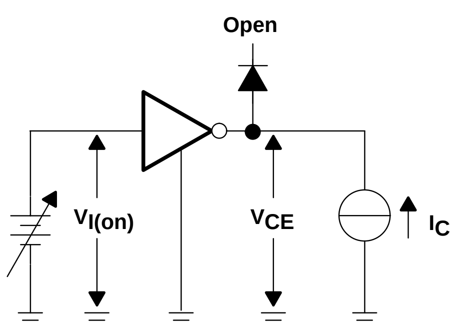


Figure 5. $V_{I(on)}$ Test Circuit

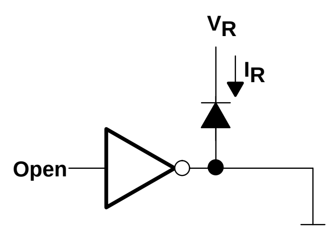


Figure 6. I_R Test Circuit

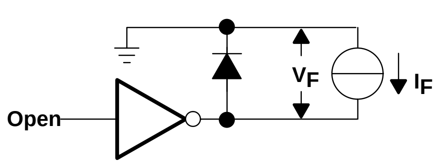
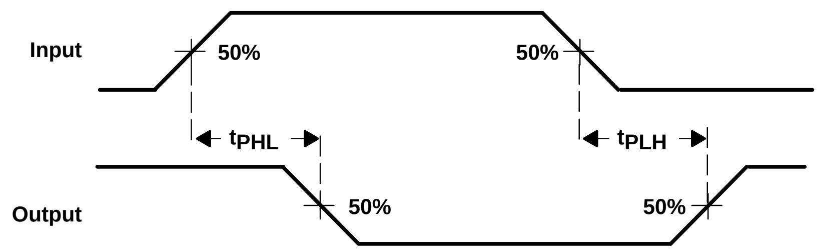


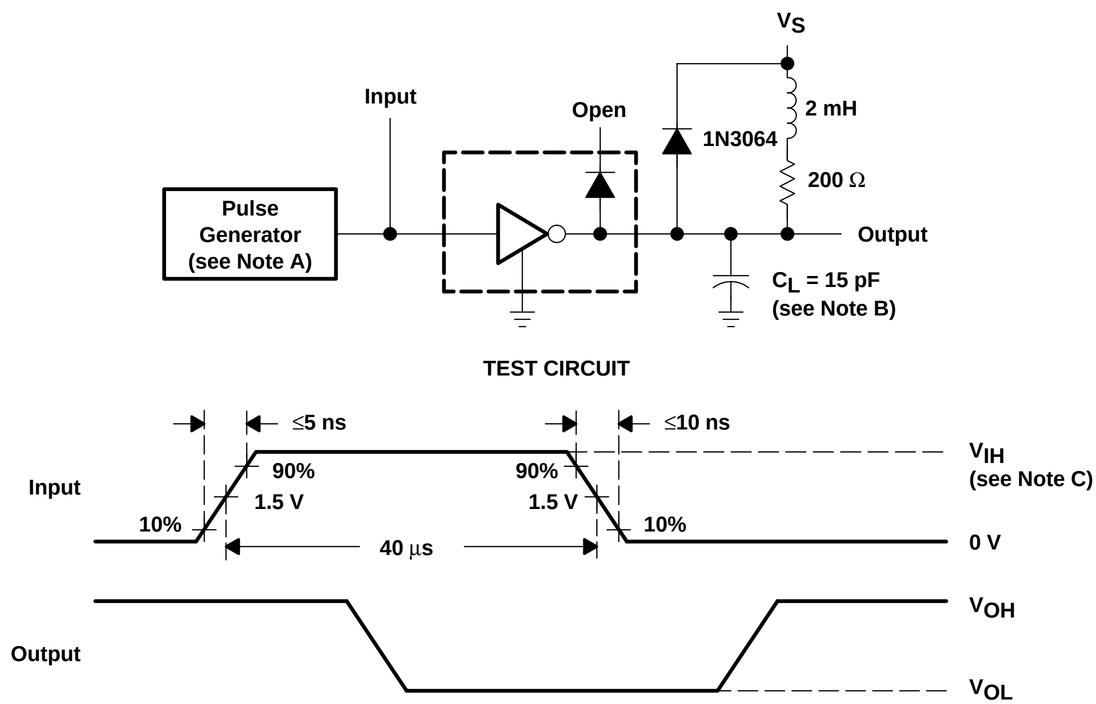
Figure 7. V_F Test Circuit

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

Figure 8. Propagation Delay-Time Waveforms



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing , V_{IH} = 3 V.

Figure 9. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

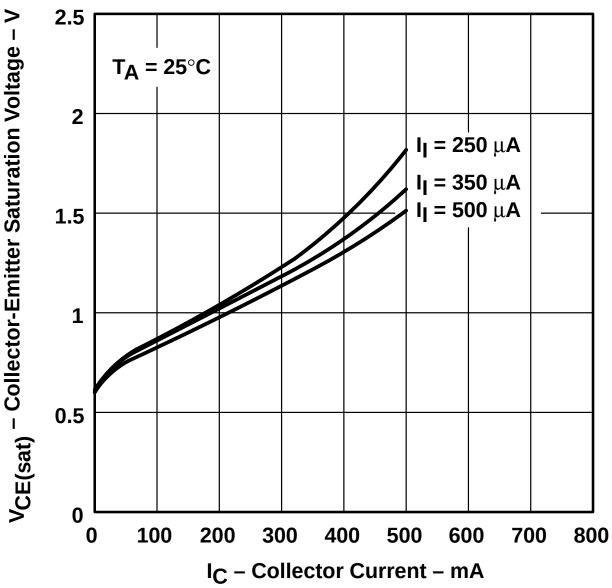


Figure 10

COLLECTOR-EMITTER SATURATION VOLTAGE vs TOTAL COLLECTOR CURRENT (TWO DARLINGTONS IN PARALLEL)

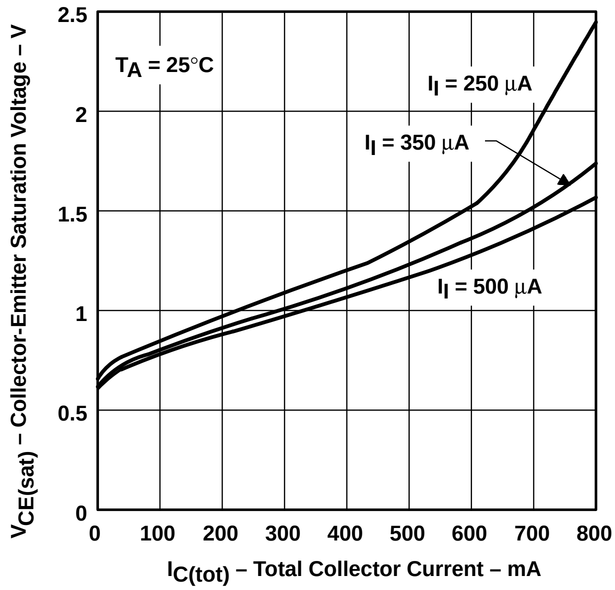


Figure 11

COLLECTOR CURRENT vs INPUT CURRENT

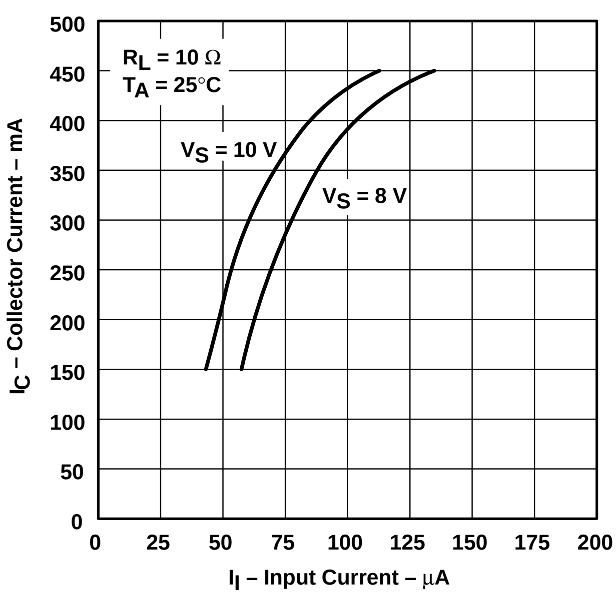


Figure 12

APPLICATION INFORMATION

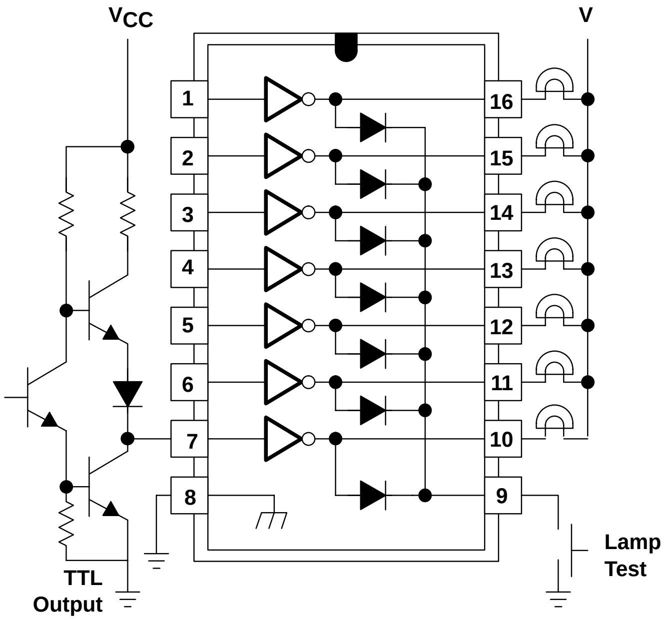


Figure 13. TTL to Load

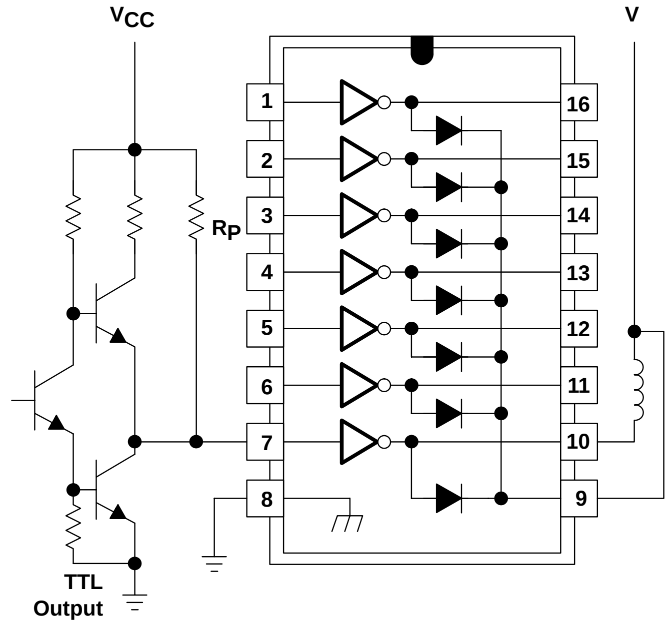
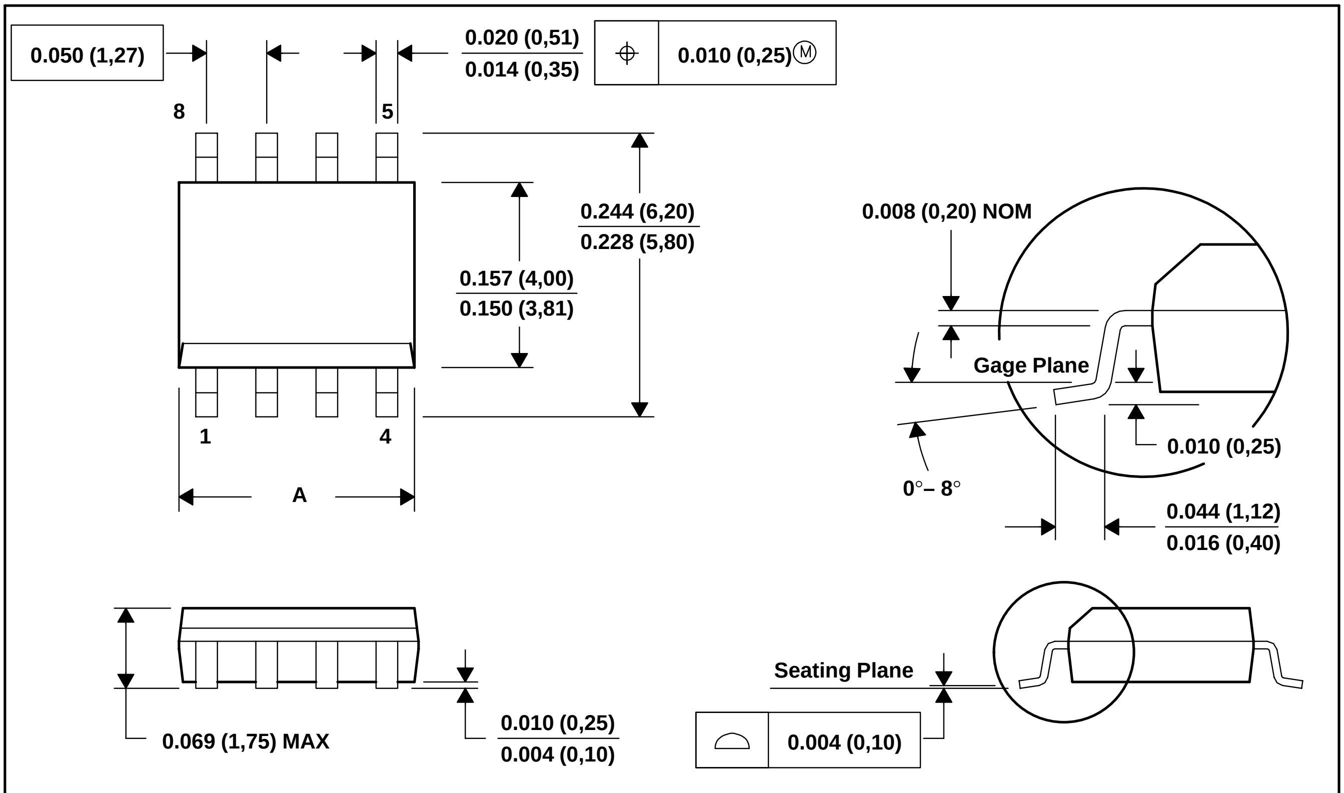


Figure 14. Use of Pullup Resistors to Increase Drive Current

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012