



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SYMBOL	TEMPERATURE RANGE, T _A	ORDERING NUMBER	TRANSPORT MEDIA
THS7530	TSSOP PowerPAD	PWP-14	THS7530	-40°C to 85°C	THS7530PWP	Tube
					THS7530PWPR	Tape and reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		THS7530
Supply voltage, V _{S+} – V _{S-}		5.5 V
Input voltage, V _I		±V _S
Output current, I _O (2)		65 mA
Differential input voltage, V _{ID}		±4 V
Continuous power dissipation		See Dissipation Rating Table
Maximum junction temperature, T _J		150°C
Maximum junction temperature for long term stability, T _J		125°C
Operating free-air temperature range, T _A		-40°C to 85°C
Storage temperature range, T _{stg}		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
ESD	HBM	3000 V
	CDM	1500 V
	MM	200 V

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The THS7530 incorporates a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage, [V _{S-} to V _{S+}]		4.5	5	5.5	V
Operating free-air temperature, T _A		-40		85	°C
Input common mode voltage	[V _{S-} to V _{S+}] = 5 V		2.5		V
Output common mode voltage	[V _{S-} to V _{S+}] = 5 V		2.5		V

PACKAGE THERMAL DATA

PACKAGE	PCB	θ _{JA} (C/W)	θ _{JC} (C/W)	T _A = 25°C POWER RATING
14PWP	See <i>Layout Considerations</i> in the application section of this data sheet.	37.5	2.07	3 W

PowerPAD is a trademark of Texas Instruments.

SPECIFICATIONS: MAIN AMPLIFIER

$V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $V_{OCM} = 2.5\text{ V}$, $V_{ICM} = 2.5\text{ V}$, $V_{G-} = 0\text{ V}$, $V_{G+} = 1\text{ V}$ (maximum gain), $T_A = 25^\circ\text{C}$, ac performance measured using the ac test circuit shown in Figure 1 (unless otherwise noted). DC performance is measured using the dc test circuit shown in Figure 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			
		25 C	25 C	-40 C to 85 C	UNITS	MIN/MAX
AC PERFORMANCE (See Figure 1)						
Small-signal bandwidth	All gains, $P_{IN} = -45\text{ dBm}$	300			MHz	Typ
Slew rate ⁽¹⁾	1 V_{PP} Step, 25% to 75%, minimum gain	1250			V/ μs	Typ
Settling time to 1% ⁽¹⁾	1 V_{PP} Step, minimum gain	11			ns	Typ
Harmonic distortion	$V_{O(PP)} = 1\text{ V}$, $R_{L(diff)} = 400\ \Omega$					
2 nd Harmonic	$f = 32\text{ MHz}$	-65			dBc	Typ
3 rd Harmonic	$f = 32\text{ MHz}$	-61			dBc	Typ
Third-order intermodulation distortion	$P_O = -10\text{ dBm}$ each tone, $f_C = 70\text{ MHz}$, 200 kHz tone spacing	-62			dBc	Typ
Third-order output intercept point	$f_C = 70\text{ MHz}$, 200 kHz tone spacing	21			dBm	Typ
Noise figure (with input termination)	Source impedance: $50\ \Omega$	9			dB	Typ
Total input voltage noise	$f > 100\text{ kHz}$	1.1			nV/ $\sqrt{\text{Hz}}$	Typ
DC PERFORMANCE—INPUTS (See Figure 2)						
Input bias current		20	39	40	μA	Max
Input bias current offset		<150			pA	Typ
Minimum input voltage	Minimum gain	1.5	1.6	1.7	V	Max
Maximum input voltage	Minimum gain	3.5	3.35	3.2	V	Min
Common-mode rejection ratio		114	56	44	dB	Min
Differential input impedance		$8.5\ \parallel\ 3.0$			$\text{k}\Omega\ \parallel\ \text{pF}$	Typ
DC PERFORMANCE—OUTPUTS (See Figure 2)						
Output offset voltage	All gains	± 100	± 340	± 480	mV	Max
Maximum output voltage high		3.5	3.275	3.25	V	Min
Minimum output voltage low		1.5	1.7	1.8	V	Max
Output current		± 37	± 16	± 16	mA	Min
Output impedance		15			Ω	Typ
OUTPUT COMMON-MODE VOLTAGE CONTROL (See Figure 2)						
Small-signal bandwidth		32			MHz	Typ
Gain		1.00			V/V	Typ
Common-mode offset voltage		4.5	12	13.8	mV	Max
Minimum input voltage		1.75			V	Typ
Maximum input voltage		3.25			V	Typ
Input impedance		$25\ \parallel\ 1$			$\text{k}\Omega\ \parallel\ \text{pF}$	Typ
Default voltage, with no connect		2.5			V	Typ
Input bias current		<1			μA	Typ

(1) Slew rate and settling time measured at amplifier output.

SPECIFICATIONS: MAIN AMPLIFIER (CONTINUED)

$V_{S+} = 5\text{ V}$, $V_{S-} = 0\text{ V}$, $V_{OCM} = 2.5\text{ V}$, $V_{ICM} = 2.5\text{ V}$, $V_{G-} = 0\text{ V}$, $V_{G+} = 1\text{ V}$ (maximum gain), $T_A = 25^\circ\text{C}$, ac performance measured using the ac test circuit shown in Figure 1 (unless otherwise noted). DC performance is measured using the dc test circuit shown in Figure 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE			
		25 C	25 C	-40 C to 85 C	UNITS	MIN/MAX
GAIN CONTROL (See Figure 2)						
Gain control differential voltage range	V_{G+}	0 to 1			V	Typ
Minus gain control voltage	$V_{G-} - V_{S-}$	-0.6 to 0.8			V	Typ
Minimum gain	$V_{G+} = 0\text{ V}$	11.6			dB	Typ
Maximum gain	$V_{G+} = 0.9\text{ V}$	46.5			dB	Typ
Gain slope	$V_{G+} = 0\text{ V to } 0.9\text{ V}$	38.8			dB/V	Typ
Gain slope variation	$V_{G+} = 0\text{ V to } 0.9\text{ V}$	± 1.5			dB/V	Typ
Gain error	$V_{G+} = 0\text{ V to } 0.15\text{ V}$	± 4			dB	Typ
	$V_{G+} = 0.15\text{ V to } 0.9\text{ V}$	± 2.25			dB	Typ
Gain control input bias current		<1			μA	Typ
Gain control input resistance		40			k Ω	Typ
Gain control bandwidth	Small signal -3 dB	15			MHz	Typ
VOLTAGE CLAMPING (See Figure 2)						
Output voltages ($V_{OUT\pm}$) relative to clamp voltages ($V_{CL\pm}$)	In voltage limiting mode	± 25	± 38	± 60	mV	Max
$V_{CL\pm}$ input resistance		3.3			k Ω	Typ
$V_{CL\pm}$ voltage limits		V_{S-} to V_{S+}			V	Typ
POWER SUPPLY (See Figure 2)						
Specified operating voltage		5	5.5	5.5	V	Max
Maximum quiescent current		40	48	49	mA	Max
Power supply rejection ($\pm\text{PSRR}$)		77	70	45	dB	Min
POWERDOWN (See Figure 2)						
Enable voltage threshold	TTL low = normal operation	1.4		1.0	V	Min
Disable voltage threshold	TTL high = shut down	1.4		1.65	V	Max
Power-down quiescent current		0.35	0.4	0.45	mA	Max
Input current high		9	16	19	μA	Max
Input current low		109	116	119	μA	Max
Input impedance		50 1			k Ω pF	Typ
Turnon time delay	Measured to 50% quiescent current	820			ns	Typ
Turnoff time delay		500			ns	Typ
Forward isolation in power down		80			dB	Typ
Input resistance in power down		> 1			M Ω	Typ
Output resistance in power down		16			k Ω	Typ

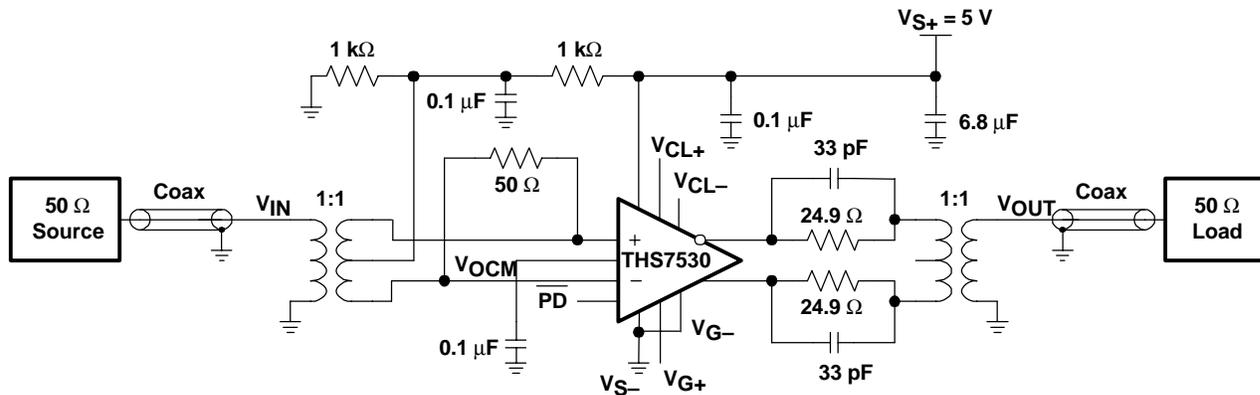


Figure 1. AC Test Circuit

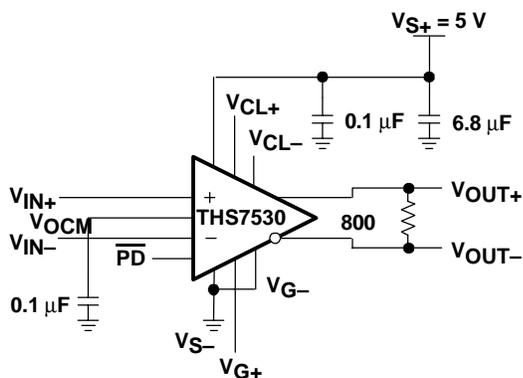
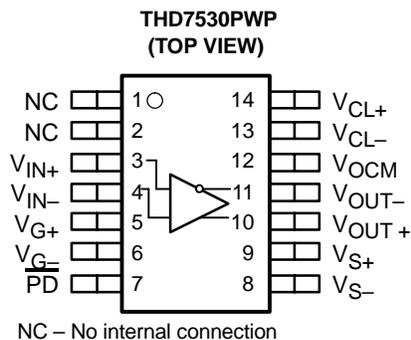


Figure 2. DC Test Circuit

PIN ASSIGNMENTS



Terminal Functions

TERMINAL		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	NC	No internal connection
3	V _{IN+}	Noninverting amplifier input
4	V _{IN-}	Inverting amplifier input
5	V _{G+}	Gain setting positive input
6	V _{G-}	Gain setting negative input
7	$\overline{\text{PD}}$	Powerdown, $\overline{\text{PD}}$ = logic low puts part into low power mode, $\overline{\text{PD}}$ = logic high or open for normal operation
8	V _{S-}	Negative amplifier power supply input
9	V _{S+}	Positive amplifier power supply input
10	V _{OUT+}	Noninverted amplifier output
11	V _{OUT-}	Inverted amplifier output
12	V _{OCM}	Output common-mode voltage input
13	V _{CL-}	Output negative clamp voltage input
14	V _{CL+}	Output positive clamp voltage input

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

Measured using the ac test circuit shown in Figure 1 (unless otherwise noted).

		FIGURE
Voltage Gain to Load	vs Frequency (Input at 45 dBm)	3
Gain and Gain Error	vs V_{G+}	4
Noise Figure	vs Frequency	5
Output Intercept Point	vs Frequency	6
1-dB Compression Point	vs Frequency	7
Total Input Voltage Noise	vs Frequency	8
Intermodulation Distortion	vs Frequency	9
Harmonic Distortion	vs Frequency	10
S-Parameters	vs Frequency	11
Differential Input Impedance of Main Amplifier	vs Frequency	12
Differential Output Impedance of Main Amplifier	vs Frequency	13
V_{G+} Input Impedance	vs Frequency	14
V_{OCM} Input Impedance	vs Frequency	15
Common-Mode Rejection Ratio	vs Frequency	16
Step Response – 2 V _{pp}	vs Time	17
Step Response – Rising Edge	vs Time	18
Step Response – Falling Edge	vs Time	19

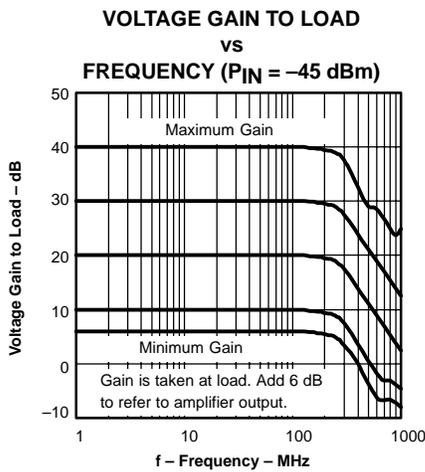


Figure 3

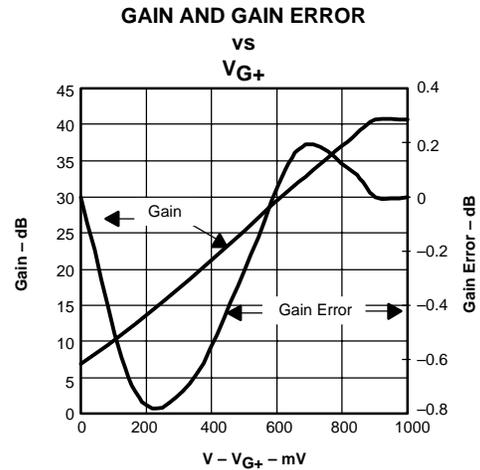


Figure 4

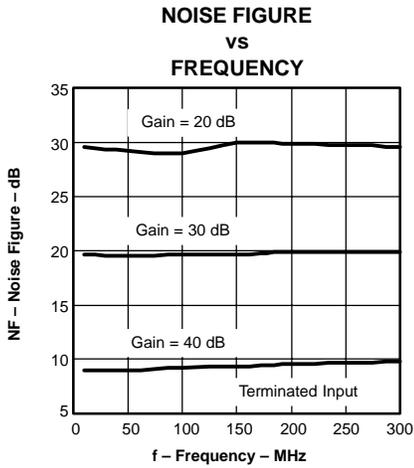


Figure 5

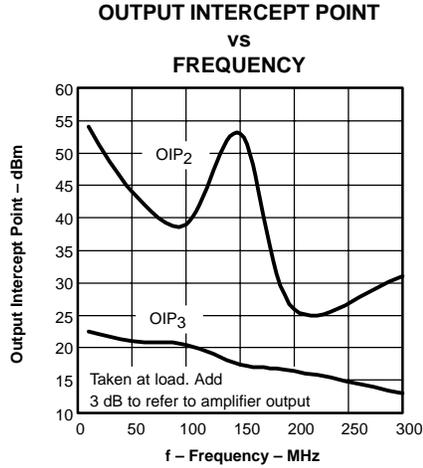


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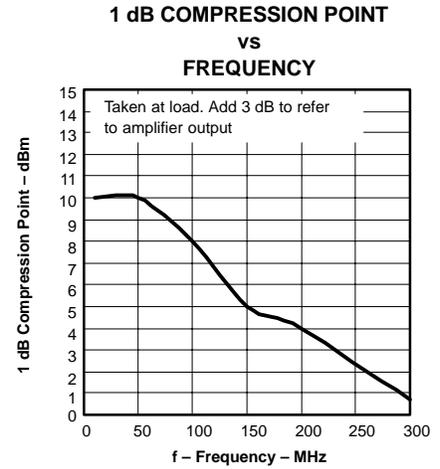


Figure 7

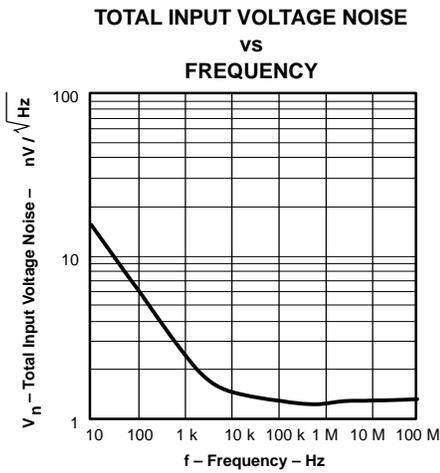


Figure 8

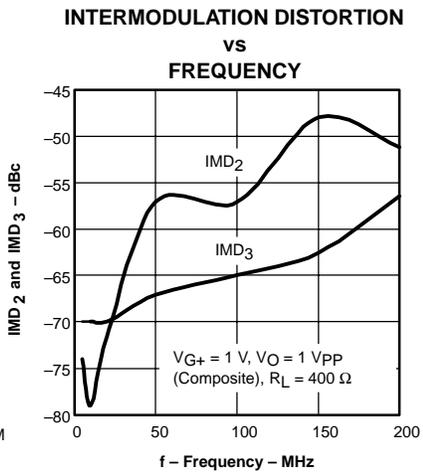


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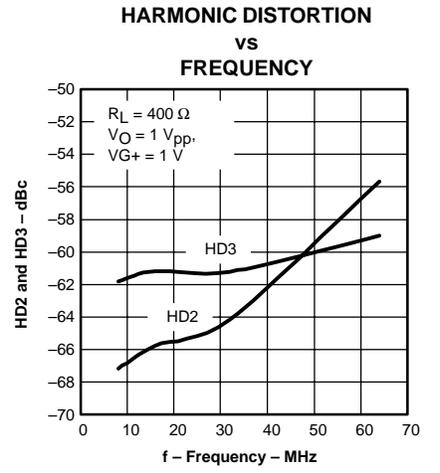


Figure 10

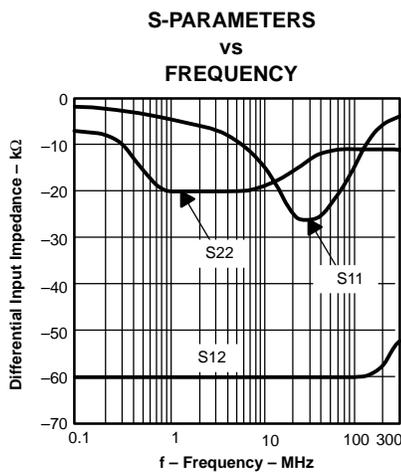


Figure 11

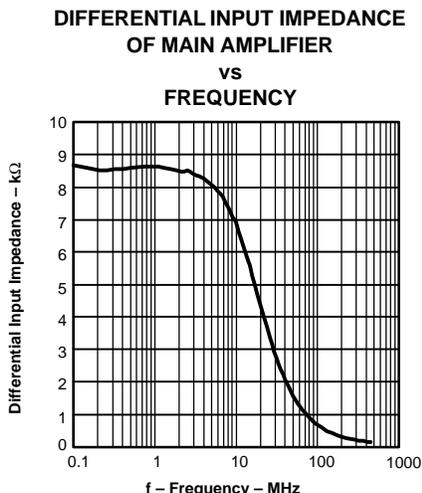


Figure 12

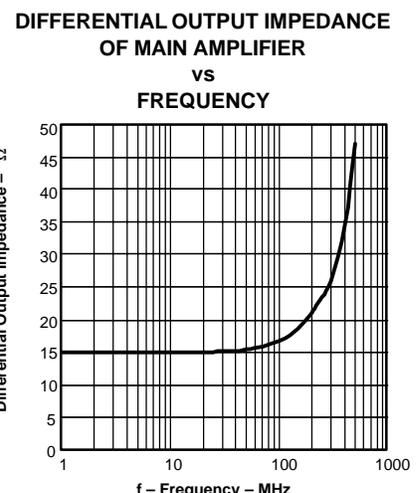


Figure 13

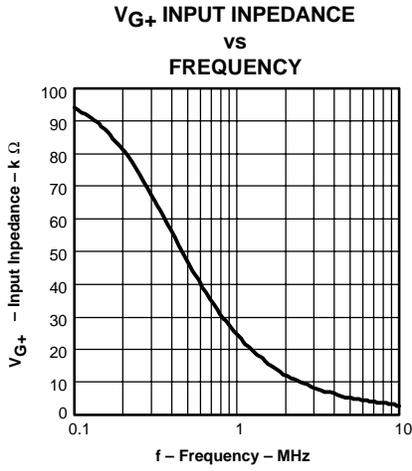


Figure 14

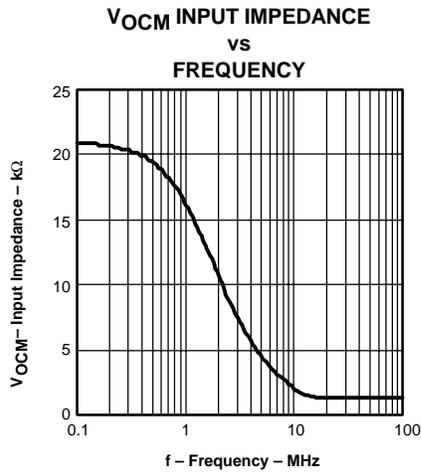


Figure 15

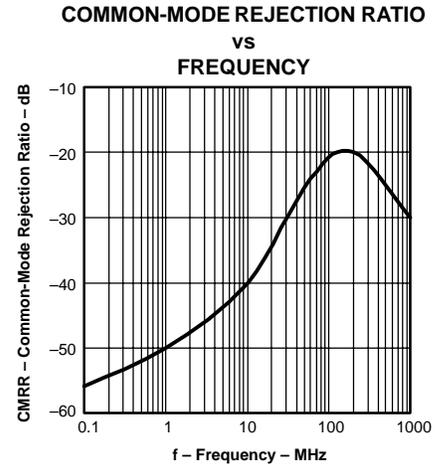


Figure 16

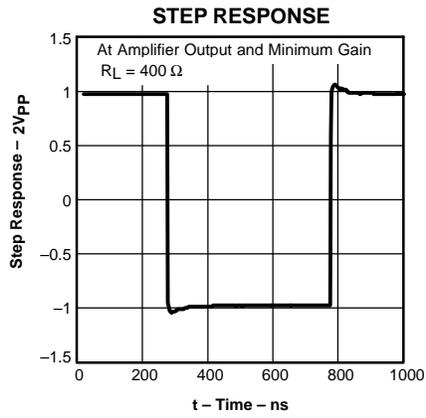


Figure 17

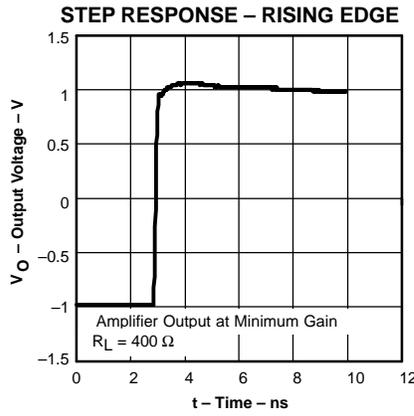


Figure 18

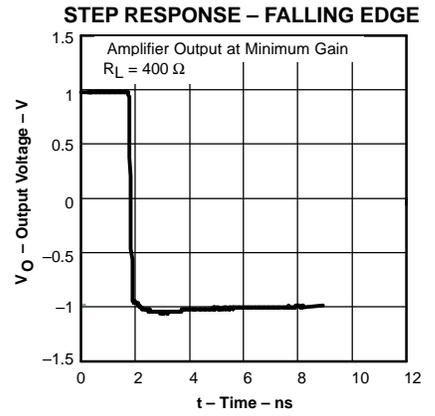


Figure 19

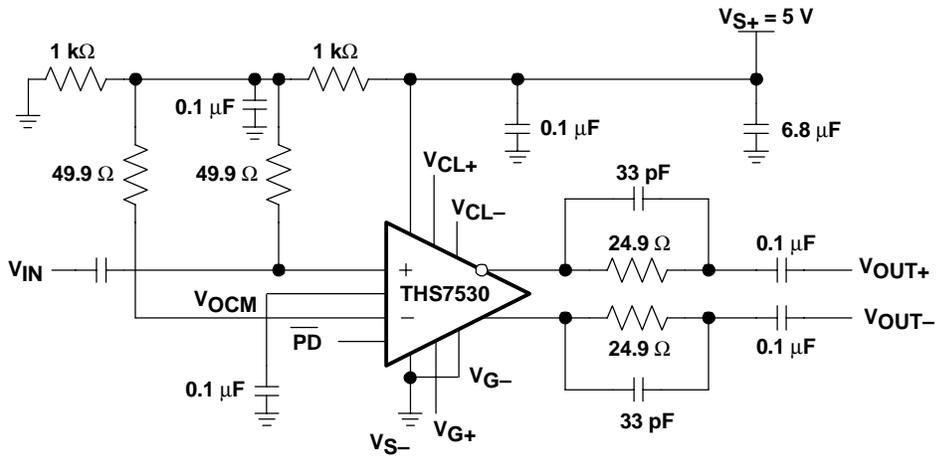


Figure 21. AC-Coupled Single-Ended Input With AC-Coupled Differential Output

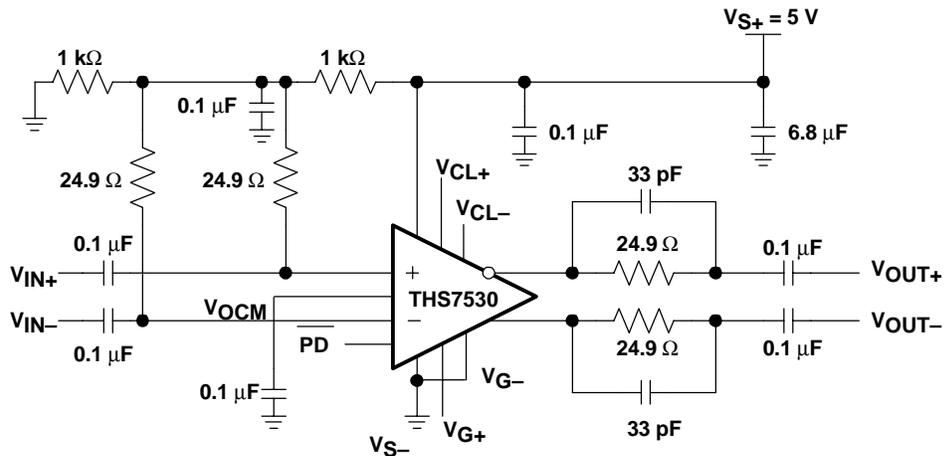


Figure 22. AC-Coupled Differential Input With AC-Coupled Differential Output

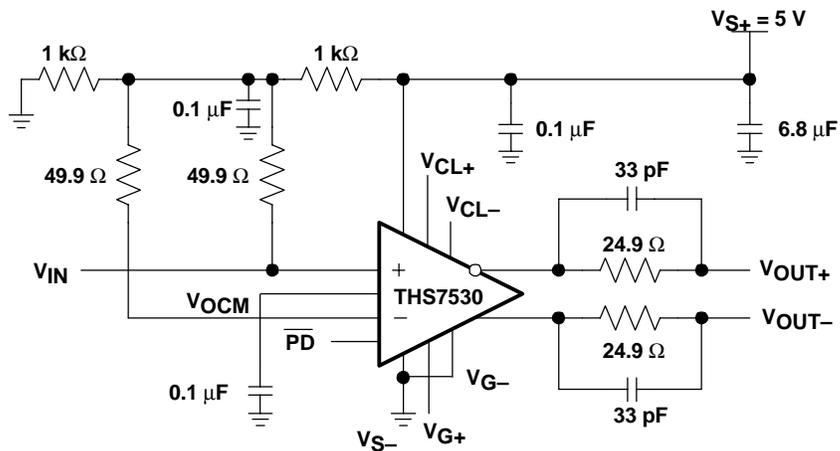


Figure 23. DC-Coupled Single-Ended Input With DC-Coupled Differential Output

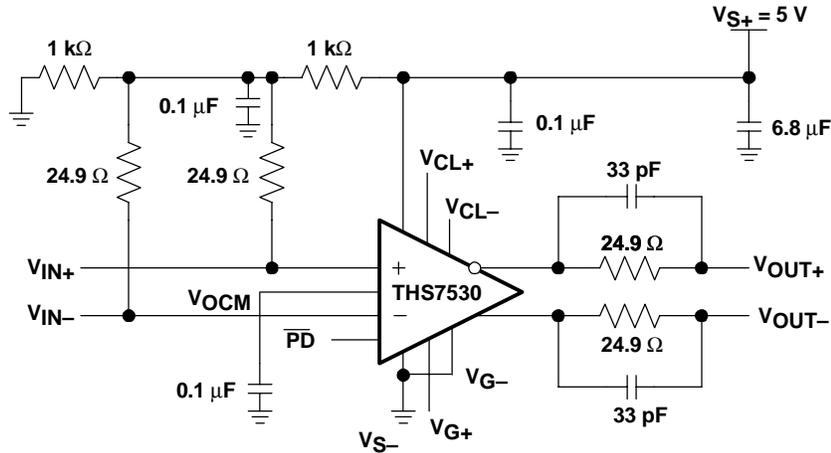


Figure 24. DC-Coupled Differential Input With DC-Coupled Differential Output

LAYOUT CONSIDERATIONS

The THS7530 comes in a thermally enhance PowerPAD™ package. Figure 25 shows the recommended number of vias and thermal land size recommended for best performance. Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solectron Texas indicate that a via drill diameter of 0.33mm (13 mils) or smaller works well when 1 ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a dimension equal to the via diameter + 0,1 mm minimum. This prevents the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB.

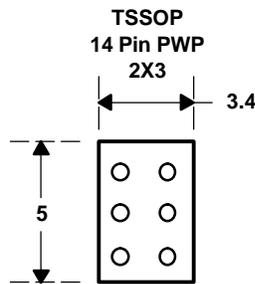


Figure 25. Recommended Thermal Land Size and Thermal Via Patterns (dimensions in mm)

See TI's Technical Brief titled PowerPAD™ Thermally Enhanced Package (SLMA002) for a detailed discussion of the PowerPAD™ package, its dimensions, and recommended use.

THEORY OF OPERATION

Figure 26 shows a simplified schematic of the THS7530.

The input architecture is a modified Gilbert Cell. The output from the Gilbert Cell is converted to a voltage and buffered to the output as a fully-differential signal. A summing node between the outputs is used to compare the output common-mode voltage to the V_{OCM} input. The V_{OCM} error amplifier then servos the output common-mode voltage to maintain it equal to the V_{OCM} input. Left unterminated, V_{OCM} is set to midsupply by internal resistors.

The gain control input is conditioned to give linear in dB gain control (block H). The gain control input is a differential signal from 0 V to 0.9 V which varies the gain from 11.6 dB to 46.5 dB.

V_{CL+} and V_{CL-} provide inputs that limit the output voltage swing of the amplifier.

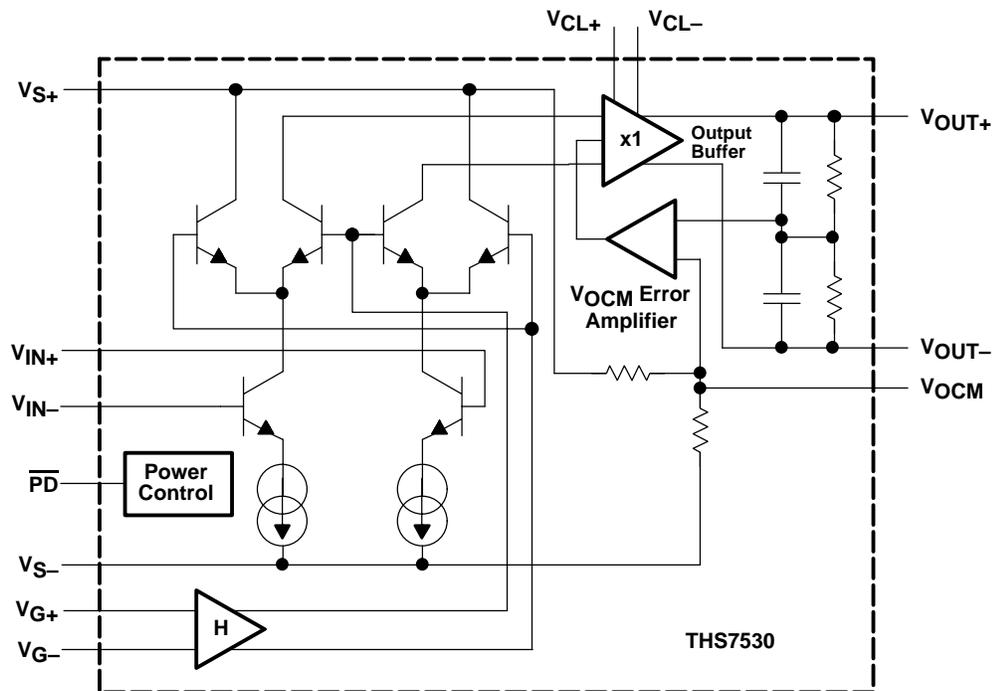


Figure 26. THS7530 Simplified Schematic

SPICE MODEL

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* THS7530 SUBCIRCUIT
 * HIGH SPEED FULLY DIFFERENTIAL VARIABLE AMPLIFIER
 * WRITTEN 11/26/02
 * VG- is tied to VS- and output clamping is not modeled

* CONNECTIONS: IN+
 * | IN-
 * | | VS+
 * | | | VS-
 * | | | | OUT-
 * | | | | | OUT+
 * | | | | | | VOVM
 * | | | | | | | VG+
 * | | | | | | | |
 .SUBCKT THS7530 1 2 3 4 5 6 7 8

* INPUT*
 Q1 122 1 101 NPN_IN 16
 Q2 123 2 102 NPN_IN 16
 R1 102 101 25
 I1 101 4 DC 4.85e-3
 I2 102 4 DC 4.85e-3

QUAD

Q3 132 120 122 NPN 16
 Q4 121 119 122 NPN 16
 Q5 132 119 123 NPN 16
 Q6 121 120 123 NPN 16
 R2 132 3 250
 R3 121 3 250

CURRENT AMP

F1 128 129 VF1 6
 VF1 132 121 0V

Z NODE

R4 128 129 2k
 I3 129 4 DC 0.75e-3
 I4 128 4 DC 0.75e-3
 V9 128 328 0.7
 V10 129 329 0.7

FREQUENCY SHAPING

E3 131 0 329 0 1
 R5 131 140 30
 L3 140 133 7.5n
 C6 133 0 24p
 E4 130 0 328 0 1
 R9 130 141 30
 L4 141 125 10n
 C7 125 0 27p

OUTPUT BUFFER

Q9 4 133 117 PNP 5.12
 Q10 3 133 127 NPN 5.12
 Q11 3 117 134 NPN 81.92
 Q12 4 127 135 PNP 81.92
 Q13 4 125 116 PNP 5.12
 Q14 3 125 126 NPN 5.12
 Q15 3 116 136 NPN 81.92
 Q16 4 126 137 PNP 81.92
 R6 138 134 5
 R7 135 138 5
 R10 139 136 5
 R11 137 139 5
 I5 3 117 DC 0.4e-3
 I6 127 4 DC 0.4e-3
 I7 3 116 DC 0.4e-3
 I8 126 4 DC 0.4e-3

OUTPUT Z

R8 113 138 2
R12 115 139 2
L1 113 5 4n
L2 115 6 4n
C1 6 5 2p

*VOCM

Rcm1 115 114 8k
Ccm1 115 114 0.1p
Rcm2 114 113 8k
Ccm2 114 113 0.1p
E1 118 0 114 7 1e3
Rtop 3 7 50k
Rbot 4 7 50k
Q7 128 118 3 PNP 16
Q8 129 118 3 PNP 16

GAIN CONTROL

V8 235 8 0.454
E5 231 0 235 4 0.51
E6 232 0 POLY(1) 231 0 0.0 1 1 0.5 3.5
E7 233 0 232 0 0.115
E8 234 0 POLY(1) 233 0 0.0 0 1 0 0.333
E9 120 119 234 0 0.42
V7 3 120 1.6

Rsupply 3 4 310

.MODEL NPN_IN NPN

+ KF=1E-12

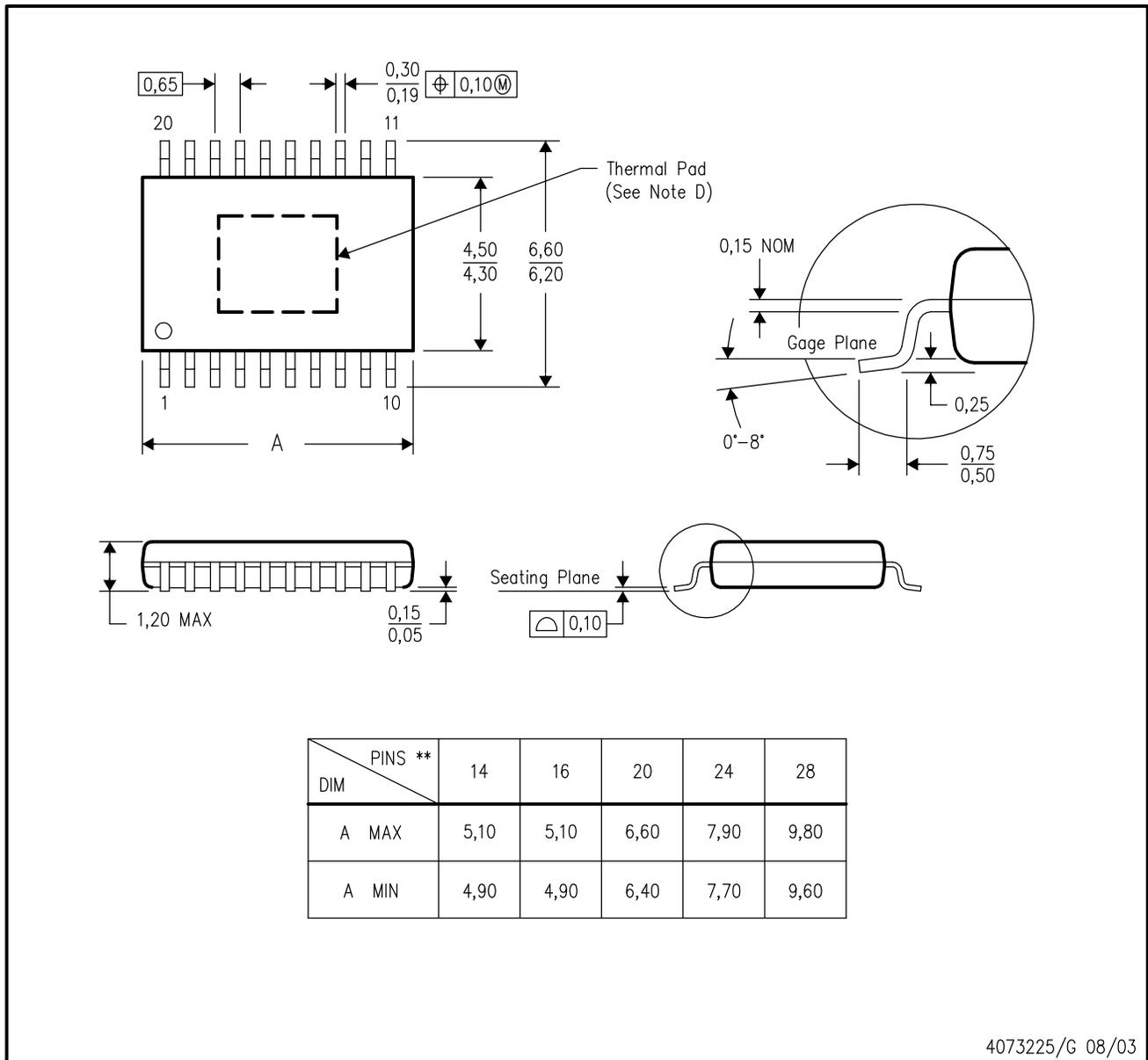
.MODEL NPN NPN

.MODEL PNP PNP

.ENDS

PWP (R-PDSO-G**) 20 PIN SHOWN

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



4073225/G 08/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MO-153

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