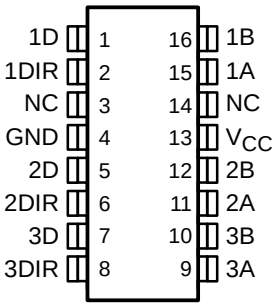
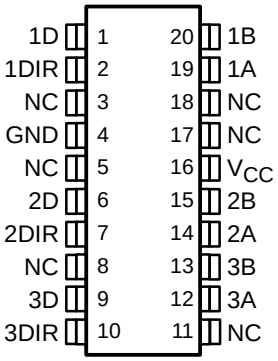
SLLS459B – NOVEMBER 2000 – REVISED FEBRUARY 2002

- **Three Differential Transceivers in One Package**
- **Signaling Rates† Up to 30 Mbps**
- **Low Power and High Speed**
- **Designed for TIA/EIA-485, TIA/EIA-422, ISO 8482, and ANSI X3.277 (HVD SCSI Fast–20) Applications**
- **Common-Mode Bus Voltage Range –7 V to 12 V**
- **ESD Protection on Bus Terminals Exceeds 12 kV**
- **Driver Output Current up to ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Power-Up, Power-Down Glitch-Free Operation**
- **Pin-Compatible With the SN75ALS170**
- **Available in Shrink Small-Outline Package**

SN65LBC170DB (marked as BL170)
SN75LBC170DB (marked as BL170)
(TOP VIEW)



SN65LBC170DW (marked as 65LBC170)
SN75LBC170DW (marked as 75LBC170)
(TOP VIEW)



NC – No internal connection

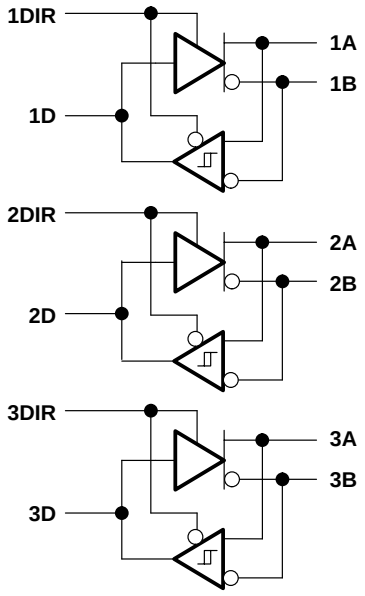
description

The SN65LBC170 and SN75LBC170 are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. Potential applications include serial or parallel data transmission, cabled peripheral buses with twin axial, ribbon, or twisted-pair cabling. These devices are suitable for FAST-20 SCSI and can transmit or receive data pulses as short as 25 ns, with skew less than 3 ns.

These devices combine three 3-state differential line drivers and three differential input line receivers, all of which operate from a single 5-V power supply.

The driver differential outputs and the receiver differential inputs are connected internally to form three differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature a wide common-mode voltage range making the device suitable for party-line applications over long cable runs.

logic diagram



†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

description (continued)

The driver's active-high enable and the receiver's active-low enable are tied together internally and provide a direction input for each driver/receiver pair.

The SN75LBC170 is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC170 is characterized for operation over the temperature range of –40°C to 85°C.

AVAILABLE OPTIONS†

T_A	PACKAGE	
	PLASTIC SHRINK SMALL-OUTLINE (JEDEC MO-150)	PLASTIC SMALL-OUTLINE (JEDEC MS-013)
0°C to 70°C	SN75LBC170DB	SN75LBC170DW
–40°C to 85°C	SN65LBC170DB	SN65LBC170DW

† Add R suffix for taped and reel

Function Tables

EACH DRIVER

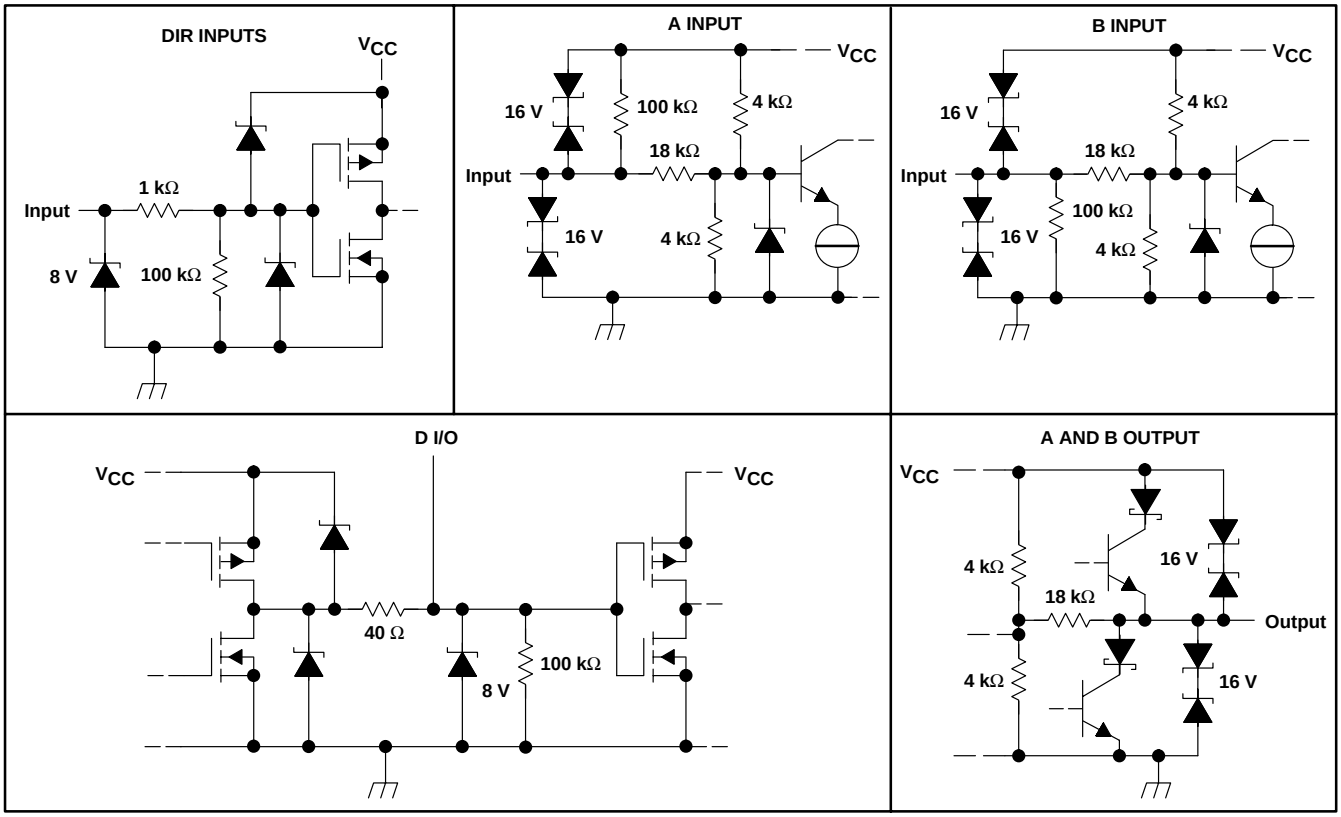
INPUT D	ENABLE DIR	OUTPUTS A	B
H	H	H	L
L	H	L	H
OPEN	H	L	H
X	L	Z	Z
X	OPEN	X	X

EACH RECEIVER

DIFFERENTIAL INPUT (V_A–V_B)	ENABLE DIR	OUTPUT D
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
OPEN	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

equivalent input and output schematic diagrams



absolute maximum ratings†

Supply voltage, V_{CC} (see Note 1) . . . . . –0.3 V to 6 V
Voltage range at any bus I/O terminal (steady state) . . . . . –10 V to 15 V
Voltage input range, A and B, (transient pulse through 100 Ω, see Figure 12) . . . . . –30 V to 30 V
Voltage range at any D or DIR terminal . . . . . – 0.5 V to V_{CC} + 0.5 V
Electrostatic discharge: Human body model (A, B, GND) (see Note 2) . . . . . 12 kV
All pins . . . . . 5 kV
Charged-device model (all pins) (see Note 3) . . . . . 1 kV
Continuous total power dissipation . . . . . See Power Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114–A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

POWER DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	995 mW	8.0 mW/°C	635 mW	515 mW
DW	1480 mW	11.8 mW/°C	950 mW	770 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus I/O terminal	A, B	–7		12	V
High-level input voltage, V_{IH}	D, DIR	2		V_{CC}	V
Low-level input voltage, V_{IL}	D, DIR	0		0.8	V
Differential input voltage, V_{ID}	A with respect to B	–12		12	V
Output current	Driver	–60		60	mA
	Receiver	–8		8	mA
Operating free-air temperature, T_A	SN75LBC170	0		70	°C
	SN65LBC170	–40		85	°C

DRIVER SECTION

electrical characteristics over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D and DIR	I_I = 18 mA		–1.5	–0.7		V
V_O	Open-circuit output voltage (single-ended)		A or B, No load		0		V_{CC}	V
$\lvert V_{OD(SS)} \rvert$	Steady-state differential output voltage magnitude‡		No load		3.8	4.3	V_{CC}	V
			R_L = 54 Ω,	See Figure 1	1	1.6	2.4	
			With common-mode loading,	See Figure 2	1	1.6	2.4	
ΔV_{OD}	Change in differential output voltage magnitude, $\lvert V_{OD(H)} \rvert - \lvert V_{OD(L)} \rvert$		R_L = 54 Ω, C_L = 50 pF	See Figure 1	–0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				2	2.4	2.8	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage ($V_{OC(H)} - V_{OC(L)}$)				–0.2		0.2	V
I_I	Input current		D, DIR		–100		100	µA
I_O	Output current with power off		V_{CC} = 0 V,	V_O = –7 V to 12 V	–700		900	µA
I_{OS}	Short-circuit output current		V_O = –7 V to 12 V,	See Figure 7	–250		250	mA
I_{CC}	Supply current (driver enabled)		D at 0 V or V_{CC},	DIR at V_{CC}, No load		14	20	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Differential output propagation delay, low-to high	R_L = 54 Ω, C_L = 50 pF, See Figure 3	4	8.5	12	ns
t_{PHL}	Differential output propagation delay, high-to-low		4	8.5	11	
t_r	Differential output rise time		3	7.5	11	
t_f	Differential output fall time		3	7.5	11	
$t_{sk(p)}$	Pulse skew $\lvert (t_{PLH} - t_{PHL}) \rvert$				2	
$t_{sk(o)}$	Output skew§				1.5	
$t_{sk(pp)}$	Part-to-part skew¶				2	
t_{PLH}	Differential output propagation delay, low-to high	See Figure 4, (HVD SCSI double-terminated load)	3	7	10	ns
t_{PHL}	Differential output propagation delay, high-to-low		3	7.5	10	
t_r	Differential output rise time		3	7.5	12	
t_f	Differential output fall time		3	7.5	12	
$t_{sk(p)}$	Pulse skew $\lvert (t_{PLH} - t_{PHL}) \rvert$				3	
$t_{sk(o)}$	Output skew§				1.5	
$t_{sk(pp)}$	Part-to-part skew¶				2.5	
t_{PZH}	Output enable time to high level	See Figure 5		15	25	ns
t_{PHZ}	Output disable time from high level			18	25	
t_{PZL}	Output enable time to low level	See Figure 6		10	25	ns
t_{PLZ}	Output disable time from low level			17	25	

§ Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
¶ Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER SECTION

electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 8				0.2	V
V_{IT-}	Negative-going differential input voltage threshold			–0.2			
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)				40		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See Figure 8		4	4.7	V_{CC}	V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = –8 mA, See Figure 8		0	0.2	0.4	V
I_I	Line input current	Other input = 0 V	V_I = 12 V			0.9	mA
			V_I = –7 V	–0.7			
R_I	Input resistance	A, B		12			kΩ
I_{CC}	Supply current (receiver enabled)	A, B, D, and DIR open				16	mA

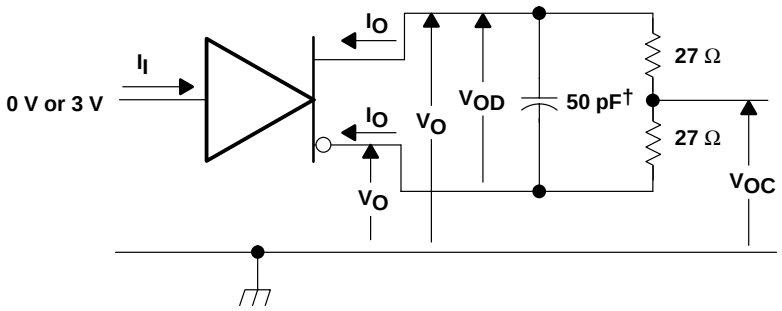
† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 9	7		16	ns
t_{PHL}	Propagation delay time, high-to-low level output		7		16	ns
t_r	Receiver output rise time			1.3	3	ns
t_f	Receiver output fall time			1.3	3	ns
t_{PZH}	Receiver output enable time to high level	See Figure 10		26	40	ns
t_{PHZ}	Receiver output disable time from high level				40	
t_{PZL}	Receiver output enable time to low level	See Figure 11		29	40	ns
t_{PLZ}	Receiver output enable time to high level				40	
$t_{sk(p)}$	Pulse skew (| $t_{PLH} – t_{PHL}$ |)				2	ns
$t_{sk(o)}$	Output skew‡				1.5	ns
$t_{sk(pp)}$	Part-to-part skew§				3	ns

‡ Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
§ Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION



† Includes probe and jig capacitance

Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

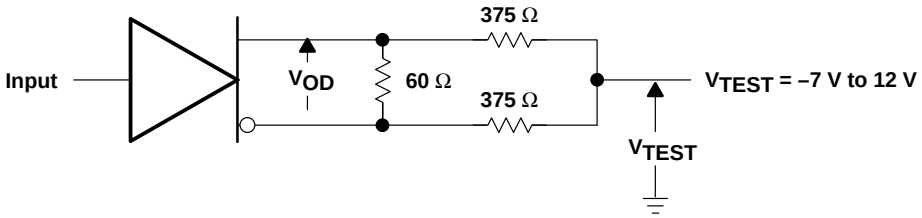
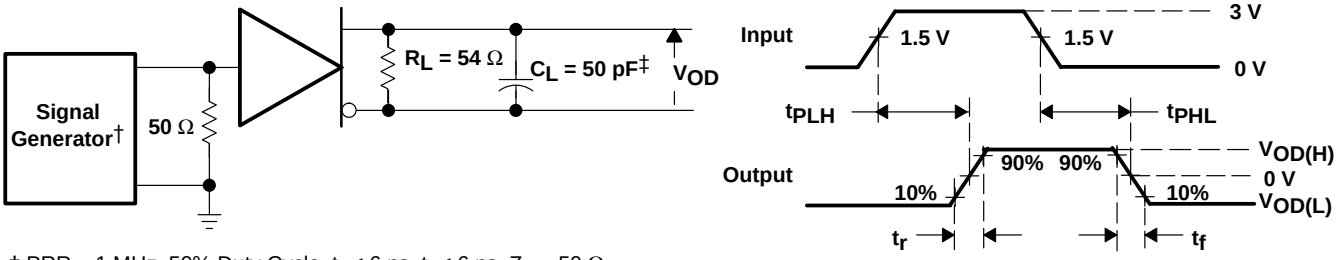


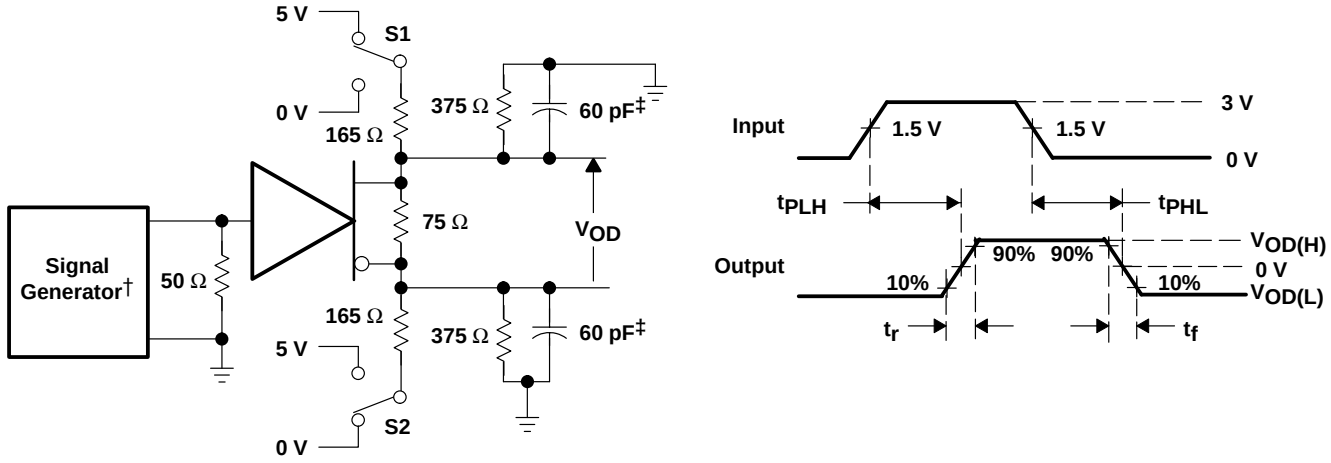
Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

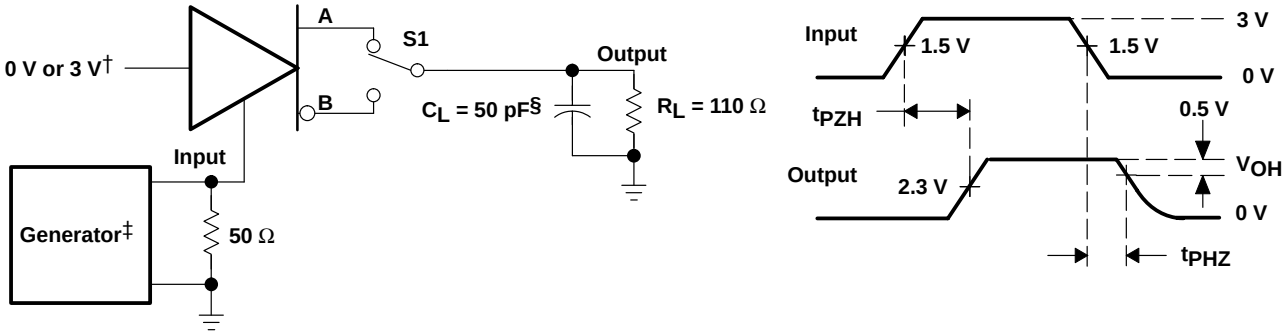
Figure 3. Driver Switching Test Circuit and Waveforms, 485-Loading

PARAMETER MEASUREMENT INFORMATION



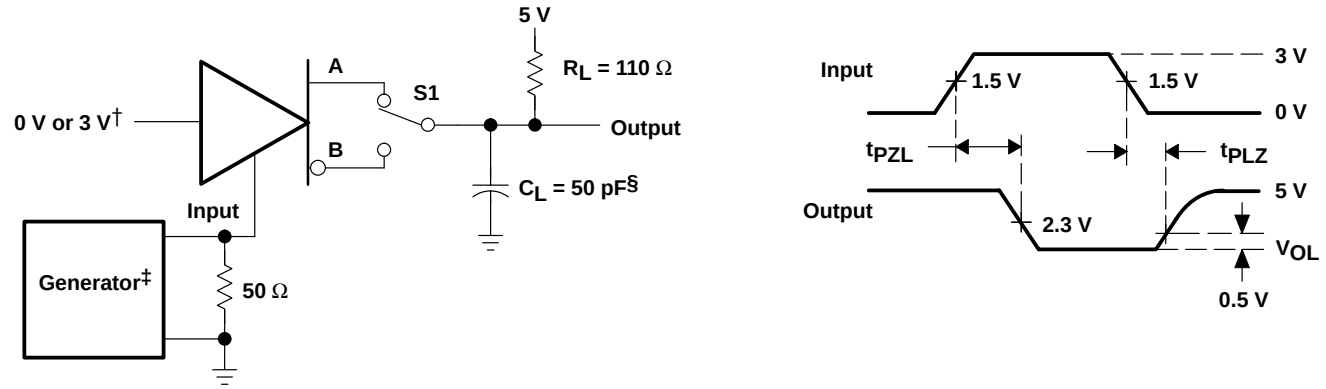
† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

Figure 4. Driver Switching Test Circuit and Waveforms, HVD SCSI-Loading (double terminated)



† 3 V if testing A output, 0 V if testing B output
‡ PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
§ Includes probe and jig capacitance

Figure 5. Driver Enable/Disable Test, High Output



† 0 V if testing A output, 3 V if testing B output
‡ PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
§ Includes probe and jig capacitance

Figure 6. Driver Enable/Disable Test, Low Output

PARAMETER MEASUREMENT INFORMATION

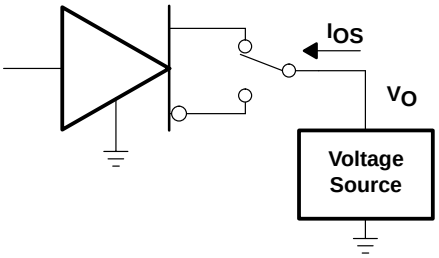


Figure 7. Driver Short-Circuit Test

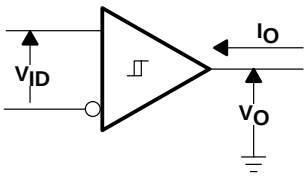
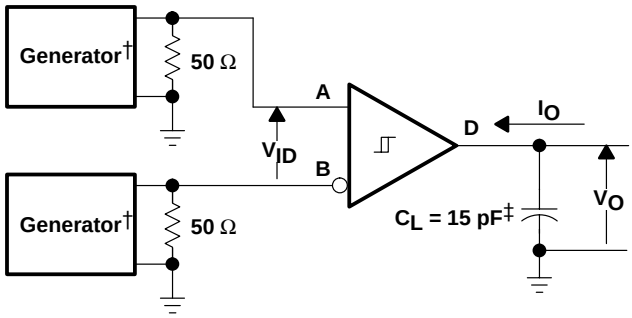
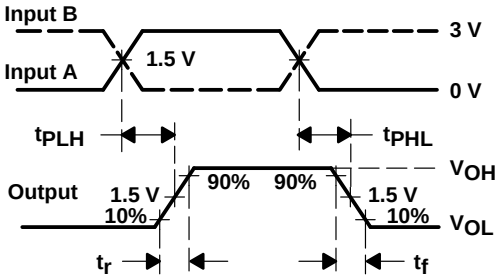


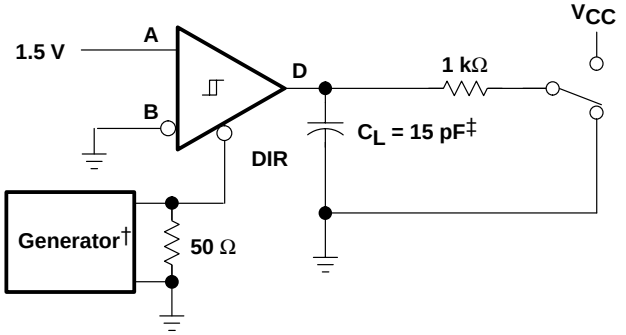
Figure 8. Receiver DC Parameters

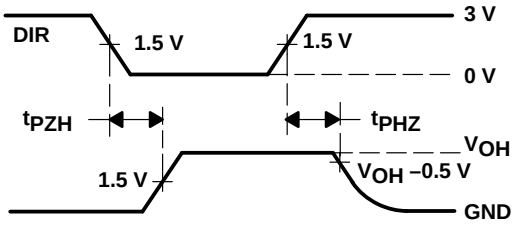




† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

Figure 9. Receiver Switching Test Circuit and Waveforms

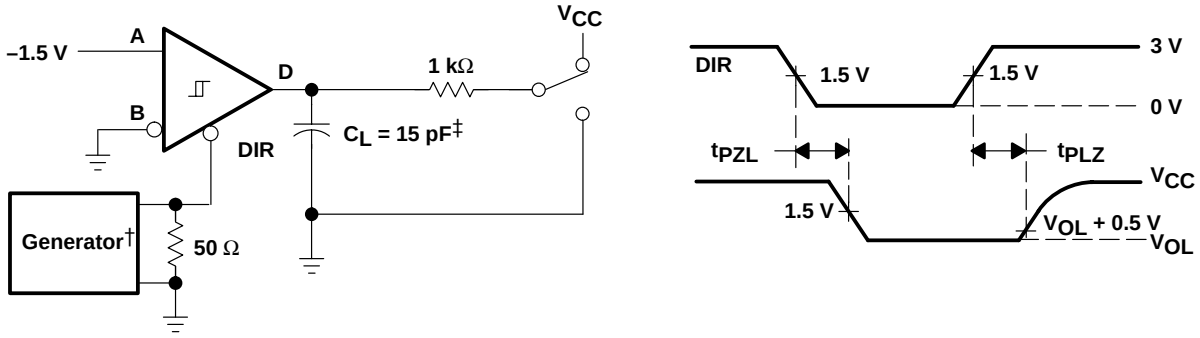




† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

Figure 10. Receiver Enable/Disable Test, High Output

PARAMETER MEASUREMENT INFORMATION



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

Figure 11. Receiver Enable/Disable Test, Low Output

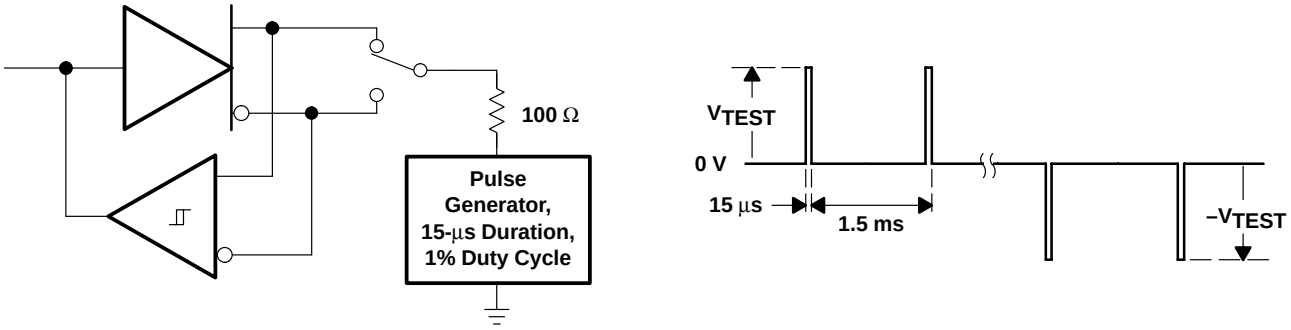


Figure 12. Test Circuit and Waveform, Transient Over Voltage Test

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

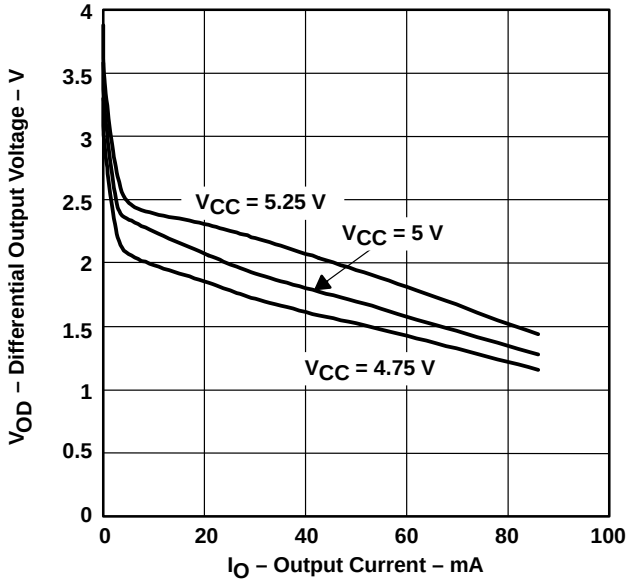


Figure 13

DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

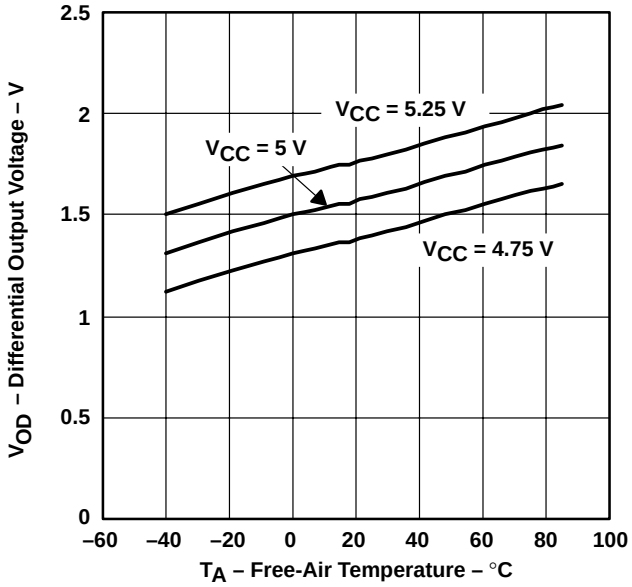


Figure 14

DRIVER PROPAGATION DELAY vs FREE-AIR TEMPERATURE

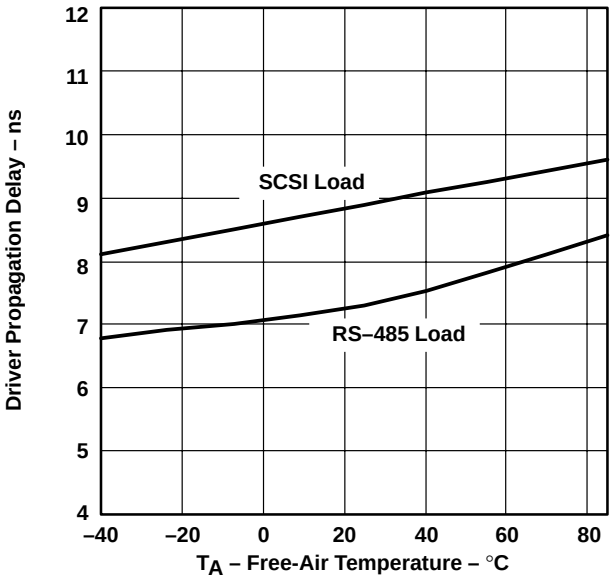


Figure 15

SUPPLY CURRENT vs SIGNALING RATE

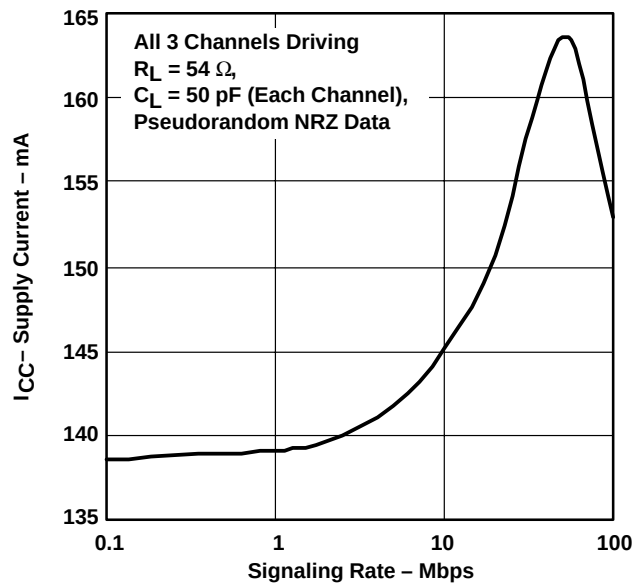


Figure 16

TYPICAL CHARACTERISTICS

BUS INPUT CURRENT vs BUS INPUT VOLTAGE

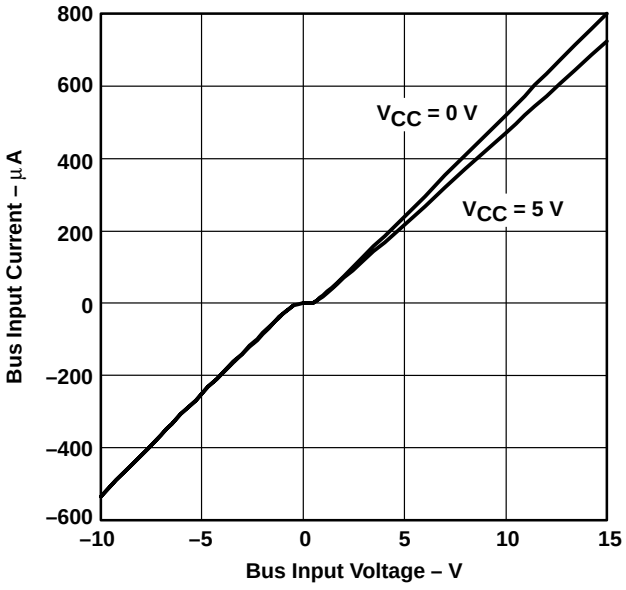


Figure 17

RECEIVER PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

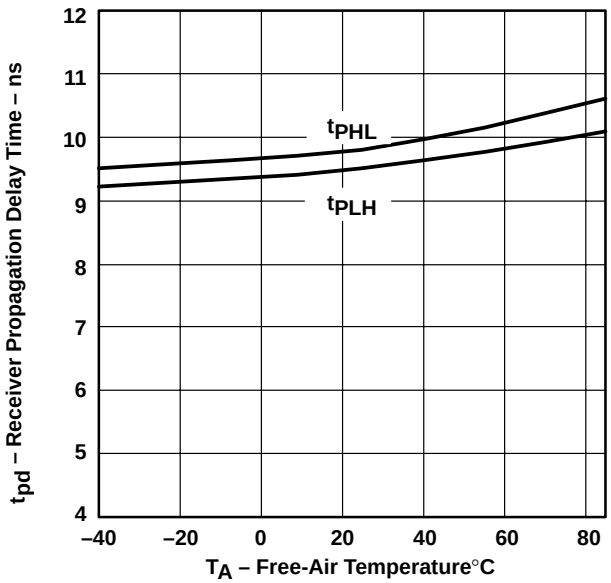


Figure 18

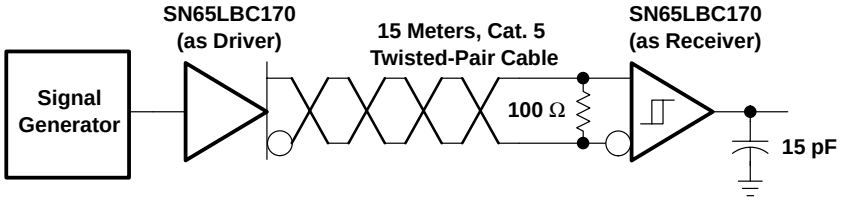


Figure 19. Circuit Diagram for Signaling Characteristics

TYPICAL CHARACTERISTICS

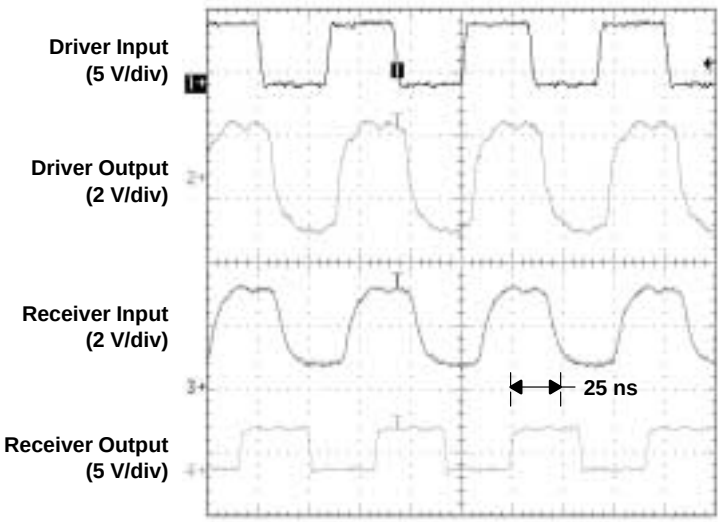


Figure 20. Signal Waveforms at 30 Mbps

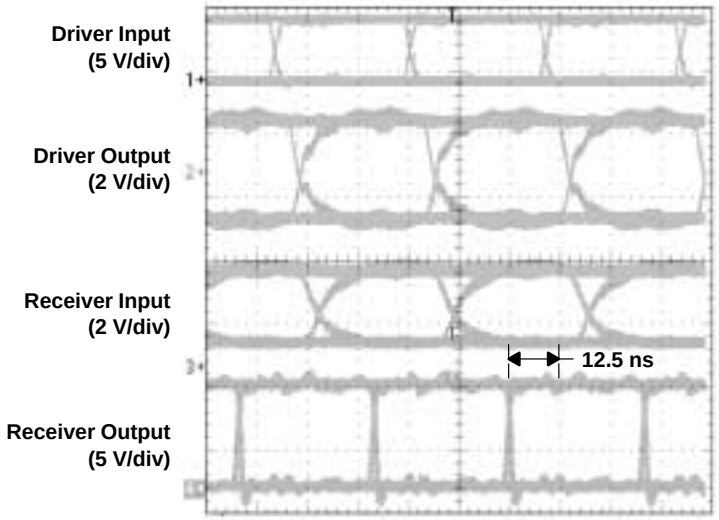


Figure 21. Eye Patterns, Pseudorandom Data at 30 Mbps

TYPICAL CHARACTERISTICS

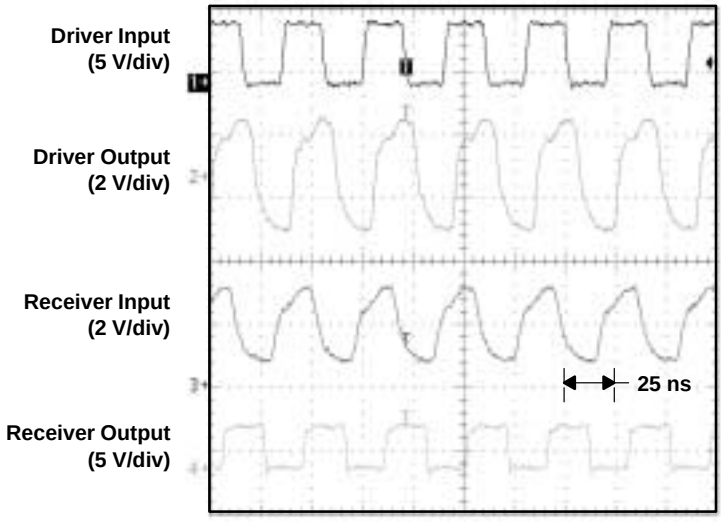


Figure 22. Signal Waveforms at 50 Mbps

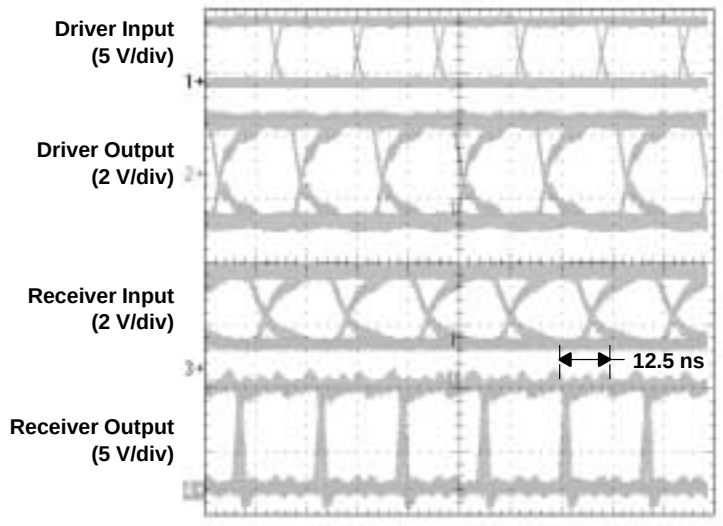
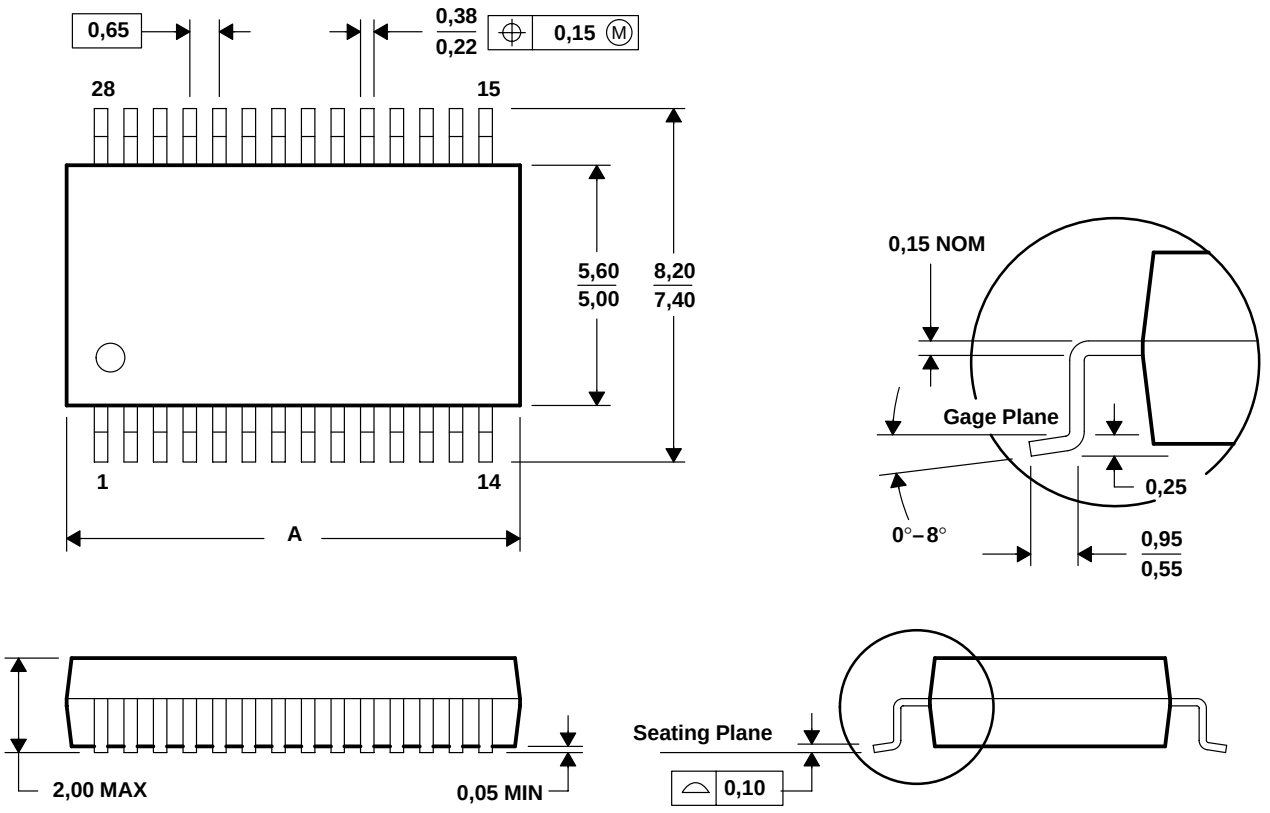


Figure 23. Eye Patterns, Pseudorandom Data at 50 Mbps

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

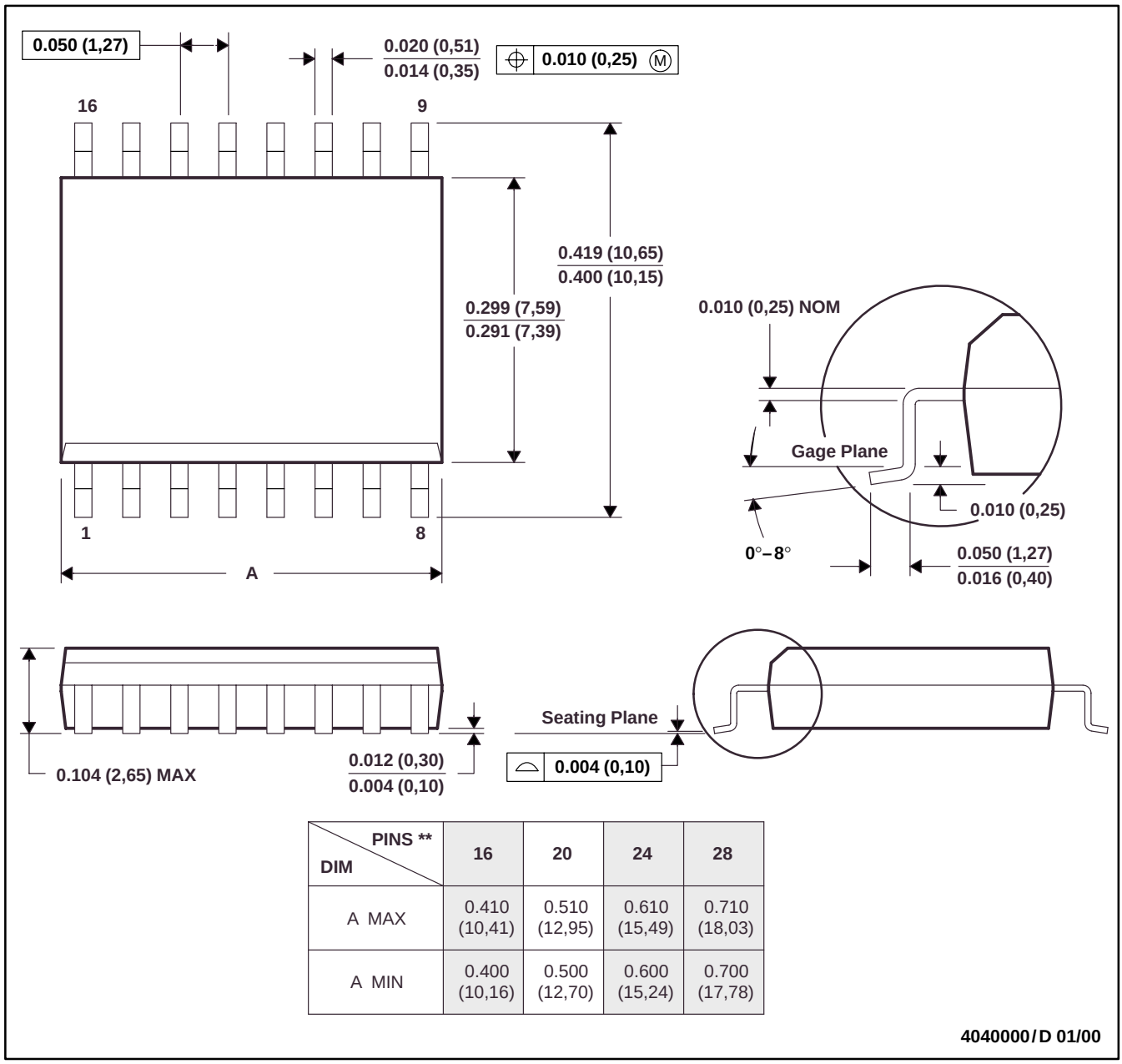
4040065 /D 09/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/D 01/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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