SN65LVDS100, SN65LVDT100
SN65LVDS101, SN65LVDT101

SLLS516A – AUGUST 2002 – REVISED OCTOBER 2002

2-Gbps DIFFERENTIAL TRANSLATOR/REPEATER

FEATURES

- **Designed for Signaling Rates(1) up to 2 Gbps**
- **Total Jitter < 65 ps**
- **Low-Power Alternative for the MC100EP16**
- **Low 100 ps (Max) Part-To-Part Skew**
- **25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range**
- **Inputs Electrically Compatible With LVPECL, CML, and LVDS Signal Levels**
- **3.3-V Supply Operation**
- **LVDT Integrates 110-Ω Terminating Resistor**
- **Offered in SOIC and MSOP**
- **Chip Scale Package (Product Preview)**

APPLICATIONS

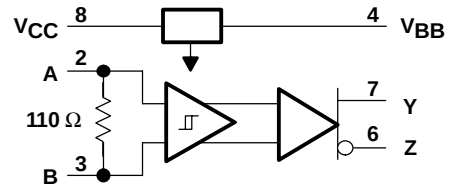
- **622 MHz Central Office Clock Distribution**
- **High-Speed Network Routing**
- **Wireless Basestations**
- **Low Jitter Clock Repeater**
- **Serdes LVPECL o/p to FPGA LVDS i/p Translator**

DESCRIPTION

These high-speed translators/repeaters were designed for signaling rates up to 2 Gbps to address various high-speed network routing applications. Inputs accept LVDS, LVPECL, and CML levels. The SN65LVDx100 provides LVDS outputs, while the SN65LVDx101 supports LVPECL outputs. They are compatible with the TIA/EIA-644-A (LVDS) standard (exception; the LVPECL output). Utilization of the LVDS technology allows for low power and high-speed operation. Internal data paths from input to output are fully differential for lower noise generation and low pulse width distortion. Although these devices are designed for 2 Gbps, some applications at a 2.5 Gbps data rate can be supported depending on loading and signal quality. The V_{BB} pin is an internally generated voltage supply to allow operation with single-ended (LVPECL) inputs. For those applications where board space is a premium, the LVDT devices have the integrated 110-Ω termination resistor. All devices are characterized for operation from –40°C to 85°C.

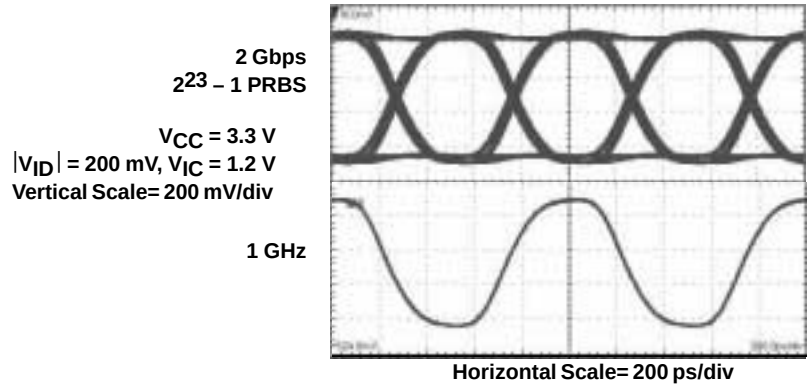
DEVICE	INPUT	OUTPUT
SN65LVDS100	LVDS or LVPECL or CML	LVDS
SN65LVDT100		
SN65LVDS101	LVDS or LVPECL or CML	LVPECL
SN65LVDT101		

FUNCTIONAL DIAGRAM



INTEGRATED TERMINATION ON SN65LVDTx

EYE PATTERN



Horizontal Scale= 200 ps/div

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

1The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

OUTPUT	TERMINATION RESISTOR	PART NUMBER	PART MARKING	PACKAGE	STATUS
LVDS	No	SN65LVDS100D	DL100	SOIC	Production
LVDS	No	SN65LVDS100DGK	AZK	MSOP	Production
LVDS	Yes	SN65LVDT100D	DE100	SOIC	Production
LVDS	Yes	SN65LVDT100DGK	AZL	MSOP	Production
LVPECL	No	SN65LVDS101D	DL101	SOIC	Production
LVPECL	No	SN65LVDS101DGK	AZM	MSOP	Production
LVPECL	Yes	SN65LVDT101D	DE101	SOIC	Production
LVPECL	Yes	SN65LVDT101DGK	BAF	MSOP	Production

Add the suffix R for taped and reeled carrier (i.e. SN65LVDS100DR).

(1) Chipscale packaging is under consideration for SN65LVDS100 and SN65LVDT100. Contact your local TI sales office for further information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			SN65LVDS100, SN65LVDT100 SN65LVDS101, SN65LVDT101
Supply voltage range,(2) V_{CC}			–0.5 V to 4 V
Sink/source, I_{BB}			±0.5 mA
Voltage range, (A, B, Y, Z)			0 V to 4.3 V
Differential voltage, $\|V_A - V_B\|$ (LVDT only)			1 V
ESD	Human Body Model(3)	A, B, Y, Z, and GND	±5 kV
		All pins	±2 kV
	Charged-Device Model(4)	All pins	±1500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range, T_{stg}			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Magnitude of differential input voltage $\|V_{ID}\|$	LVDS	0.1		1	V
	LVDT	0.1		0.8	
Input voltage (any combination of common-mode or input signals)		0		4	V
V_{BB} output current				400	µA
Operating free-air temperature, T_A		–40		85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DGK	425 mW	3.4 mW/°C	221 mW
D	725 mW	5.8 mW/°C	377 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

DEVICE CHARACTERISTICS

PARAMETER			MIN	NOM	MAX	UNIT
I_{CC}	Supply current	LVDS100		25	30	mA
		LVDS101		50	90	
V_{BB}	Switching reference voltage(1)		1890	1950	2010	mV

(1) V_{BB} parameter varies 1:1 with V_{CC}

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		–100			
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT+} - V_{IT-}$			25		mV
I_I	Input current (A or B inputs 'LVDS)	V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
		V_I = 4 V, Second input at 1.2 V			33	
	Input current (A or B inputs 'LVDT)	V_I = 0 V or 2.4 V, Other input open	–40		40	µA
		V_I = 4 V, Other input open			66	
$I_{I(OFF)}$	Power off input current (A or B inputs 'LVDS)	V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Second input at 1.2 V	–20		20	µA
		V_{CC} = 1.5 V, V_I = 4 V, Second input at 1.2 V			33	
	Power off input current (A or B inputs 'LVDT)	V_{CC} = 1.5 V, V_I = 0 V or 2.4 V, Other input open	–40		40	µA
		V_{CC} = 1.5 V, V_I = 2.4 V or 4 V, Other input open			66	
I_{IO}	Input offset current ($\lvert I_{IA} - I_{IB} \rvert$) ('LVDS)	$V_{IA} = V_{IB}$, $0 \le V_{IA} \le 4$ V	–6		6	µA
$R_{(T)}$	Termination resistance ('LVDT)	V_{ID} = 300 mV and 500 mV, V_{IC} = 0 to 2.4 V	90	110	132	Ω
	Termination resistance ('LVDT with power-off)	V_{ID} = 300 mV and 500 mV, V_{CC} = 1.5 V, V_{IC} = 0 to 2.4 V	90	110	132	
C_i	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
		V_{CC} = 0 V, V_I = 0.4 sin (4E6πt) + 0.5 V		3		

(1) All typical values are at 25°C and with a 3.3-V supply.

OUTPUT ELECTRICAL CHARACTERISTICS FOR SN65LVDx100 WITH LVDS OUTPUTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	See Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	See Figure 2	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3	–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 3		50	150	mV
I_{OS}	Short-circuit output current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0 V	–24		24	mA
$I_{OS(D)}$	Differential short-circuit output current	V_{OD} = 0 V	–12		12	mA
C_o	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
		V_{CC} = 0 V		3		

(1) All typical values are at 25°C and with a 3.3-V supply.

OUTPUT ELECTRICAL CHARACTERISTICS FOR SN65LVDx101 WITH LVPECL OUTPUTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	Output high voltage(2)	See Figure 4	2155	2280	2405	mV
V_{OL}	Output low voltage(2)	See Figure 4	1575	1690	1775	mV
$\|V_{OD}\|$	Differential output voltage magnitude	See Figure 4	475	575	750	mV
C_o	Differential output capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
		V_{CC} = 0 V		3		

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) Outputs are terminated through a 50-Ω resistor to V_{CC} – 2 V; PECL level specifications are referenced to V_{CC} and will track 1:1 with variation of V_{CC}.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	NOM(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	LVDx100	See Figure 5	300	470	800	ps
		LVDx101	See Figure 5	400	630	900	ps
t_{PHL}	Propagation delay time, high-to-low-level output	LVDx100	See Figure 5	300	470	800	ps
		LVDx101	See Figure 5	400	630	900	ps
t_r	Differential output signal rise time (20% – 80%)		See Figure 5			220	ps
t_f	Differential output signal fall time (20% – 80%)		See Figure 5			220	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)(2)				5	50	ps
$t_{sk(pp)}$	Part-to-part skew(3)		V_{ID} = 0.2 V			100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)		1 GHz clock input(5)		1	3.7	ps
$t_{jit(cc)}$	Cycle–to–cycle jitter (peak)(4)		1 GHz clock input(6)		6	23	ps
$t_{jit(pp)}$	Peak–to–peak jitter(4)		2 Gbps 2^{23}–1 PRBS input(7)		28	65	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak(4)		2 Gbps 2^7–1 PRBS input(8)		17	48	ps

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(5) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 1 GHz, t_r = t_f = 50 ps (20% to 80%), measured over 1000 samples.
(6) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 1 GHz, t_r = t_f = 50 ps (20% to 80%).
(7) Input voltage = V_{ID} = 200 mV, 2^{23}–1 PRBS pattern at 2 Gbps, t_r = t_f = 50 ps (20% to 80%), measured over 200k samples.
(8) Input voltage = V_{ID} = 200 mV, 2^7–1 PRBS pattern at 2 Gbps, t_r = t_f = 50 ps (20% to 80%).

PARAMETER MEASUREMENT INFORMATION

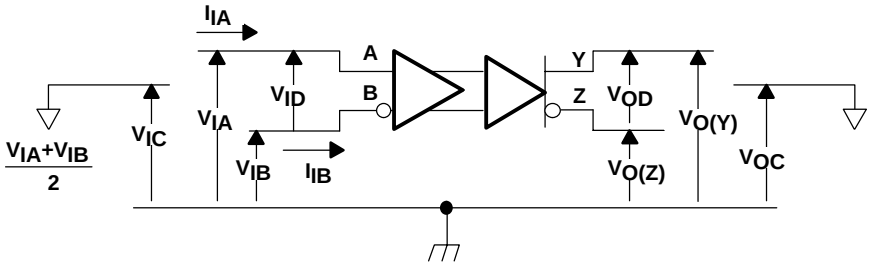


Figure 1. Voltage and Current Definitions

Table 1. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	–100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4. 0 V	–100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	–100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	–1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	–1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	–1000 mV	0.5 V	L

H = high level, L = low level

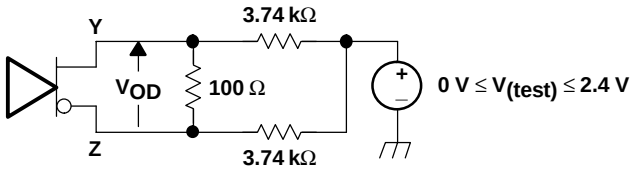
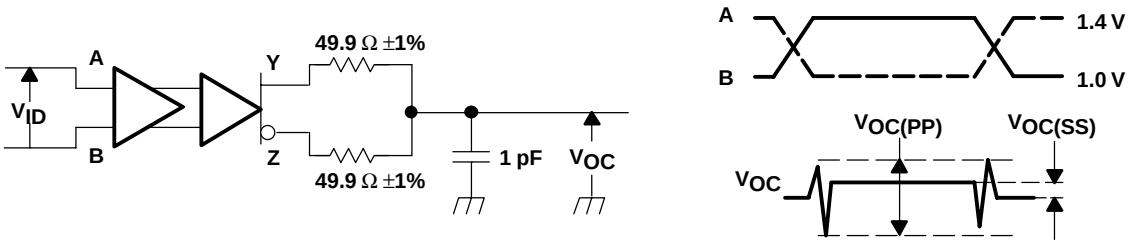


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 0.25$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

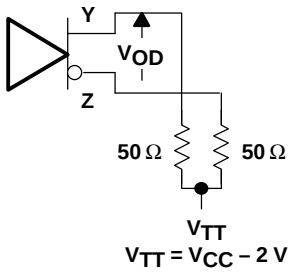
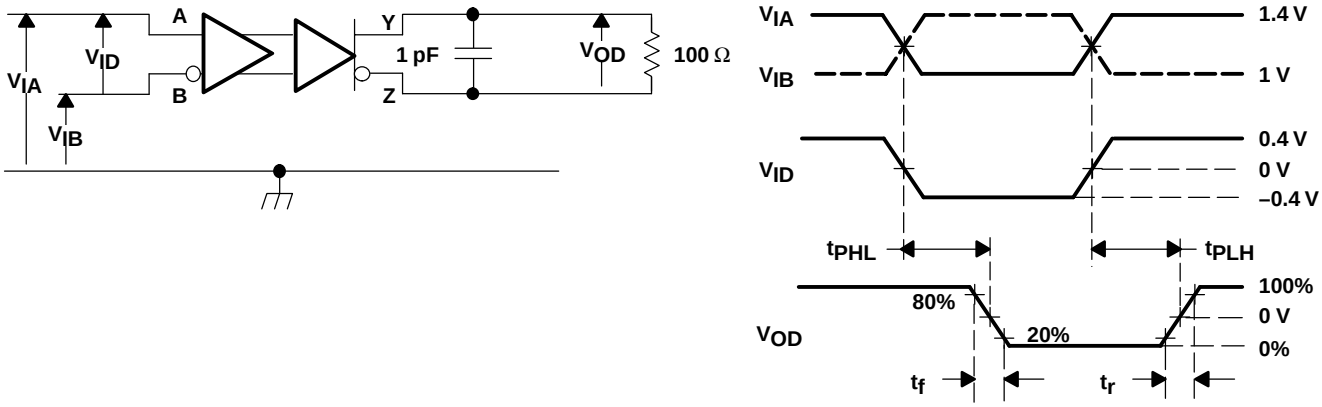


Figure 4. Typical Termination for LVPECL Output Driver (65LVDx101)

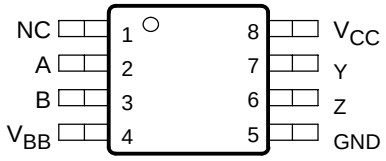


NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 0.25$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. Measurement equipment provides a bandwidth of 5 GHz minimum.

Figure 5. Timing Test Circuit and Waveforms

PIN ASSIGNMENTS

D AND DGK PACKAGE
(TOP VIEW)



V_{BB} on 'LVDS devices only

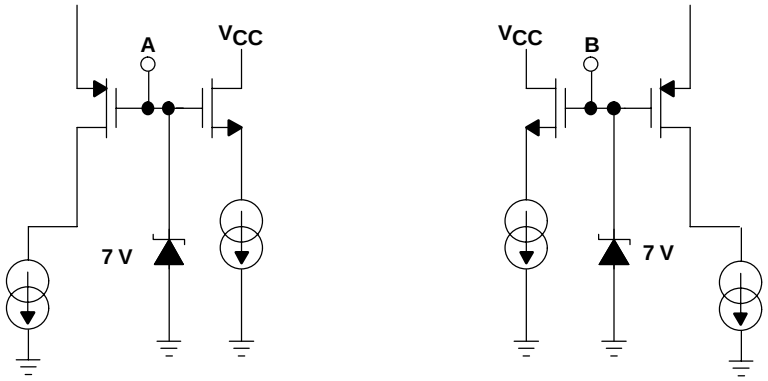
FUNCTION TABLE

DIFFERENTIAL INPUT	OUTPUTS	
$V_{ID} = V_A - V_B$	Y	Z
$V_{ID} \ge 100$ mV	H	L
-100 mV $< V_{ID} < 100$ mV	?	?
$V_{ID} \le -100$ mV	L	H
Open	?	?

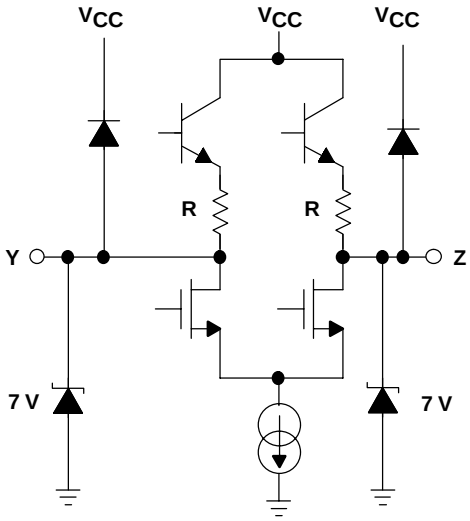
H = high level, L = low level, ? = intermediate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

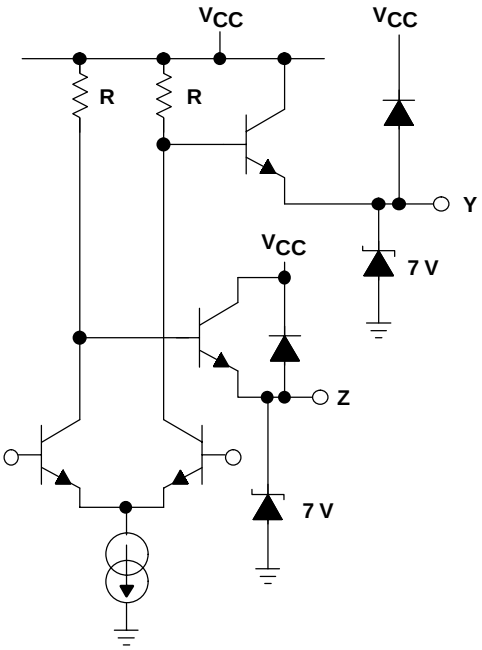
INPUT LVDS100/101



OUTPUT LVDS100



OUTPUT LVDS101



TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

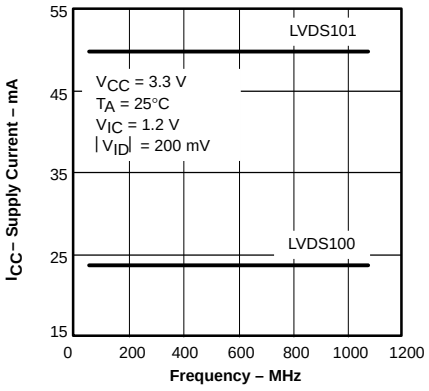


Figure 6

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

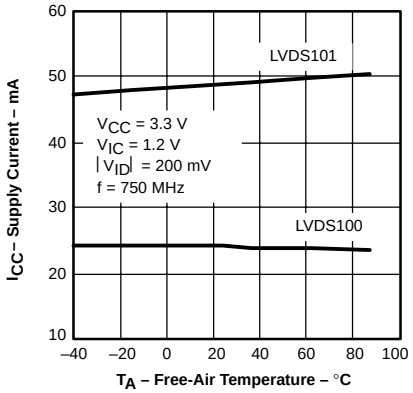


Figure 7

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

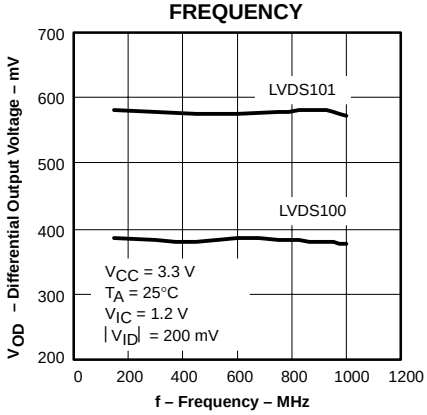


Figure 8

LVDS100 PROPAGATION DELAY TIME vs COMMON-MODE INTPUT VOLTAGE

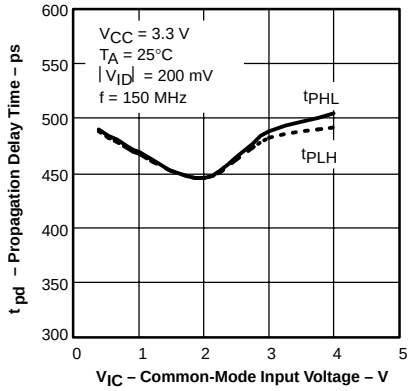


Figure 9

LVDS101 PROPAGATION DELAY TIME vs COMMON-MODE INPUT VOLTAGE

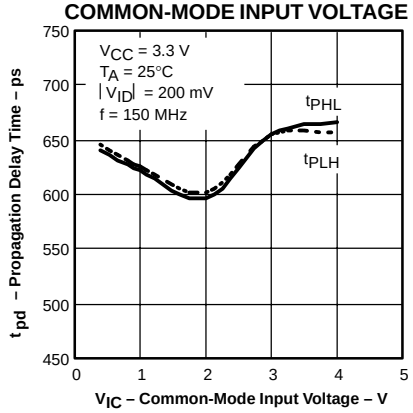


Figure 10

LVDS100 PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

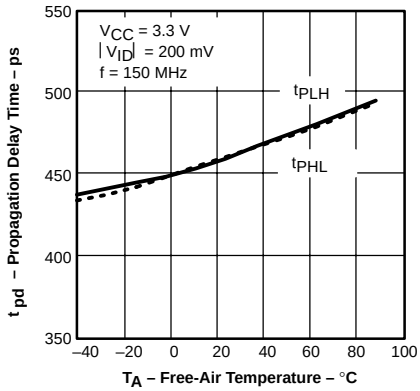


Figure 11

LVDS101 PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

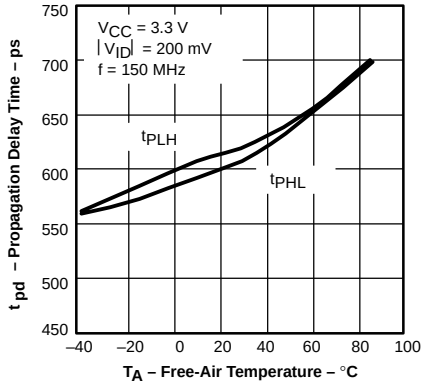


Figure 12

LVDS100 PEAK-TO-PEAK JITTER vs FREQUENCY

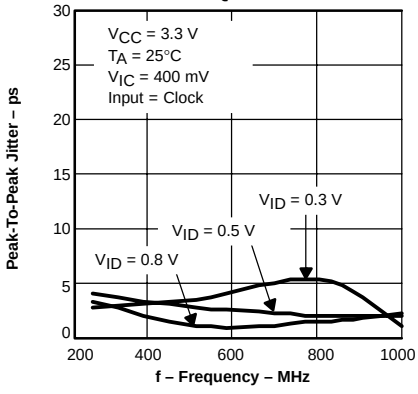


Figure 13

LVDS100 PEAK-TO-PEAK JITTER vs DATA RATE

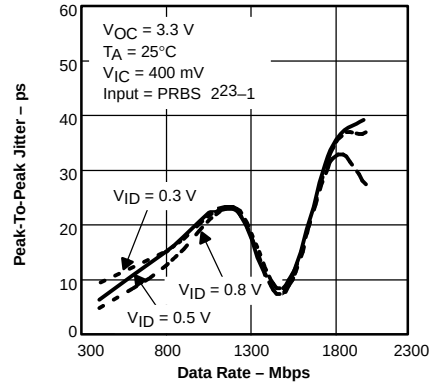


Figure 14

TYPICAL CHARACTERISTICS

LVDS101
PEAK-TO-PEAK JITTER
vs
FREQUENCY

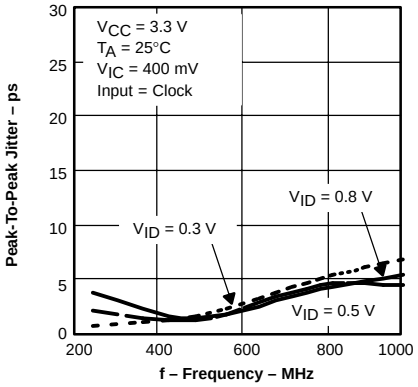


Figure 15

LVDS101
PEAK-TO-PEAK JITTER
vs
DATA RATE

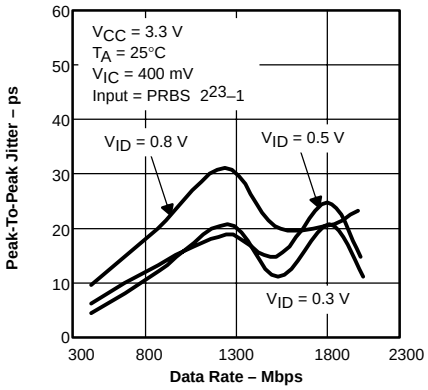


Figure 16

LVDS100
PEAK-TO-PEAK JITTER
vs
FREQUENCY

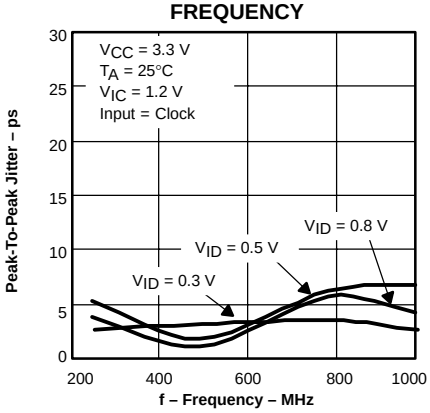


Figure 17

LVDS100
PEAK-TO-PEAK JITTER
vs
DATA RATE

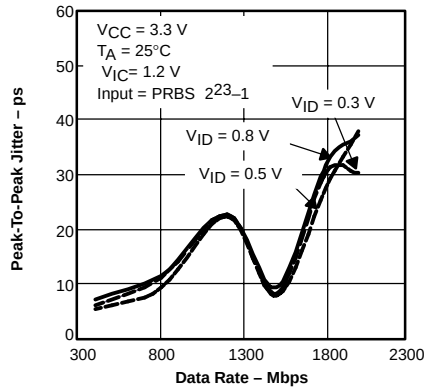


Figure 18

LVDS101
PEAK-TO-PEAK JITTER
vs
FREQUENCY

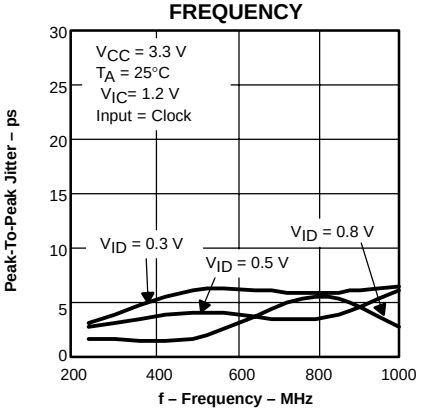


Figure 19

LVDS101
PEAK-TO-PEAK JITTER
vs
DATA RATE

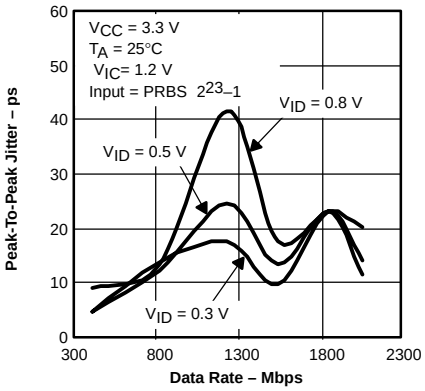


Figure 20

LVDS100
PEAK-TO-PEAK JITTER
vs
FREQUENCY

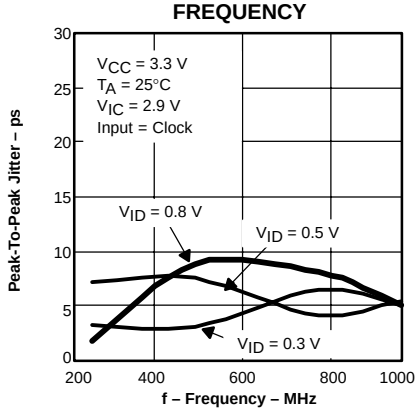


Figure 21

LVDS100
PEAK-TO-PEAK JITTER
vs
DATA RATE

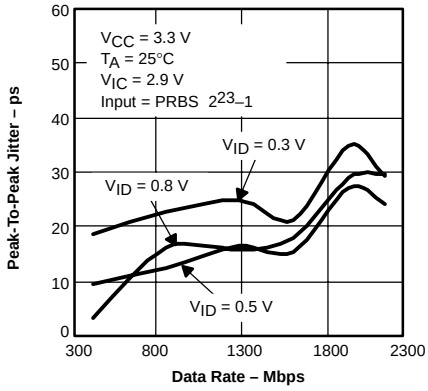


Figure 22

LVDS101
PEAK-TO-PEAK JITTER
vs
FREQUENCY

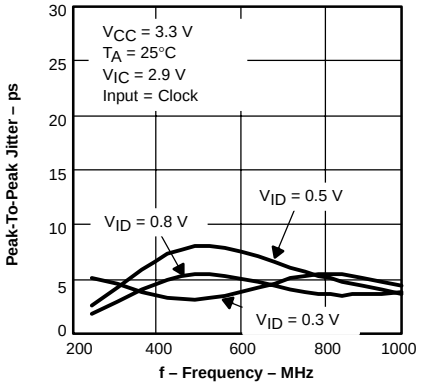


Figure 23

TYPICAL CHARACTERISTICS

LVDS101
PEAK-TO-PEAK JITTER
vs
DATA RATE

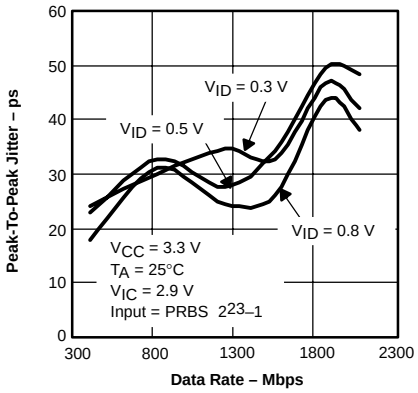


Figure 24

PEAK-TO-PEAK JITTER
vs
FREE-AIR TEMPERATURE

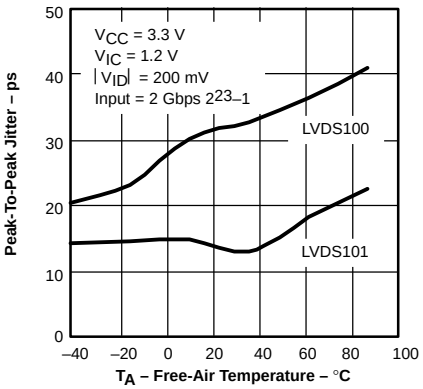
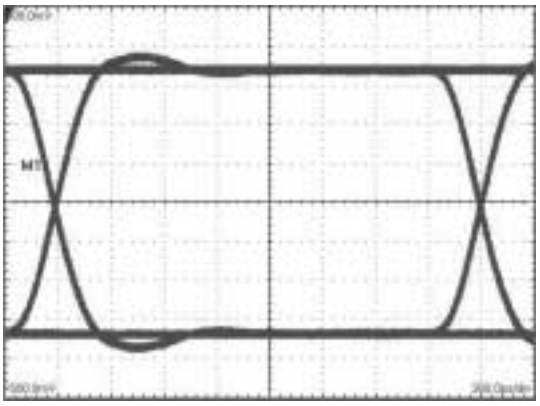


Figure 25

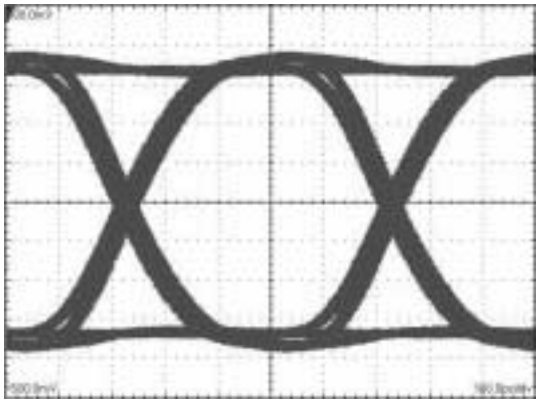
LVDS100
622 Mbps, 2^{23} – 1 PRBS



Horizontal Scale= 200 ps/div
LVPECL-to-LVDS

Figure 26

LVDS100
2 Gbps, 2^{23} – 1 PRBS

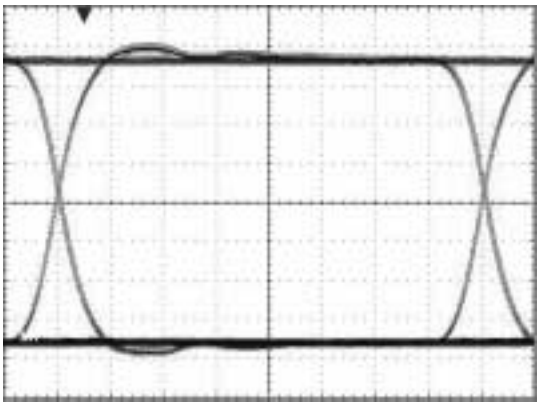


Horizontal Scale= 100 ps/div
LVPECL-to-LVDS

Figure 27

LVDS101

622 Mbps, 2^{23} – 1 PRBS

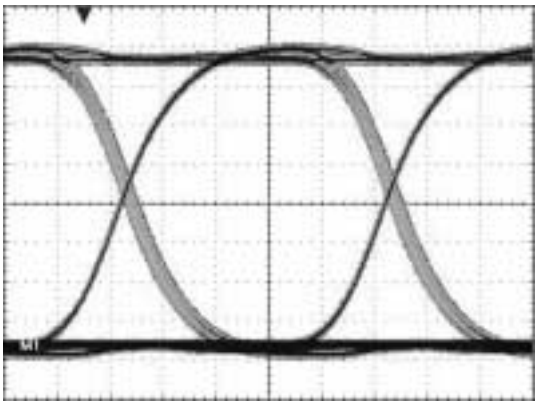


Horizontal Scale= 200 ps/div
LVDS-to-LVPECL

Figure 28

LVDS101

2 Gbps, 2^{23} – 1 PRBS



Horizontal Scale= 100 ps/div
LVDS-to-LVPECL

Figure 29

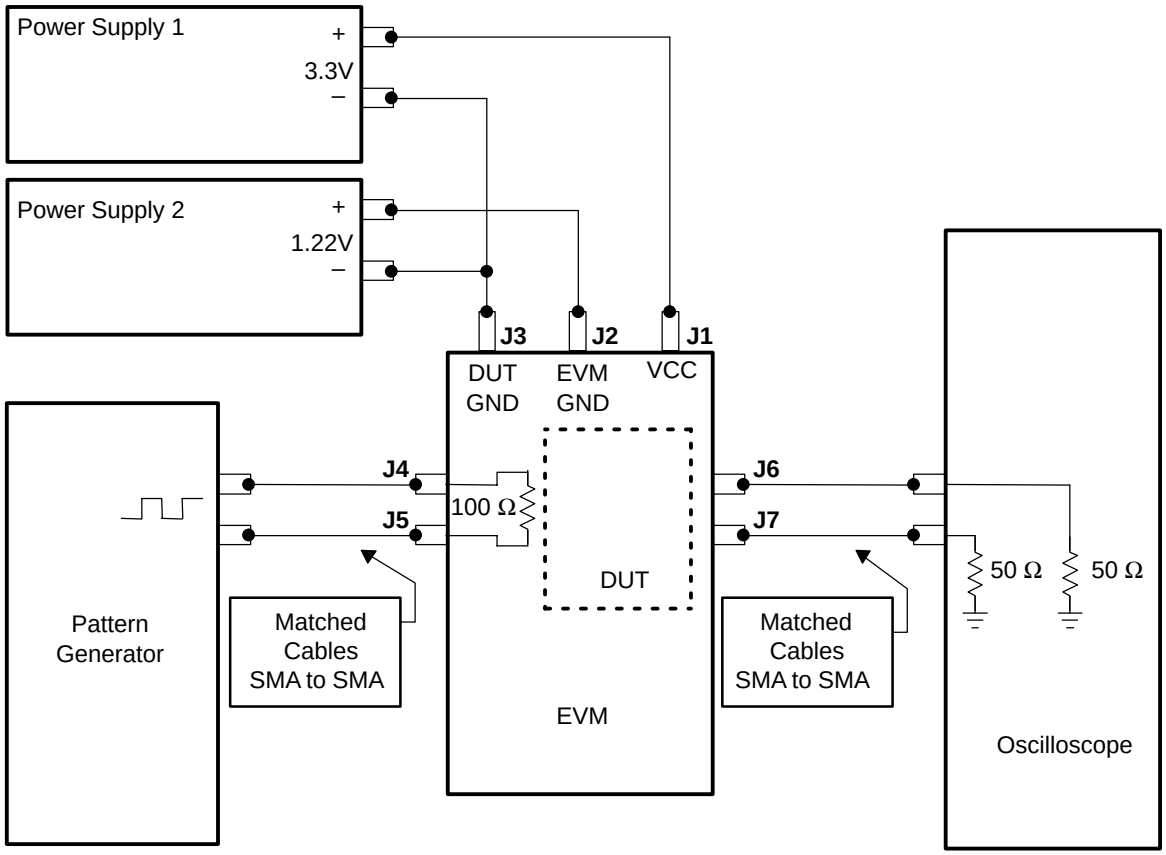


Figure 30. Jitter Setup Connections for SN65LVDS100 and SN65LVDS101

APPLICATION INFORMATION

For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. When V_{BB} is used, decouple V_{BB} and V_{CC} via a 0.01-µF capacitor and limit the current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, ETC.)

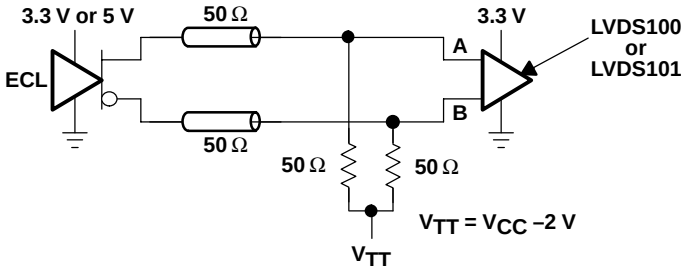


Figure 31. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

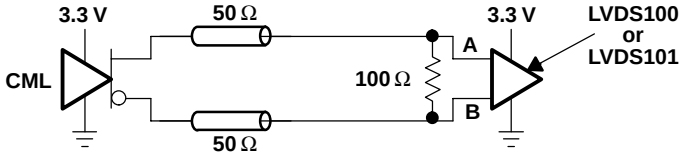


Figure 32. Common–Mode Logic (CML)

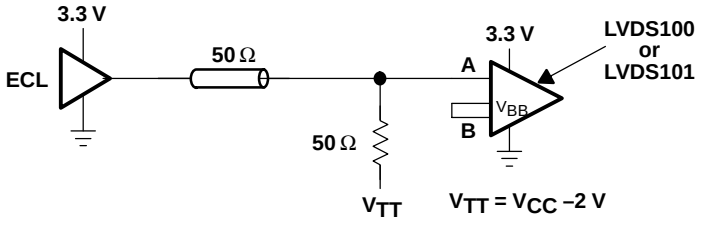


Figure 33. Single-Ended (LVPECL)

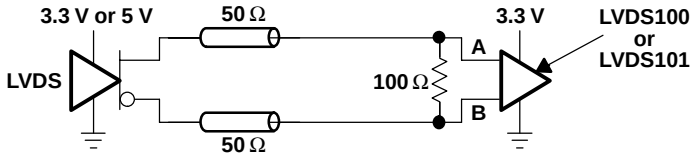


Figure 34. Low-Voltage Differential Signaling (LVDS)

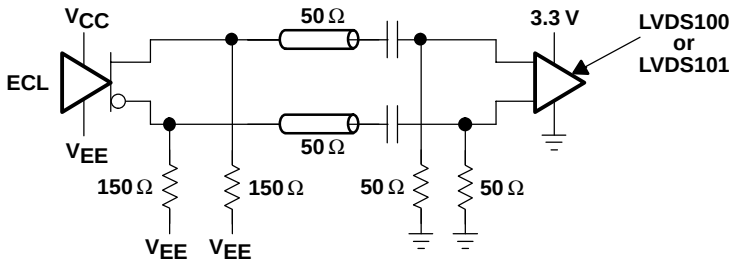
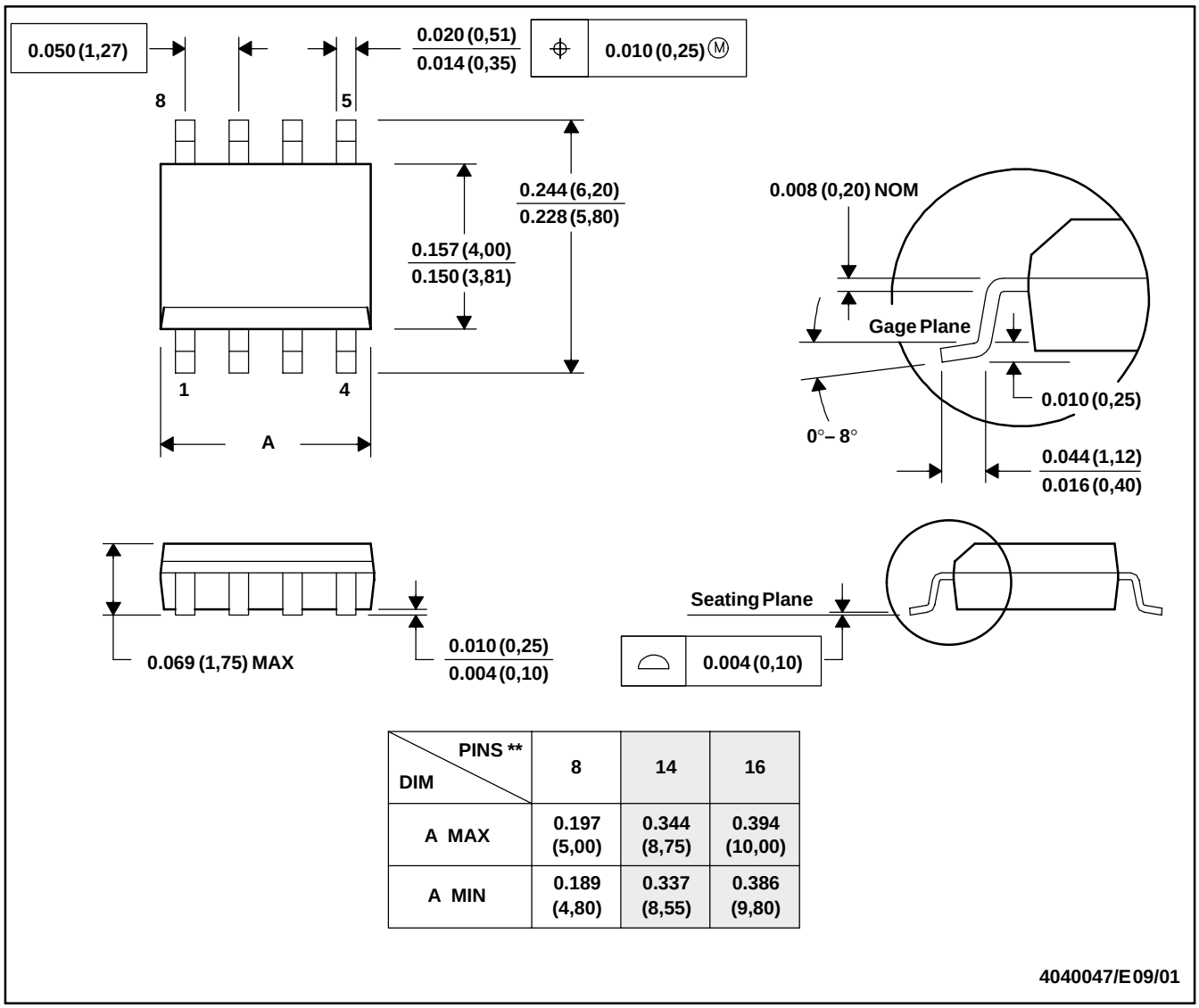


Figure 35. AC-Coupled Between ECL and LVDS or LVPECL

MECHANICAL DATA

D (R-PDSO-G) PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



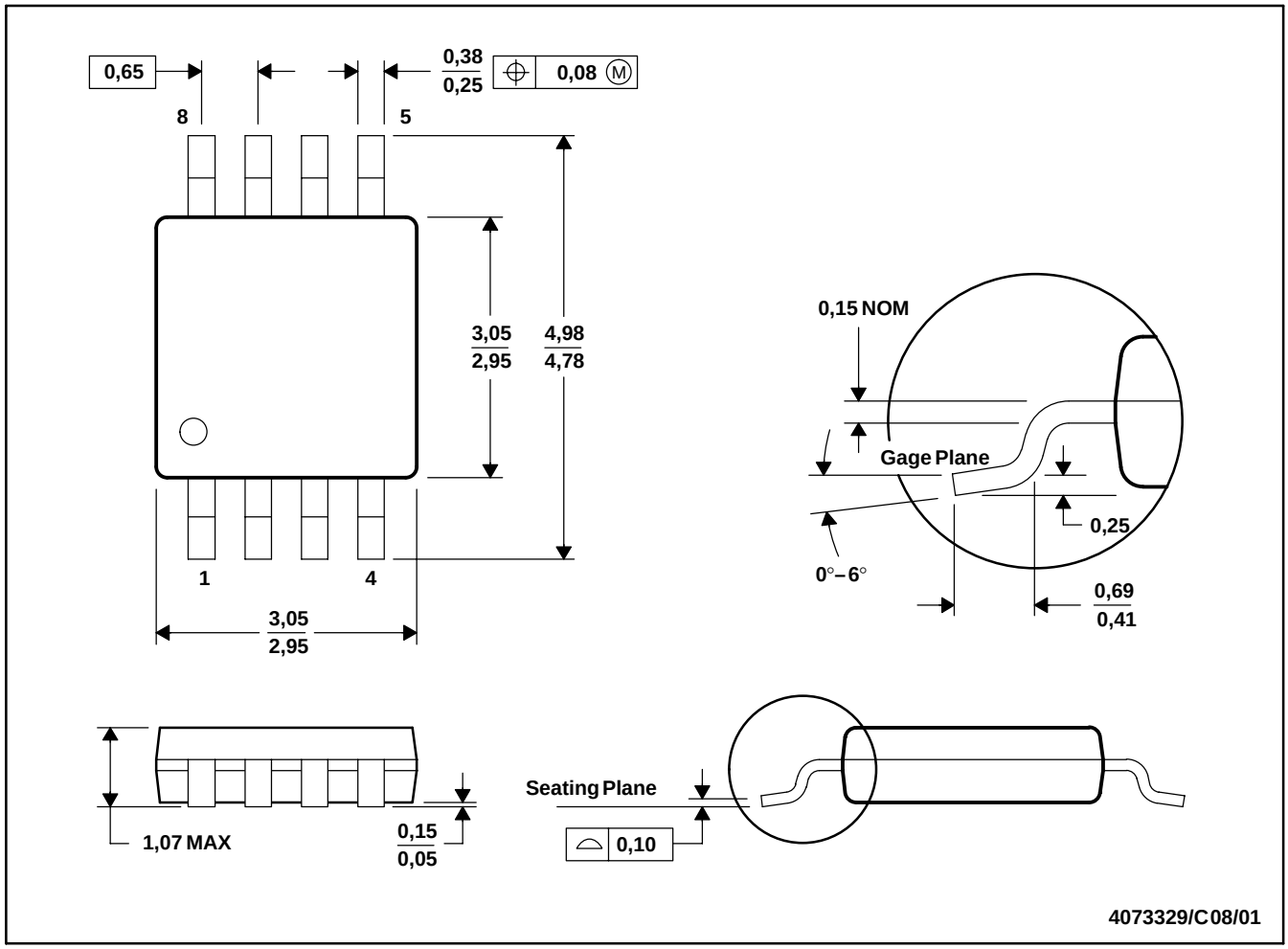
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES:A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

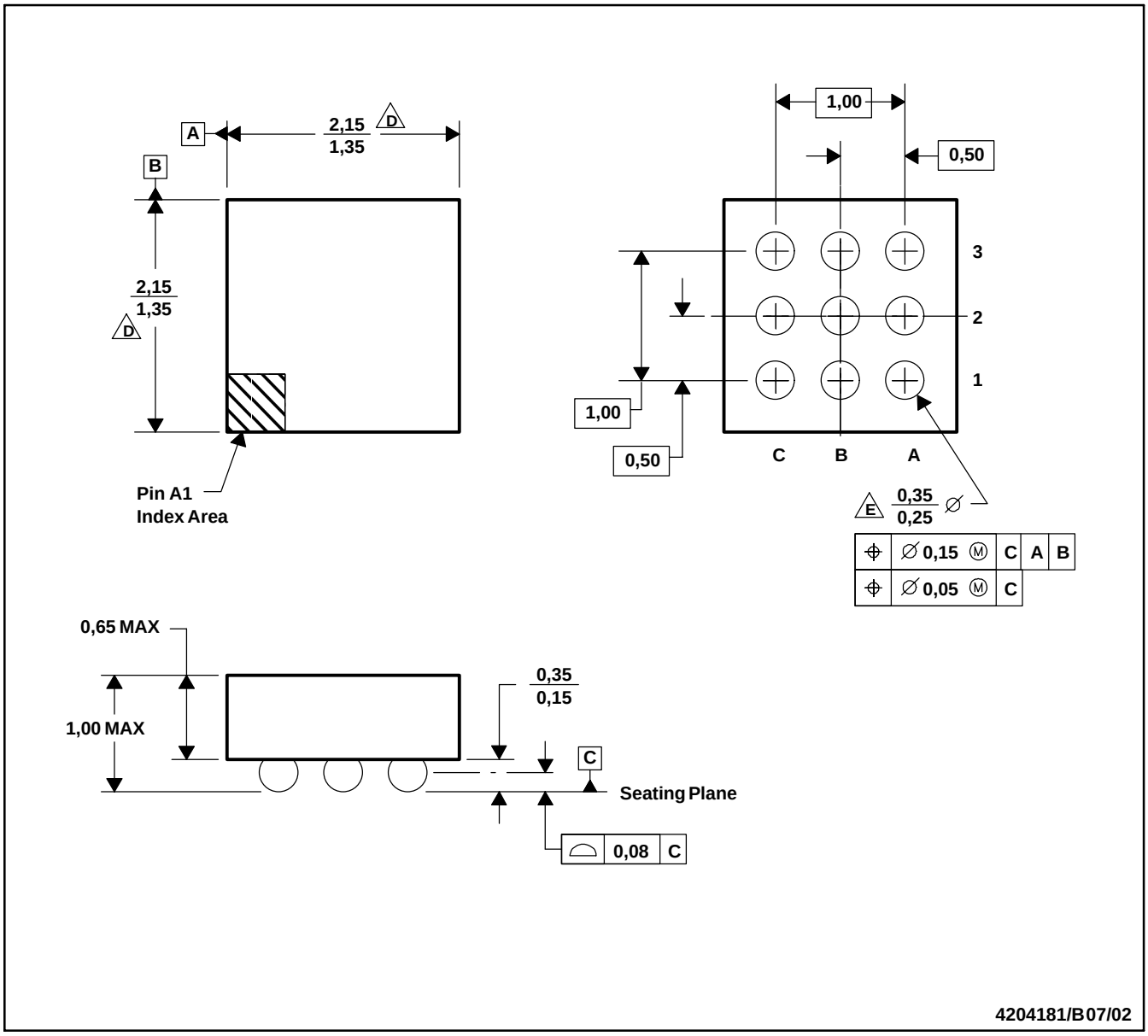
DGK (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

MECHANICAL DATA

YEF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Die size package configuration.
D. Reference Product Data Sheet for die size and orientation.
E. Reference Product Data Sheet for array population.
3 x 3 matrix pattern is shown for illustration only.

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