



Low-Noise, High-Speed, 16-Bit Accurate, CMOS OPERATIONAL AMPLIFIER

FEATURES

- High Bandwidth: 180MHz
- 16-Bit Settling in 150ns
- Low Noise: $3\text{nV}/\sqrt{\text{Hz}}$
- Low Distortion: 0.003%
- Low Power: 9.5mA (typ) on 5.5V
- Shutdown to $5\mu\text{A}$
- Unity Gain Stable
- Excellent Output Swing:
(V+) – 100mV to (V–) + 100mV
- Single Supply: +2.7V to +5.5V
- Tiny Packages: SO-8 and SOT23-6
(SOT23-6 available Q3, 2003)

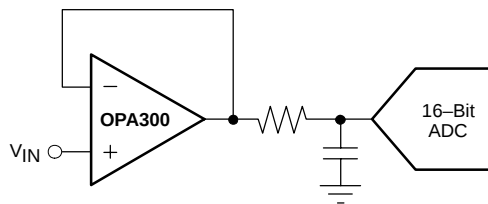
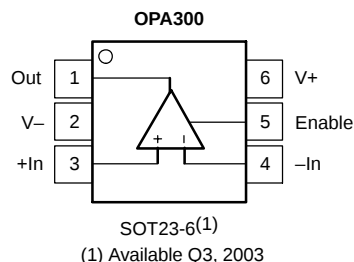
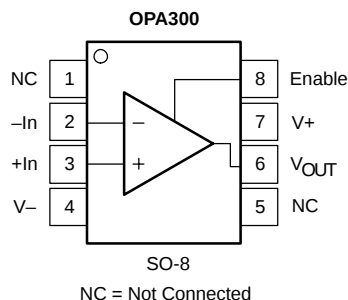
APPLICATIONS

- 16-Bit ADC Input Drivers
- Low-Noise Preamplifiers
- IF/RF Amplifiers
- Active Filtering

DESCRIPTION

The OPA300 series high-speed, voltage-feedback, CMOS operational amplifiers are designed for 16-bit resolution systems. The OPA300 is unity gain stable and features excellent settling and harmonic distortion specifications. Low power applications benefit from the low quiescent current of the OPA300, and a digital shutdown (Enable) function provides additional power savings during idle periods. Optimized for single-supply operation, the OPA300 offers superior output swing and excellent common-mode range.

The OPA300 has 180MHz of unity gain bandwidth, 500MHz of available bandwidth, low $3\text{nV}/\sqrt{\text{Hz}}$ voltage noise, and 0.1% settling within 30ns. Single-supply operation on 2.7V ($\pm 1.35\text{V}$) and 5.5V ($\pm 2.75\text{V}$) and a shutdown function that reduces supply current to $5\mu\text{A}$ are useful for portable low-power applications. The OPA300 is available in SO-8 packages, with SOT23-6 packages to be available Q3, 2003. The OPA300 is specified over the industrial temperature range of -40°C to $+125^{\circ}\text{C}$.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA300D	SO-8	D	–40°C to +125°C	300A	OPA300AID	Tube, 100
					OPA300AIDR	Tape and Reel, 2500
OPA300DBV(2)	SOT23-6	DBV	–40°C to +125°C	A52	OPA300AIDBVT	Tape and Reel, 250
					OPA300AIDBVR	Tape and Reel, 2500

(1) For the most current specification and package information, refer to our web site at www.ti.com.

(2) Shaded area indicates availability Q3, 2003.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

Power Supply V+	5.5V
Signal Input Terminals(2), Voltage	0.5V to (V+) + 0.5V
Current	±10mA
Open Short-Circuit Current(3)	Continuous
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–60°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Short-circuit to ground; one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS

TOP VIEW	SO	TOP VIEW	SOT23
OPA300 NC = Not Connected		OPA300(1) (1) Available Q3, 2003	

ELECTRICAL CHARACTERISTICS: $V_S = 2.7V$ TO $5.5V$

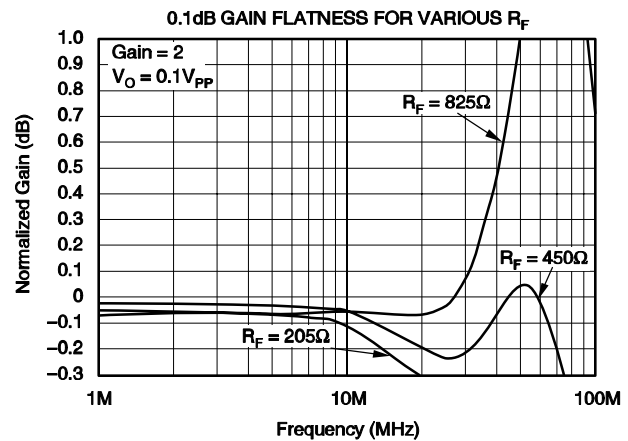
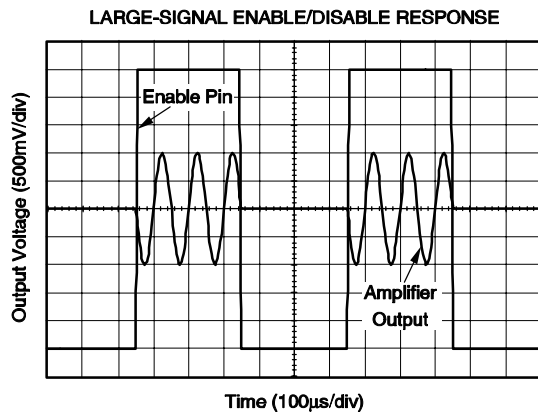
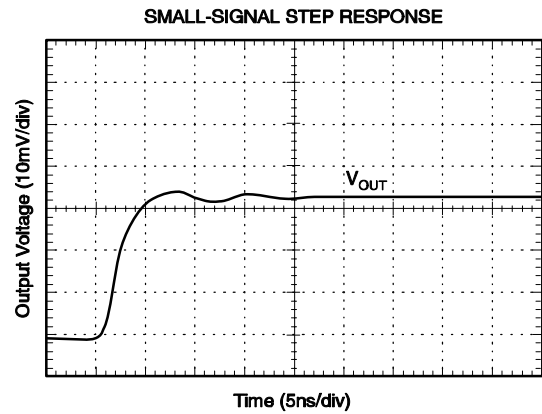
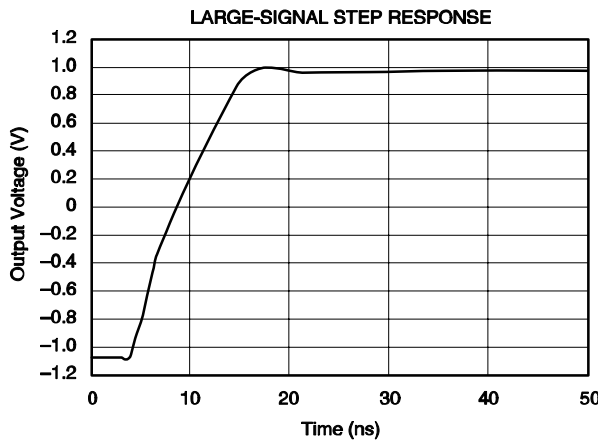
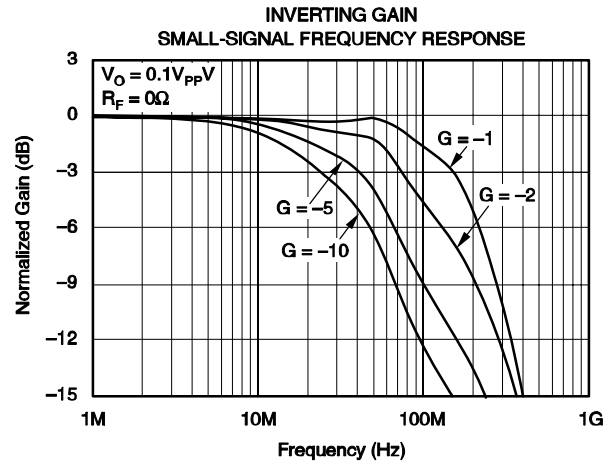
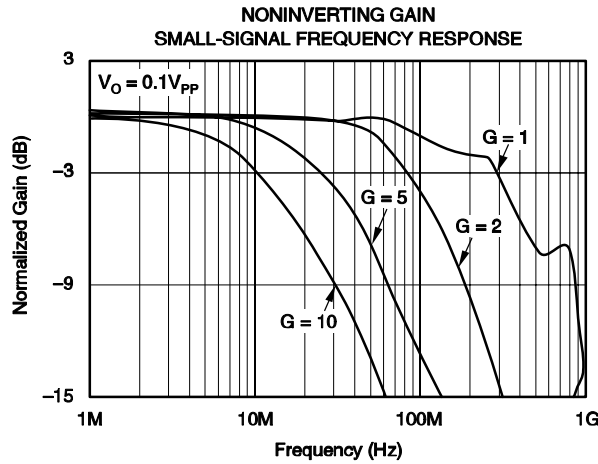
Boldface limits apply over the temperature range, $T_A = -40^{\circ}C$ to $+125^{\circ}C$.

All specifications at $T_A = +25^{\circ}C$, $R_L = 2k\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, and $V_{CM} = V_S/2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA300			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage V_{OS}	$V_S = 5V$		1	5	mV
Over Temperature				7	mV
Drift			2.5		$\mu V/^{\circ}C$
vs. Power Supply	$V_S = 2.7V$ to $5.5V$, $V_{CM} < (V+) - 0.9V$		50	200	$\mu V/V$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range V_{CM}		$(V-) - 0.2$		$(V+) - 0.9$	V
Common-Mode Rejection Ratio	$(V-) - 0.2V < V_{CM} < (V+) - 0.9V$	66	80		dB
INPUT BIAS CURRENT					
Input Bias Current I_B			± 0.1	± 5	pA
Input Offset Current I_{OS}			± 0.5	± 5	pA
INPUT IMPEDANCE					
Differential			$10^{13} \parallel 3$		$\Omega \parallel pF$
Common-Mode			$10^{13} \parallel 6$		$\Omega \parallel pF$
NOISE					
Input Voltage Noise, $f = 0.1Hz$ to $1MHz$			40		μV_{pp}
Input Voltage Noise Density, $f = 100kHz$			3		$nV/\sqrt{Hz}$
Input Current Noise Density, $f = 1kHz$			1.5		$fA/\sqrt{Hz}$
Differential Gain Error	$R_L = 150\Omega$		0.01		%
Differential Phase Error	$R_L = 150\Omega$		0.1		$^{\circ}$
OPEN-LOOP GAIN					
Open-Loop Voltage Gain A_{OL}	$V_S = 5V$, $R_L = 2k\Omega$, $0.1V < V_O < 4.9V$	95	106		dB
Over Temperature	$V_S = 5V$, $R_L = 2k$, $0.1V < V_O < 4.9V$	90			dB
	$V_S = 5V$, $R_L = 100\Omega$, $0.5V < V_O < 4.5V$	95	106		dB
Over Temperature	$V_S = 5V$, $R_L = 100$, $0.5V < V_O < 4.5V$	90			dB
OUTPUT					
Voltage Output Swing from Rail	$R_L = 2k\Omega$, $A_{OL} > 95dB$		75	100	mV
Short-Circuit Current I_{SC}	$R_L = 100\Omega$, $A_{OL} > 95dB$		300	500	mV
Capacitive Load Drive C_{LOAD}			70		mA
		See Typical Characteristic			
FREQUENCY RESPONSE					
Gain-Bandwidth Product GBW			180		MHz
Slew Rate SR	$G = +1$		80		$V/\mu s$
Settling Time, 0.01% t_S	$V_S = 5V$, 2V Step, $G = +1$		90		ns
0.1%			30		ns
Overload Recovery Time	Gain = -1		30		ns
Total Harmonic Distortion + Noise $THD+N$	$V_S = 5V$, $V_O = 3V_{pp}$, $G = +1$, $f = 1kHz$		0.003		%
POWER SUPPLY					
Specified Voltage Range V_S		2.7		5.5	V
Operating Voltage Range			2.7 to 5.5		V
Quiescent Current (per amplifier) I_Q	$I_O = 0$		9.5	12	mA
Over Temperature				13	mA
SHUTDOWN					
t_{OFF}			40		ns
t_{ON}			5		μs
V_L (shutdown)		$(V-) - 0.2$		$(V-) + 0.8$	V
V_H (amplifier is active)		$(V-) + 2.5$		$(V+) + 0.2$	V
I_{QSD}			3	5	μA
TEMPERATURE RANGE					
Specified Range		-40		125	$^{\circ}C$
Operating Range		-55		150	$^{\circ}C$
Storage Range		-65		150	$^{\circ}C$
Thermal Resistance θ_{JA}					$^{\circ}C/W$
SO-8			200		$^{\circ}C/W$

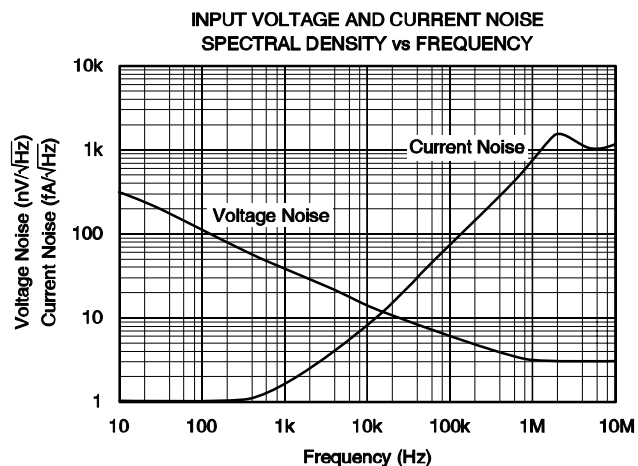
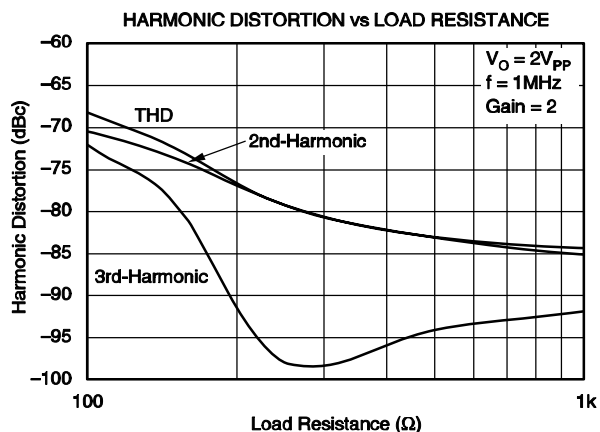
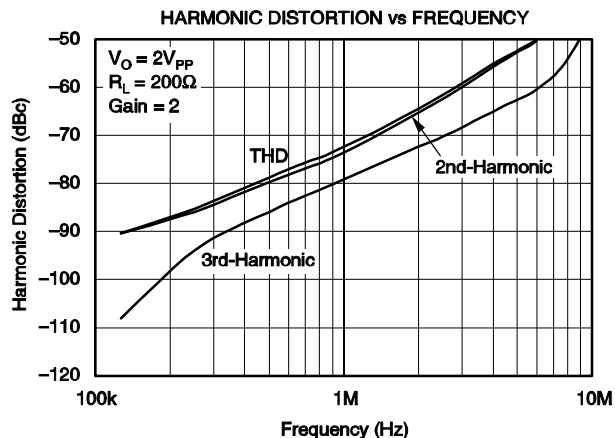
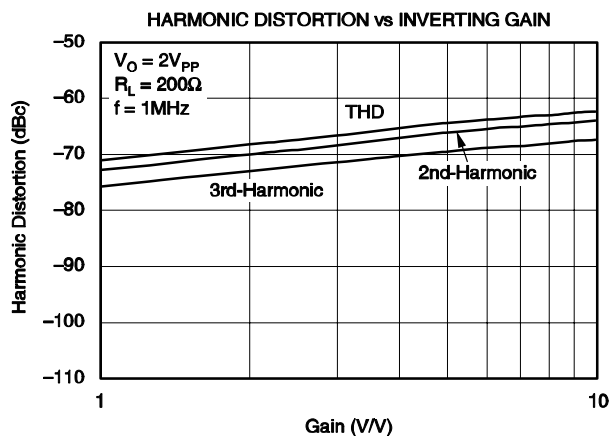
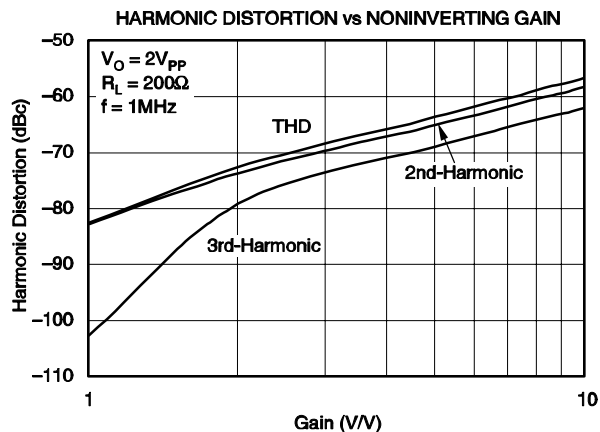
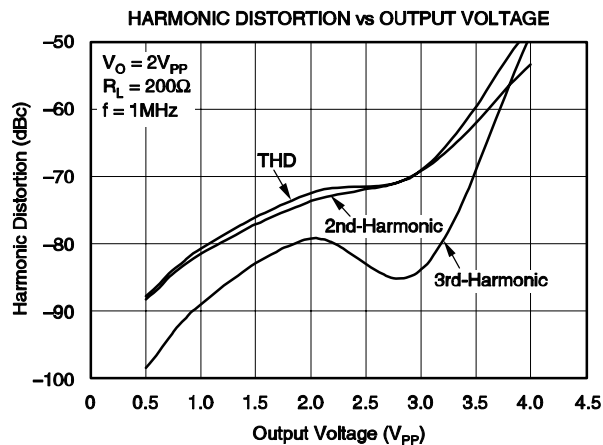
TYPICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_F = 310\Omega$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.



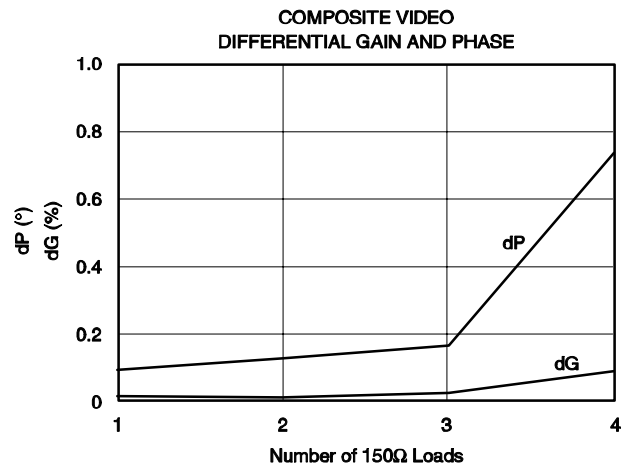
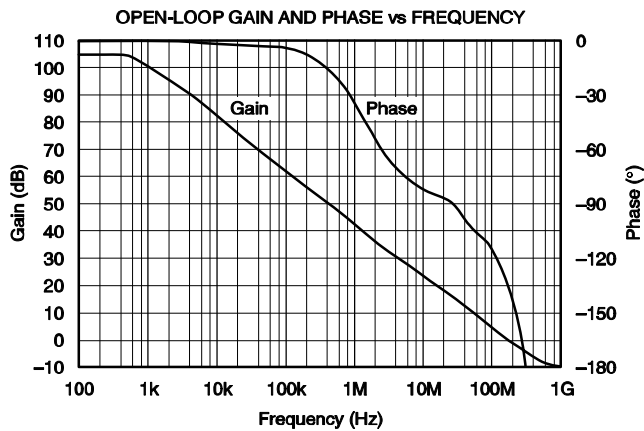
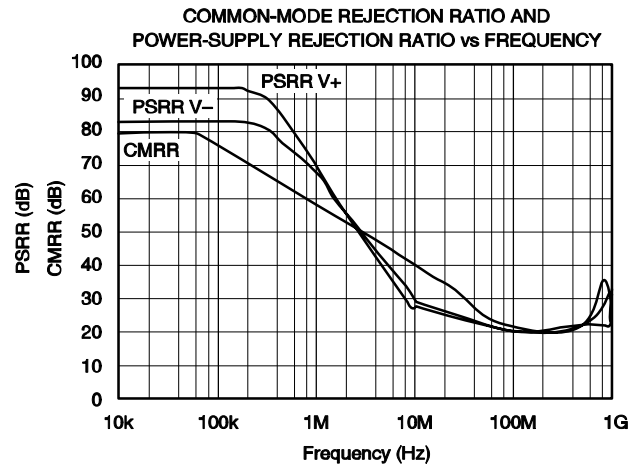
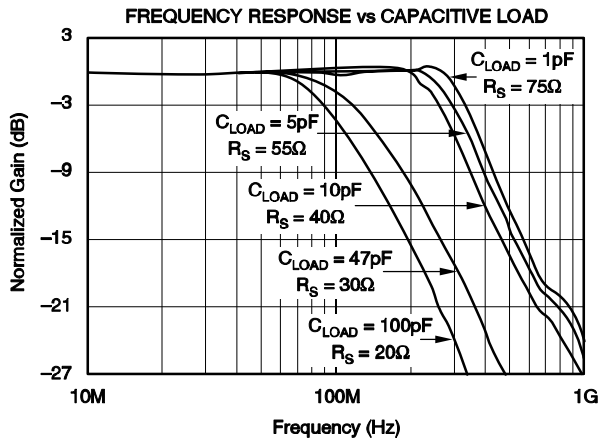
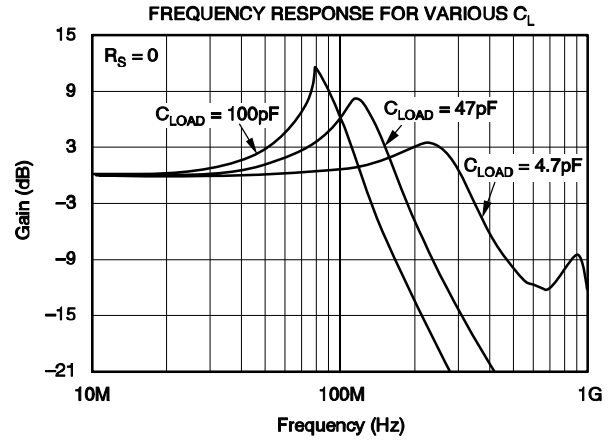
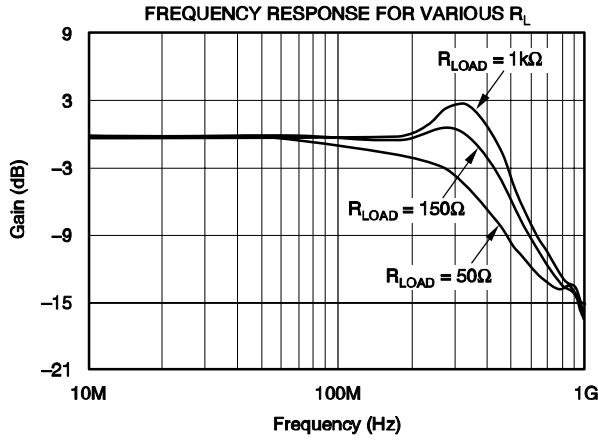
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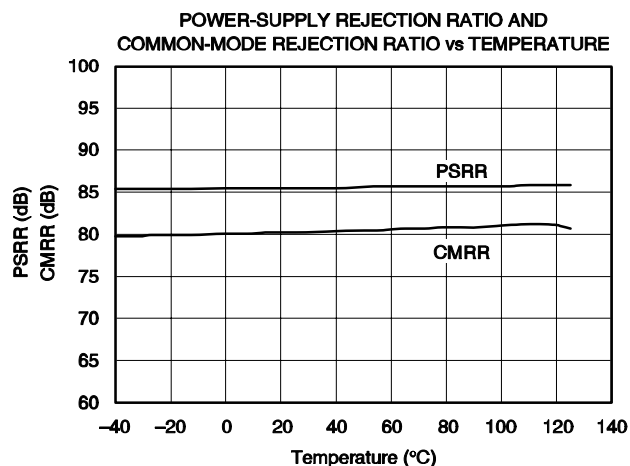
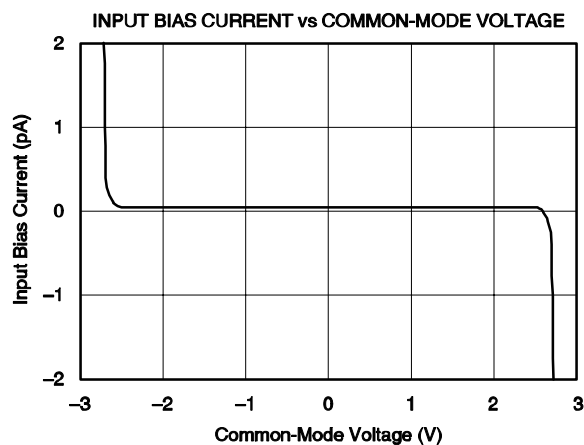
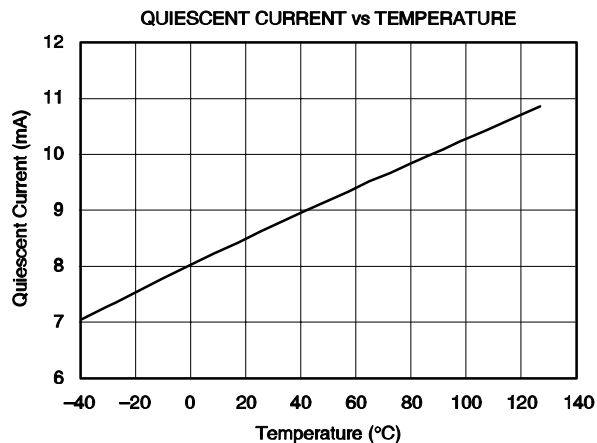
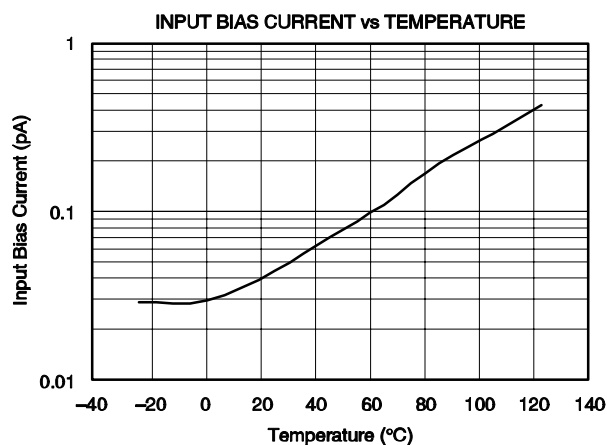
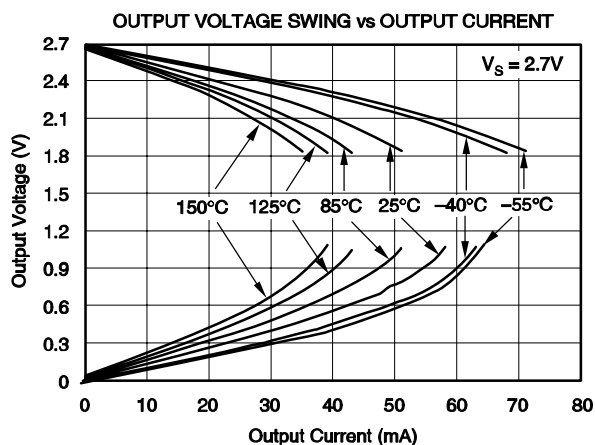
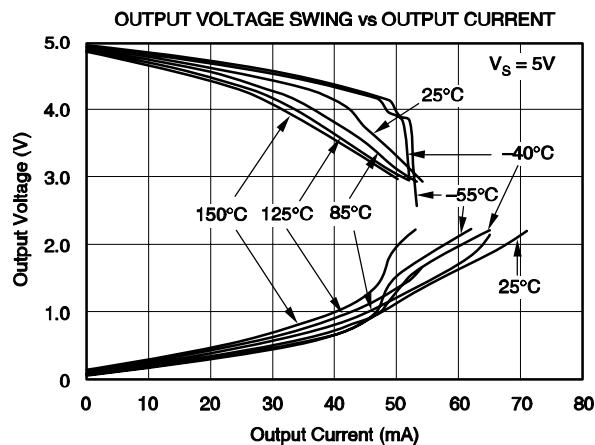
TYPICAL CHARACTERISTICS (continued)

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TYPICAL CHARACTERISTICS (continued)

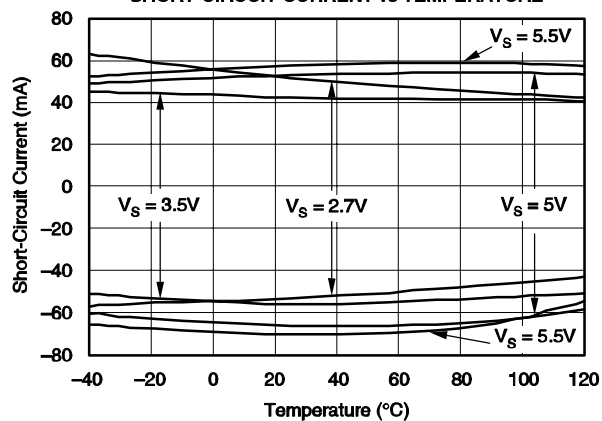
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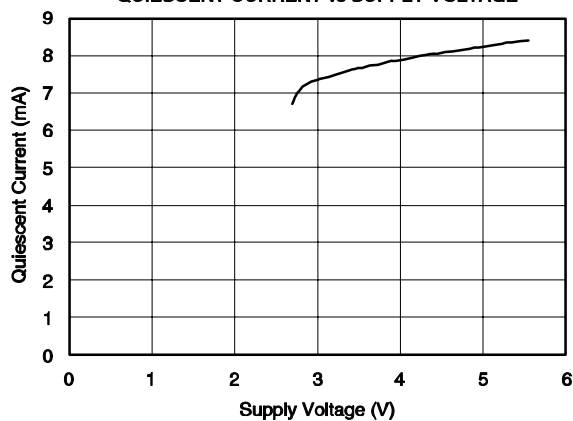
TYPICAL CHARACTERISTICS (continued)

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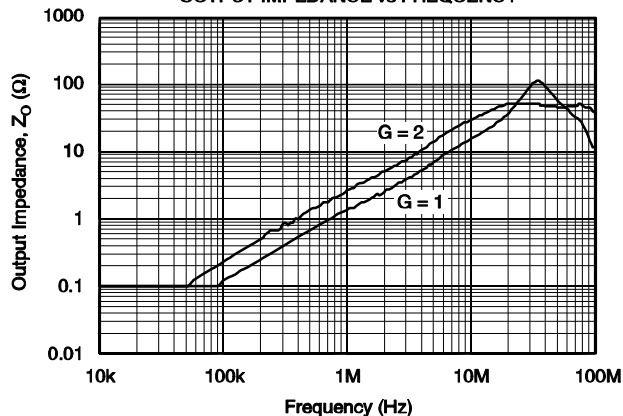
SHORT-CIRCUIT CURRENT vs TEMPERATURE



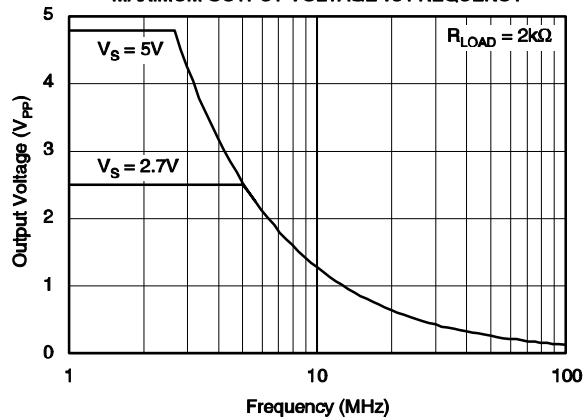
QUIESCENT CURRENT vs SUPPLY VOLTAGE



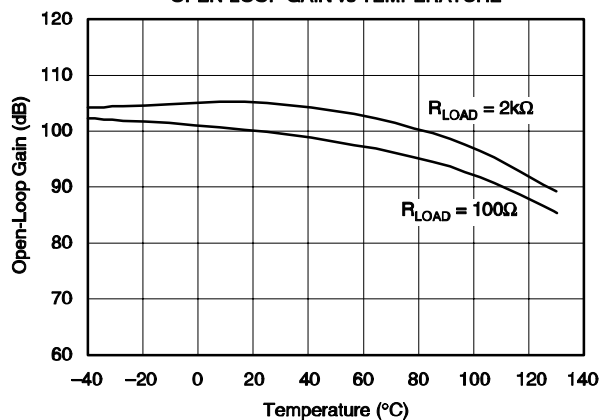
OUTPUT IMPEDANCE vs FREQUENCY



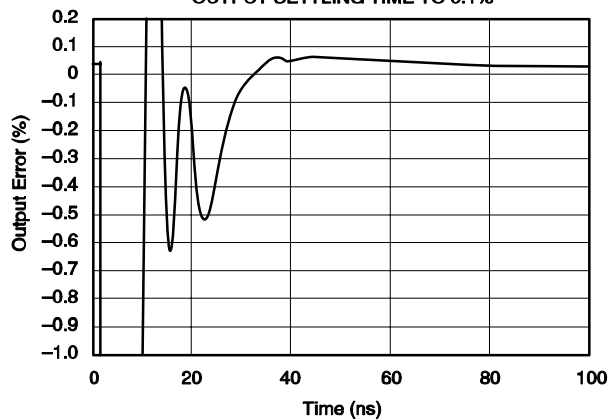
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



OPEN-LOOP GAIN vs TEMPERATURE

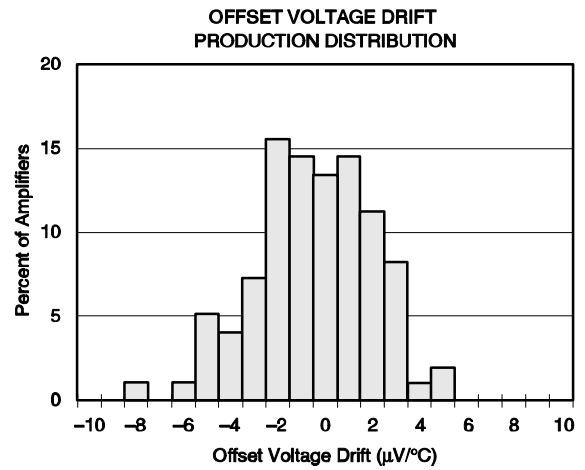
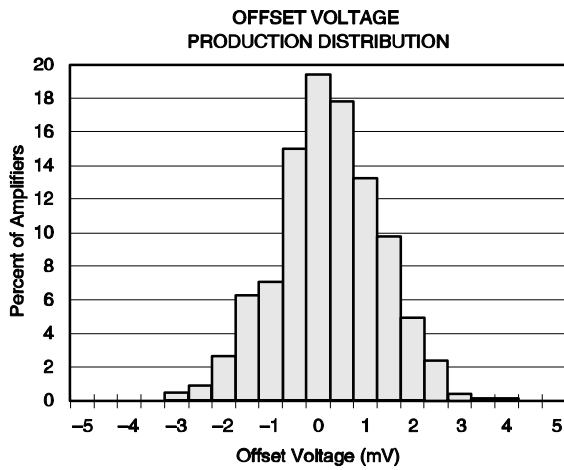


OUTPUT SETTLING TIME TO 0.1%



TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_F = 310\Omega$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.



APPLICATIONS INFORMATION

Built on HPA07, the latest TI high-precision analog process, the OPA300 single-supply CMOS op amp is designed to interface with high-speed 16-bit analog-to-digital converters (ADCs). Featuring wide 180MHz bandwidth, fast 150nS settling time to 16 bits, and high open loop gain, the OPA300 series offer excellent performance in a small SO-8 package.

THEORY OF OPERATION

The OPA300 uses a classic two-stage topology, shown in Figure 1. The differential input pair is biased to maximize slew rate without compromising stability or bandwidth. The folded cascode adds the signal from the input pair and presents a differential signal to the class AB output stage. The class AB output stage allows rail to rail output swing, with high-impedance loads ($> 2k\Omega$), typically 100mV from the supply rails. With 10 Ω loads, a useful output swing can be achieved and still maintain high open-loop gain. See the typical characteristic *Output Voltage Swing vs Output Current*.

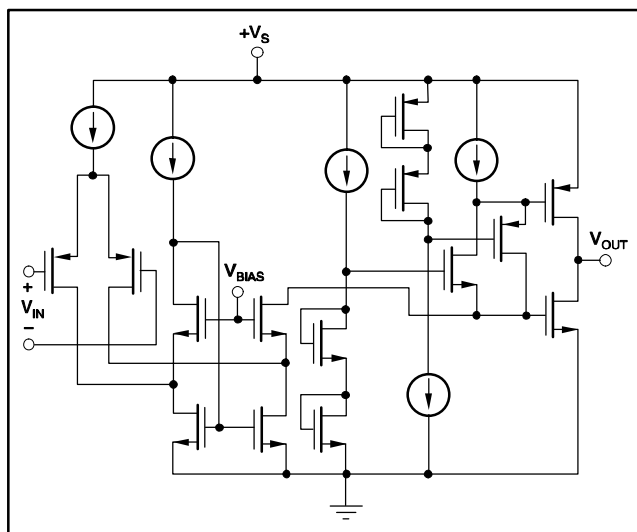


Figure 1. OPA300 Classic Two-Stage Topology

OPERATING VOLTAGE

OPA300 op amp parameters are fully specified from +2.7V to +5.5V. Supply voltages higher than 5.5V (absolute maximum) can cause permanent damage to the amplifier. Many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

PCB LAYOUT

As with most high-speed operational amplifiers, board layout requires special attention to maximize AC and DC performance. Extensive use of ground planes, short lead lengths, and high-quality bypass capacitors will minimize leakage that can compromise signal quality. Guard rings applied with potential as near to the input pins as possible help minimize board leakage.

INPUT AND ESD PROTECTION

All OPA300 pins are static protected with internal ESD protection diodes tied to the supplies, as shown in Figure 2. These diodes will provide overdrive protection if the current is externally limited to 10mA, as stated in the Absolute Maximum Ratings. Any input current beyond the Absolute Maximum Ratings, or long-term operation at maximum ratings, will shorten the lifespan of the amplifier.

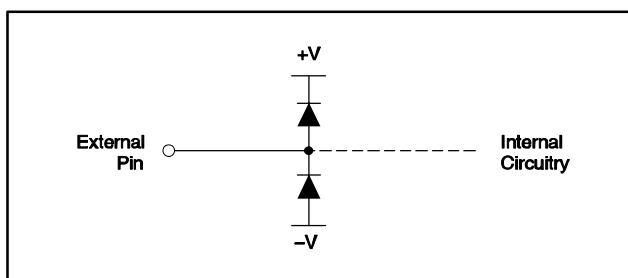


Figure 2. ESD Protection Diodes

ENABLE FUNCTION

The shutdown function of the OPA300 is referenced to the negative supply voltage of the operational amplifier. A logic level HIGH enables the op amp. A valid logic HIGH is defined as 2.5V above the negative supply applied to the enable pin. A valid logic LOW is defined as $< 0.8\text{V}$ above the negative supply pin. If dual or split power supplies are used, care should be taken to ensure logic input signals are properly referred to the negative supply voltage. If this pin is not connected to a valid high or low voltage, the internal circuitry will pull the node high and enable the part to function.

The logic input is a high-impedance CMOS input. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 μs ; disable time is 1 μs . When disabled, the output assumes a high-impedance state. This allows the OPA300 to be operated as a gated amplifier, or to have its output multiplexed onto a common analog output bus.

DRIVING CAPACITIVE LOADS

When using high-speed operational amplifiers, it is extremely important to consider the effects of capacitive loading on amplifier stability. Capacitive loading will interact with the output impedance of the operational amplifier, and depending on the capacitor value, may significantly decrease the gain bandwidth, as well as introduce peaking. To reduce the effects of capacitive loading and allow for additional capacitive load drive, place a series resistor between the output and the load. This will reduce available bandwidth, but permit stable operation with capacitive loading. Figure 3 illustrates the recommended relationship between the resistor and capacitor values.

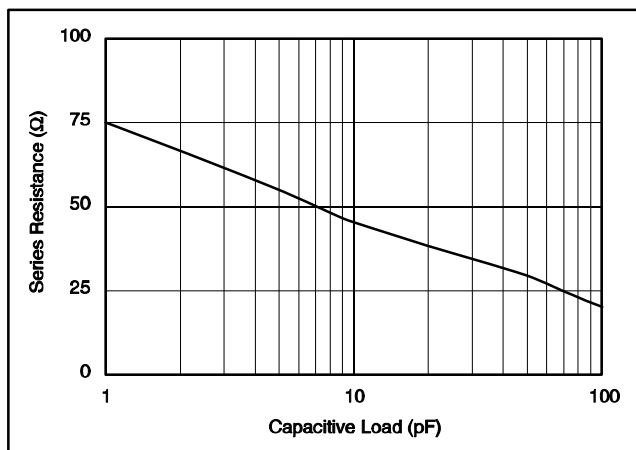


Figure 3. Recommended R_S and C_L Combinations

Amplifiers configured in unity gain are most susceptible to stability issues. The typical characteristic, *Frequency Response vs Capacitive Load*, describes the relationship between capacitive load and stability for the OPA300. In unity gain, the OPA300 is capable of driving a few picofarads of capacitive load without compromising stability. Board level parasitic capacitance can often fall into the range of a picofarad or more, and should be minimized through good circuit-board layout practices to avoid compromising the stability of the OPA300.

DRIVING A 16-BIT ADC

The OPA300 features excellent THD+noise, even at frequencies greater than 1MHz, with a 16-bit settling time of 150ns. Figure 4 shows a total single supply solution for high-speed data acquisition. The OPA300 directly drives the ADS8401, a 1.25 mega sample per second (MSPS) 16-bit data converter. The OPA300 is configured in an inverting gain of 1, with a 5V single supply. Results of the OPA300 performance are summarized in Table 1.

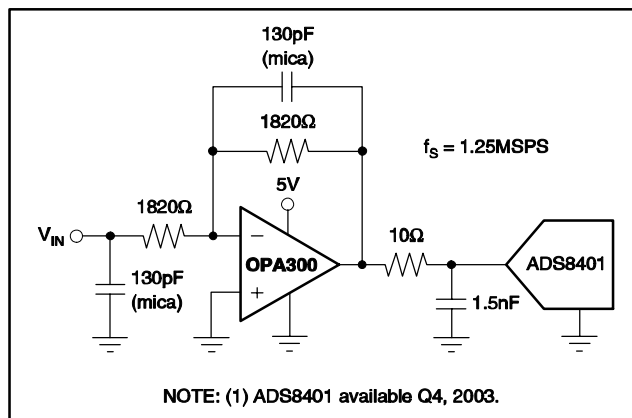
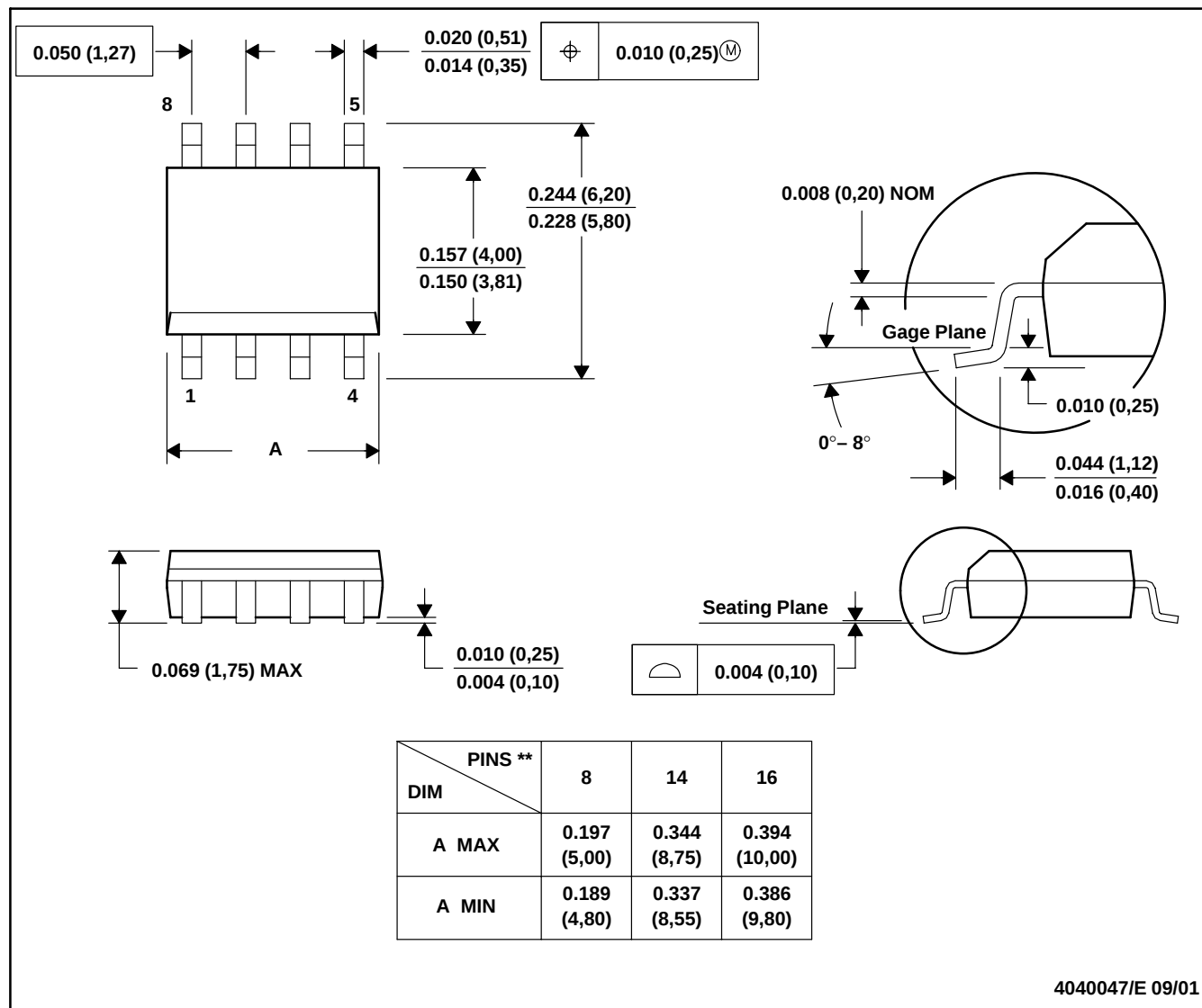


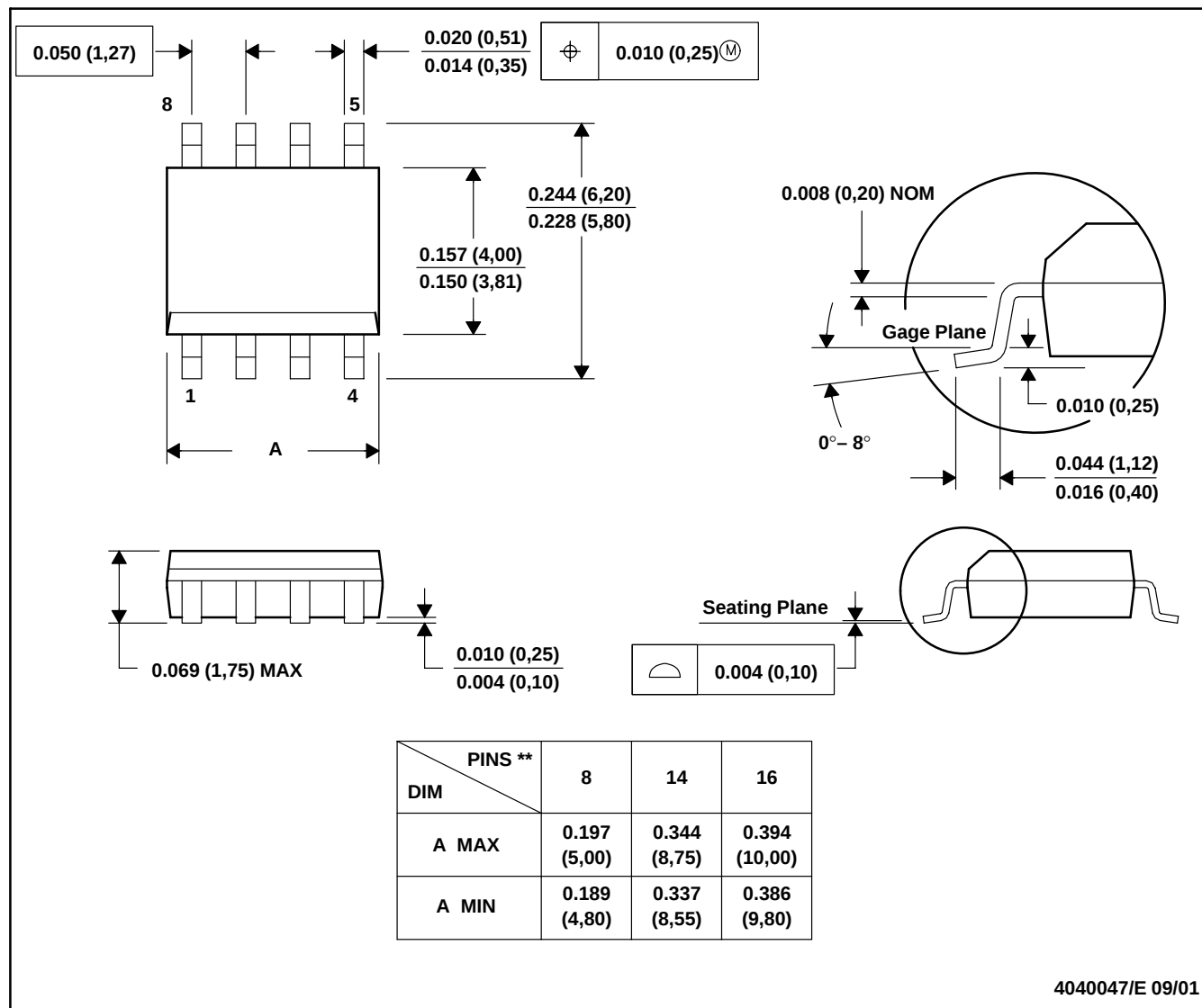
Figure 4. The OPA300 Drives the 16-Bit ADS8401

PARAMETER	RESULTS
THD+Noise	99.3dB
SFDR	101.3dB
2 nd Harmonic	107.4dB
3 rd Harmonic	103.5dB

Table 1. OPA300 Performance Results Driving a 1.25MSPS ADS8401

D (R-PDSO-G)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

D (R-PDSO-G)****PLASTIC SMALL-OUTLINE PACKAGE****8 PINS SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

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