- **Low Supply-Voltage Range, 1.8 V . . . 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 200 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in 6 μs**
- **Frequency-Locked Loop, FLL+**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **Integrated LCD Driver for 96 Segments**
- **On-Chip Comparator**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader in Flash Devices**
- **Family Members Include:**
  - **MSP430C412: 4KB ROM, 256B RAM**
  - **MSP430C413: 8KB ROM, 256B RAM**
  - **MSP430F412: 4KB + 256B Flash Memory, 256B RAM**
  - **MSP430F413: 8KB + 256B Flash Memory, 256B RAM**
- **Available in 64-Pin Quad Flat Pack (QFP)**
- **For Complete Module Descriptions, Refer to the MSP430x4xx Family User's Guide, Literature Number SLAU056**

description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6μs.

The MSP430x41x series are microcontroller configurations with one built-in 16-bit timer, a comparator, 96 LCD segment drive capability, and 48 I/O pins.

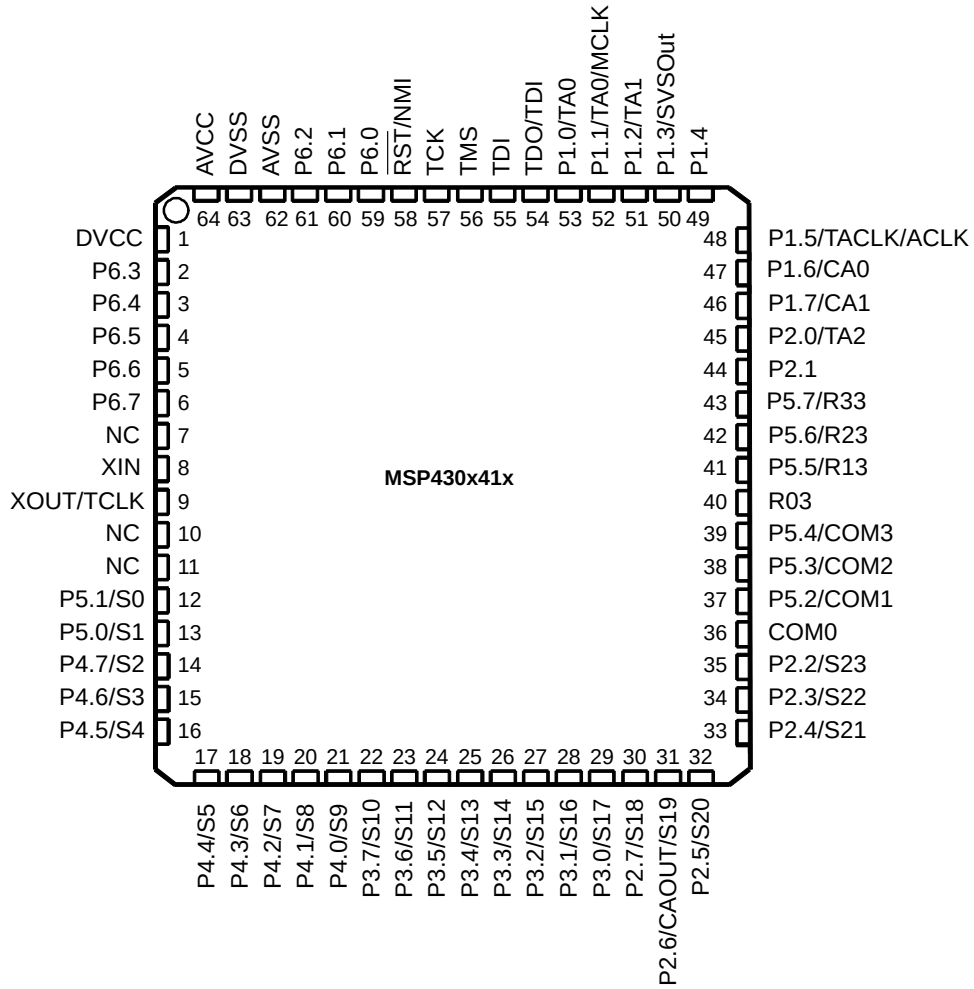
Typical applications include sensor systems that capture analog signals, convert them to digital values, and process the data and transmit them to a host system. The comparator and timer make the configurations ideal for industrial meters, counter applications, handheld meters, etc.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
–40°C to 85°C	MSP430C412IPM MSP430C413IPM MSP430F412IPM MSP430F413IPM

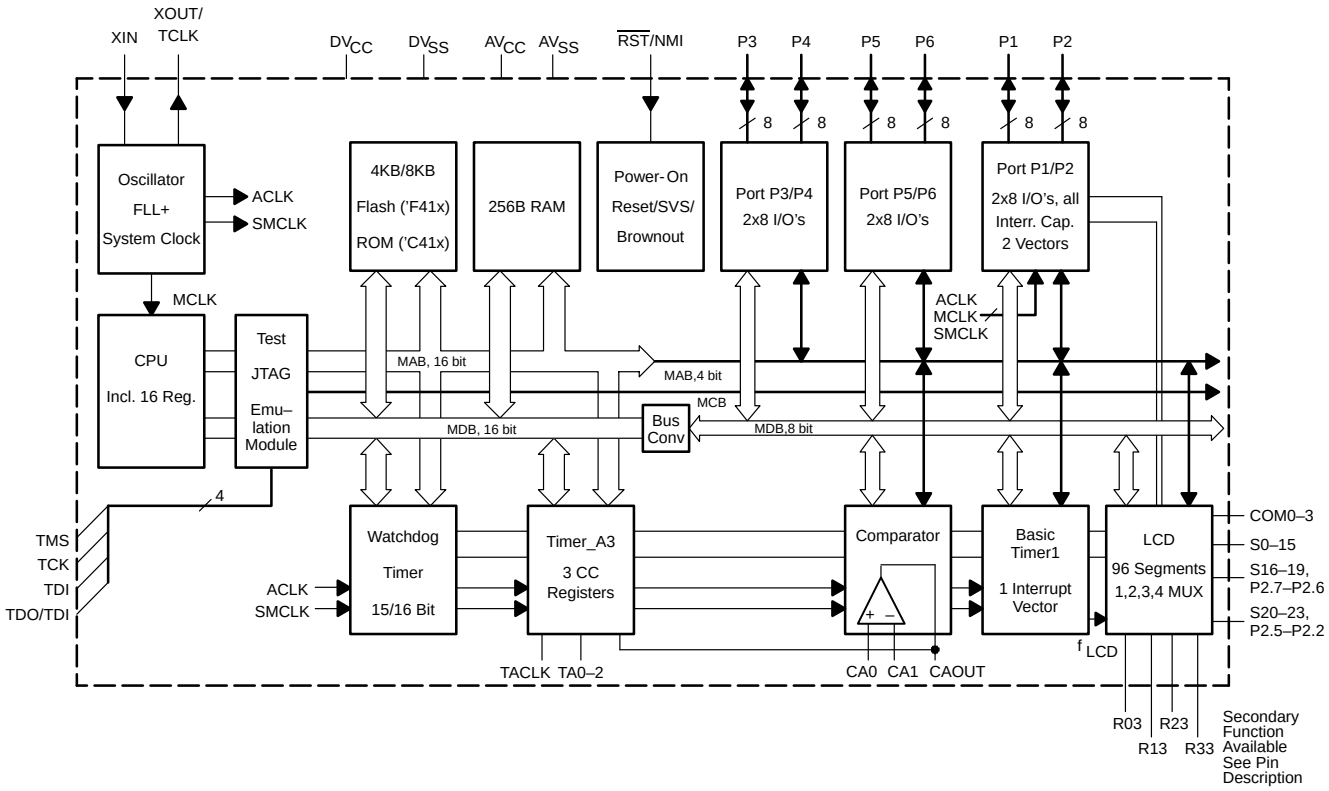
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

pin designation, MSP430x41x



NC – No internal connection

functional block diagrams



Terminal Functions

MSP430x41x

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{CC}	64		Positive terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DVCC.
AV_{SS}	62		Negative terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A. Needs to be externally connected to DVSS.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all parts, except those which are supplied via AVCC.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AVCC/AVSS.
NC	7, 10, 11		No connection
P1.0/TA0	53	I/O	General-purpose digital I/O/Timer_A. Capture: CCI0A input, compare: Out0 output
P1.1/TA0/MCLK	52	I/O	General-purpose digital I/O/Timer_A. Capture: CCI0B input/MCLK output. Note: TA0 is only an input on this pin.
P1.2/TA1	51	I/O	General-purpose digital I/O/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/SVSOut	50	I/O	General-purpose digital I/O/SVS: output of SVS comparator
P1.4	49	I/O	General-purpose digital I/O
P1.5/TACLK/ ACLK	48	I/O	General-purpose digital I/O/input of Timer_A clock/output of ACLK
P1.6/CA0	47	I/O	General-purpose digital I/O/Comparator_A input
P1.7/CA1	46	I/O	General-purpose digital I/O/Comparator_A input
P2.0/TA2	45	I/O	General-purpose digital I/O/ Timer_A capture: CCI2A input, compare: Out2 output
P2.1	44	I/O	General-purpose digital I/O
P2.2/S23	35	I/O	General-purpose digital I/O/LCD segment output 23 (see Note 1)
P2.3/S22	34	I/O	General-purpose digital I/O/LCD segment output 22 (see Note 1)
P2.4/S21	33	I/O	General-purpose digital I/O/LCD segment output 21 (see Note 1)
P2.5/S20	32	I/O	General-purpose digital I/O/LCD segment output 20 (see Note 1)
P2.6/CAOUT/S19	31	I/O	General-purpose digital I/O/Comparator_A output/LCD segment output 19 (see Note 1)
P2.7/S18	30	I/O	General-purpose digital I/O/LCD segment output 18 (see Note 1)
P3.0/S17	29	I/O	General-purpose digital I/O/ LCD segment output 17 (see Note 1)
P3.1/S16	28	I/O	General-purpose digital I/O/ LCD segment output 16 (see Note 1)
P3.2/S15	27	I/O	General-purpose digital I/O/ LCD segment output 15 (see Note 1)
P3.3/S14	26	I/O	General-purpose digital I/O/ LCD segment output 14 (see Note 1)
P3.4/S13	25	I/O	General-purpose digital I/O/LCD segment output 13 (see Note 1)
P3.5/S12	24	I/O	General-purpose digital I/O/LCD segment output 12 (see Note 1)
P3.6/S11	23	I/O	General-purpose digital I/O/LCD segment output 11 (see Note 1)
P3.7/S10	22	I/O	General-purpose digital I/O/LCD segment output 10 (see Note 1)

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

Terminal Functions (Continued)

MSP430x41x

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P4.0/S9	21	I/O	General-purpose digital I/O/LCD segment output 9 (see Note 1)
P4.1/S8	20	I/O	General-purpose digital I/O/LCD segment output 8 (see Note 1)
P4.2/S7	19	I/O	General-purpose digital I/O/LCD segment output 7 (see Note 1)
P4.3/S6	18	I/O	General-purpose digital I/O/LCD segment output 6 (see Note 1)
P4.4/S5	17	I/O	General-purpose digital I/O/LCD segment output 5 (see Note 1)
P4.5/S4	16	I/O	General-purpose digital I/O/LCD segment output 4 (see Note 1)
P4.6/S3	15	I/O	General-purpose digital I/O/LCD segment output 3 (see Note 1)
P4.7/S2	14	I/O	General-purpose digital I/O/LCD segment output 2 (see Note 1)
P5.0/S1	13	I/O	General-purpose digital I/O/LCD segment output 1 (see Note 1)
P5.1/S0	12	I/O	General-purpose digital I/O/LCD segment output 0 (see Note 1)
COM0	36	O	Common output. COM0–3 are used for LCD backplanes
P5.2/COM1	37	I/O	General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes
P5.3/COM2	38	I/O	General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes
P5.4/COM3	39	I/O	General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes
R03	40	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	41	I/O	General-purpose digital I/O/input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	42	I/O	General-purpose digital I/O/input port of second most positive analog LCD level (V2)
P5.7/R33	43	I/O	General-purpose digital I/O/output port of most positive analog LCD level (V1)
P6.0	59	I/O	General-purpose digital I/O
P6.1	60	I/O	General-purpose digital I/O
P6.2	61	I/O	General-purpose digital I/O
P6.3	2	I/O	General-purpose digital I/O
P6.4	3	I/O	General-purpose digital I/O
P6.5	4	I/O	General-purpose digital I/O
P6.6	5	I/O	General-purpose digital I/O
P6.7	6	I/O	General-purpose digital I/O
$\overline{\text{RST}}$/NMI	58	I	Reset input or nonmaskable interrupt input port
TCK	57	I	Test clock. TCK is the clock input port for device programming and test.
TDI	55	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ——> R5
Single operands, destination only	e.g. CALL R8	PC —>(TOS), R8—> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	✓	✓	MOV and MEM,and TCDAT		M(MEM) —> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    FLL+ Loop control remains active
- Low-power mode 1 (LPM1);
  - CPU is disabled
    FLL+ Loop control is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and FLL+ loop control and DCOCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM with an address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
Comparator_A	CMPAIFG	Maskable	0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
Timer_A3	TACCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 (see Notes 1 and 2) To P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 (see Notes 1 and 2) To P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt-enable cannot.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

Address	7	6	5	4	3	2	1	0
1h	BTIE							
	rw-0							

WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable

BTIE: Basic Timer1 interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-0

Address	7	6	5	4	3	2	1	0
3h	BTIFG							
	rw-0							

WDTIFG: Set on watchdog-timer overflow (in watchdog mode) or security key violation. Reset with V_{CC} power-up, or a reset condition at the $\overline{\text{RST}}$/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{\text{RST}}$/NMI pin

BTIFG: Basic Timer1 interrupt flag

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h/05h								

Legend: rw: Bit Can Be Read and Written
rw-0: Bit Can Be Read and Written. It Is Reset by PUC.
SFR Bit Not Present in Device

memory organization

		MSP430F412	MSP430C412	MSP430F413	MSP430C413
Memory	Size	4kB	4kB	8kB	8kB
Interrupt vector	Flash/ROM	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h
Code memory	Flash/ROM	0FFFFh – 0F000h	0FFFFh – 0F000h	0FFFFh – 0E000h	0FFFFh – 0E000h
Information memory	Size	256 Byte	NA	256 Byte	NA
		010FFh – 01000h	NA	010FFh – 01000h	NA
Boot memory	Size	1kB	NA	1kB	NA
		0FFFh – 0C00h	NA	0FFFh – 0C00h	NA
RAM	Size	256 Byte	256 Byte	256 Byte	256 Byte
		02FFh – 0200h	02FFh – 0200h	02FFh – 0200h	02FFh – 0200h
Peripherals	16-bit	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h
	8-bit	0FFh – 010h	0FFh – 010h	0FFh – 010h	0FFh – 010h
	8-bit SFR	0Fh – 00h	0Fh – 00h	0Fh – 00h	0Fh – 00h

bootstrap loader (BSL)

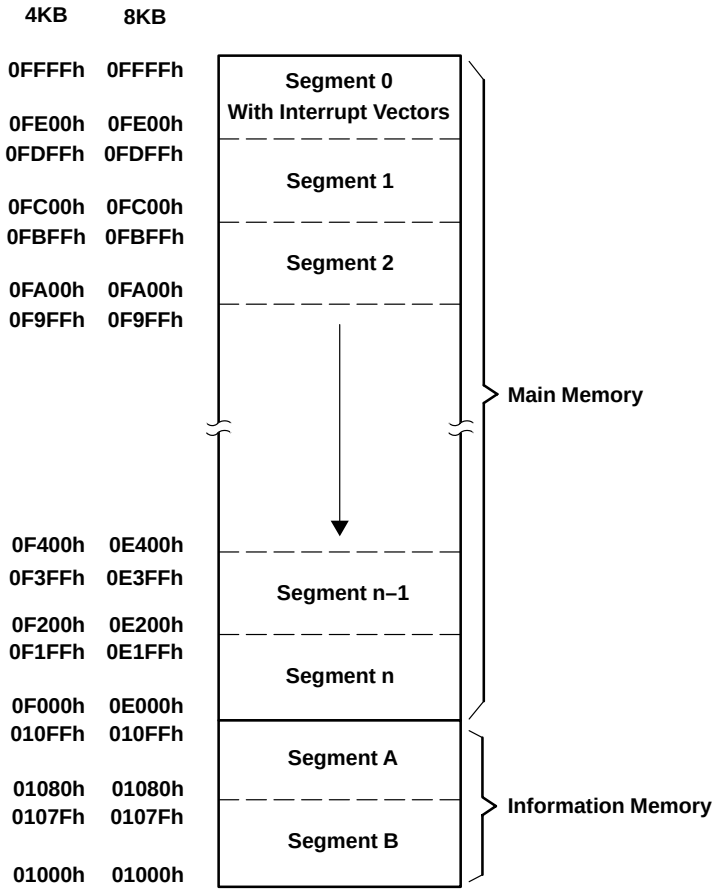
The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n.
  Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

flash memory (continued)



peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions.

oscillator and system clock

The clock system in the MSP430x41x family of devices is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

Basic Timer1

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

LCD drive

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

comparator_A

The primary function of the comparator_A module is to support precision slope analog–to–digital conversions, battery–voltage supervision, and monitoring of external analog signals.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Capture/compare control 0	TACCTL0	0162h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 2	TACCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A register	TAR	0170h
	Capture/compare register 0	TACCR0	0172h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 2	TACCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
PERIPHERALS WITH BYTE ACCESS			
LCD	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Brownout, SVS	SVS control register	SVSCTL	056h
FLL+ Clock	FLL+ Control1	FLL_CTL1	054h
	FLL+ Control0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter2	BTCNT2	047h
	BT counter1	BTCNT1	046h
	BT control	BTCTL	040h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS} (see Note 1) . . . . . –0.3 V to + 4.1 V
Voltage applied to any pin (referenced to V_{SS}) (see Note 1) . . . . . –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature (unprogrammed device) . . . . . –55°C to 150°C
Storage temperature (programmed device) . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages referenced to V_{SS}.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNITS
Supply voltage during program execution, SVS disabled V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430x41x	1.8		3.6	V
Supply voltage during program execution, SVS enabled (see Note 1), V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430x41x	2.2		3.6	V
Supply voltage during programming flash memory, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430F413	2.7		3.6	V
Supply voltage, V_{SS} (AV_{SS} = DV_{SS} = V_{SS})			0		0	V
Operating free-air temperature range, T_A		MSP430x41x	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF selected, XTS_FLL=0	Watch crystal		32768		Hz
	XT1 selected, XTS_FLL=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS_FLL=1	Crystal	1000		8000	kHz
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	
Flash-timing-generator frequency, $f_{(FTG)}$		MSP430F413	257		476	kHz
Cumulative program time, $t_{(CPT)}$ (see Note 3)		V_{CC} = 2.7 V/3.6 V MSP430F413			3	ms
Cumulative mass erase time, $t_{(CMEras)}$ (see Note 4)		V_{CC} = 2.7 V/3.6 V MSP430F413	200			ms
Input levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V XTS_FLL=1	V_{SS}		$0.2 \times V_{CC}$	V
	$V_{IH(Xin, Xout)}$		$0.8 \times V_{CC}$		V_{CC}	

NOTES: 1. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing supply voltage. POR is going inactive when the supply voltage is raised above minimum supply voltage plus the hysteresis of the SVS circuitry.
2. The LFXT1 oscillator in LF-mode requires a watch crystal.
3. The cumulative program time must not be exceeded during a block-write operation.
4. The mass-erase duration generated by the flash timing generator is at least 11.1 ms. The cummulative mass-erase time needed is 200 ms. This can be achieved by repeating the mass-erase operation until the cumulative mass-erase time is met (a minimum of 19 cycles may be required).

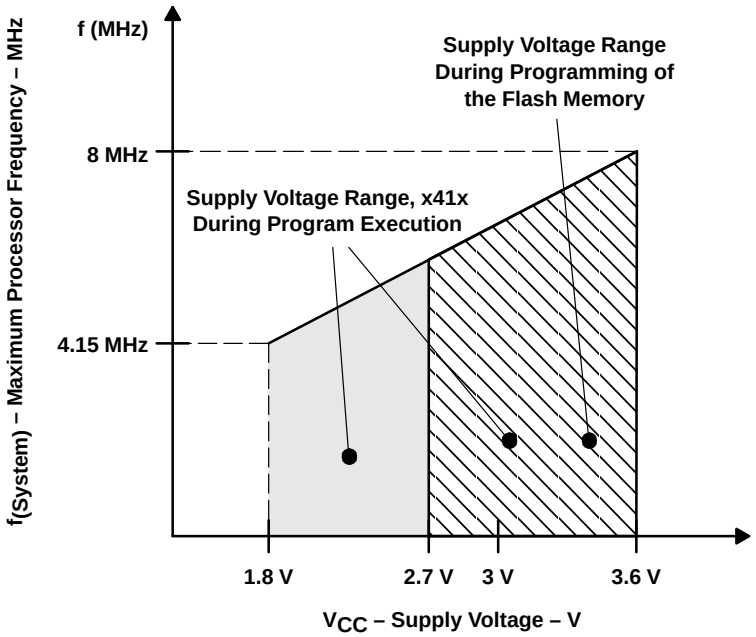


Figure 1. Frequency vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current, (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, XTS_FLL = 0 (F41x: Program executes in flash)	C41x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		160	200	µA
				V_{CC} = 3 V		240	300	
		F41x	T_A = –40°C to 85°C	V_{CC} = 2.2 V		200	250	
				V_{CC} = 3 V		300	350	
$I_{(LPM0)}$	Low-power mode, (LPM0) FN_8=FN_4=FN_3=FN_2=0		T_A = –40°C to 85°C	V_{CC} = 2.2 V		32	45	µA
				V_{CC} = 3 V		55	70	
$I_{(LPM2)}$	Low-power mode, (LPM2),		T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
				V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) (see Note 2)		T_A = –40°C	V_{CC} = 2.2 V		0.95	1.4	µA
			T_A = –10°C			0.8	1.3	
			T_A = 25°C			0.7	1.2	
			T_A = 60°C			0.95	1.4	
			T_A = 85°C			1.6	2.3	
			T_A = –40°C	V_{CC} = 3 V		1.1	1.7	
			T_A = –10°C			1.0	1.6	
			T_A = 25°C			0.9	1.5	
			T_A = 60°C			1.1	1.7	
			T_A = 85°C			2.0	2.6	
$I_{(LPM4)}$	Low-power mode, (LPM4)		T_A = –40°C	V_{CC} = 2.2 V/3 V		0.1	0.5	µA
			T_A = 25°C			0.1	0.5	
			T_A = 85°C			0.8	2.5	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2, LPM3, and LPM4 are measured with active Basic Timer1 and LCD (ACLK selected).
The current consumption of the Comparator_A and the SVS module are specified in the respective sections.
2. The LPM3 currents are characterized with a KDS Daishinku DT–38 (6 pF) crystal.

current consumption of active mode versus system frequency, F version

$$I_{(AM)} = I_{(AM)\ [1\ MHz]} \times f_{(System)\ [MHz]}$$

current consumption of active mode versus supply voltage, F version

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 140\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1, P2, P3, P4, P5, and P6; $\overline{\text{RST}}$/NMI; JTAG: TCK, TMS, TDI, TDO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.45		1	

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±24 mA to satisfy the maximum specified voltage drop.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

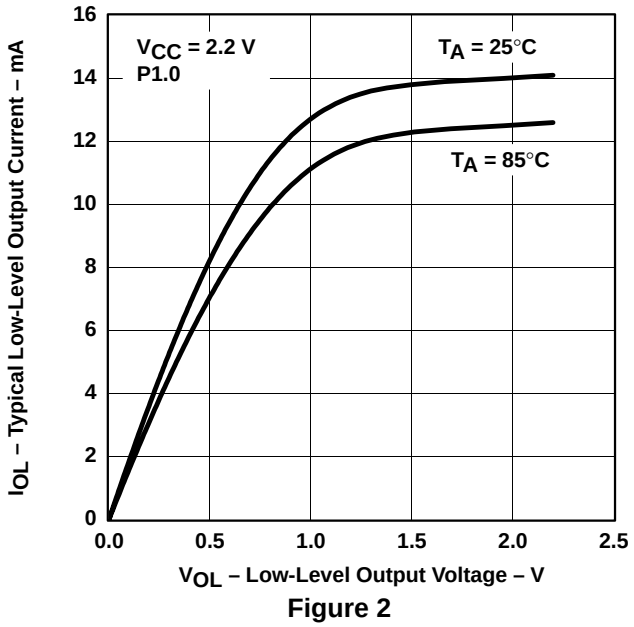


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

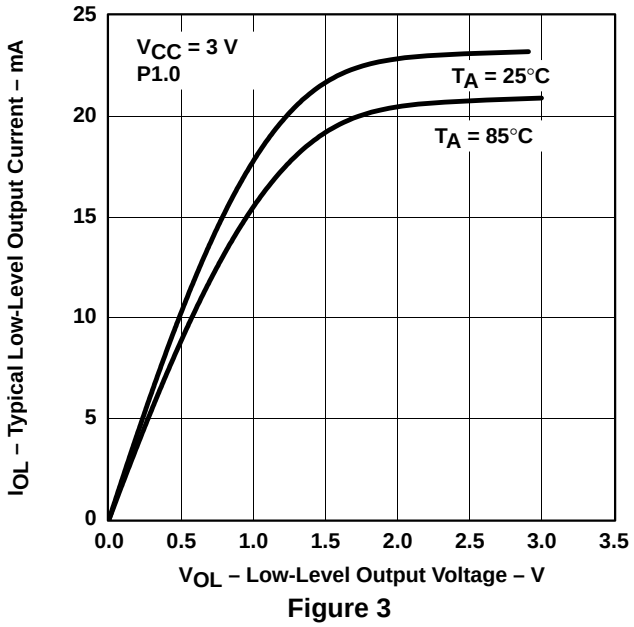


Figure 3

NOTE A: One output loaded at a time

outputs – Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

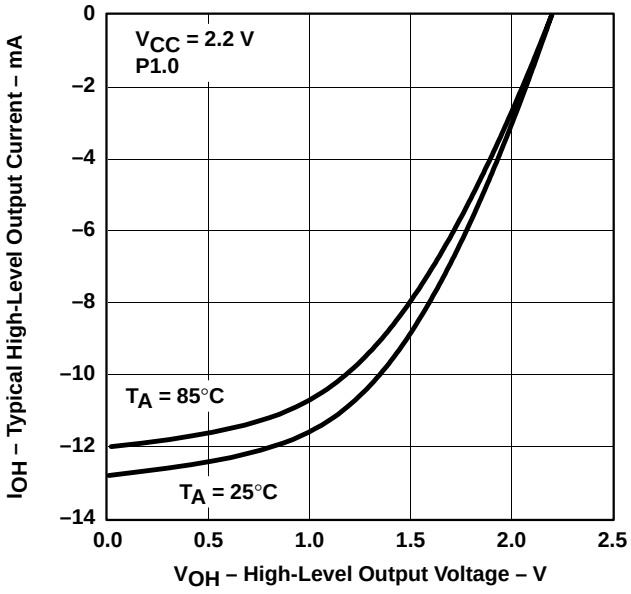


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

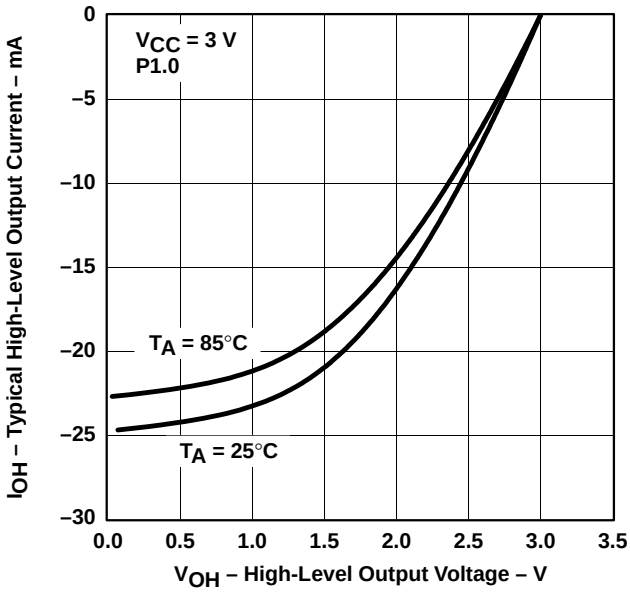


Figure 5

NOTE A: One output loaded at a time

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, capture timing	TA0, TA1, TA2 (see Note 2)	2.2 V/3 V	1.5			cycle
			2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
			3 V			10	
$f_{(TAint)}$	Timer_A clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.

2. The external capture signal triggers the capture event every time the mimimum $t_{(cap)}$ cycle and time parameters are met. A capture may be triggered with capture signals even shorter than $t_{(cap)}$. Both the cycle and timing specifications must be met to ensure a correct capture of the 16-bit timer value and to ensure the flag is set.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{Px.y}$	(1 ≤ x ≤ 6, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ± 1.5mA	V_{CC} = 2.2 V	DC		10	MHz
			V_{CC} = 3 V	DC		12	
f_{ACLK}, f_{MCLK}, f_{SMCLK}	P1.1/TA0/MCLK, P1.5/TACLK/ACLK	C_L = 20 pF	V_{CC} = 2.2 V			8	MHz
			V_{CC} = 3 V			12	
t_{Xdc}	Duty cycle of output frequency	P1.5/TACLK/ACLK, C_L = 20 pF V_{CC} = 2.2 V / 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{MCLK} = f_{LFXT1/n}$	50%– 15 ns	50%	50%+ 15 ns	
			$f_{MCLK} = f_{DCOCLK}$	50%– 15 ns	50%	50%+ 15 ns	

wake-up LPM3 (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(LPM3)}$	Delay time	V_{CC} = 2.2 V/3 V			6	µs

NOTE 1: The delay time $t_{(LPM3)}$ is independent of the system frequency and V_{CC}.

leakage current (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA
$I_{lkg(P6.x)}$		Port P6	Port 6: $V_{(P6.x)}$ (see Note 2)				±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as an input.

RAM (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in the program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

LCD

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at P5.7/R33	V_{CC} = 3 V	2.5		V_{CC} +0.2	V
$V_{(23)}$		Voltage at P5.6/R23			$(V_{33}–V_{03}) \times 2/3 + V_{03}$		
$V_{(13)}$		Voltage at P5.5/R13			$(V_{(33)}–V_{(03)}) \times 1/3 + V_{(03)}$		
$V_{(33)} – V_{(03)}$		Voltage at R33/R03		2.5		V_{CC} +0.2	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		P5.5/R13 = $V_{CC}/3$				±20	
$I_{(R23)}$		P5.6/R23 = $2 \times V_{CC}/3$				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$ = –3 µA,	V_{CC} = 3 V	$V_{(03)}$		$V_{(03)}$ – 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ – 0.1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ – 0.1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ + 0.1	

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON = 1, CARSEL = 0, CAREF = 0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P1.6/CA0/TA1 and P1.7/CA1/TA2	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2V / 3 V	0.47	0.48	0.50	
$V_{(RefVT)}$		PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1; T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3.0 V	400	490	550	
$V_{(IC)}$	Common-mode input voltage range	CAON = 1	V_{CC} = 2. 2V/3 V	0		V_{CC}–1.0	V
$V_{(offset)}$	Offset voltage	See Note 2	VCC = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	V_{CC} = 2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	160	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3.0 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

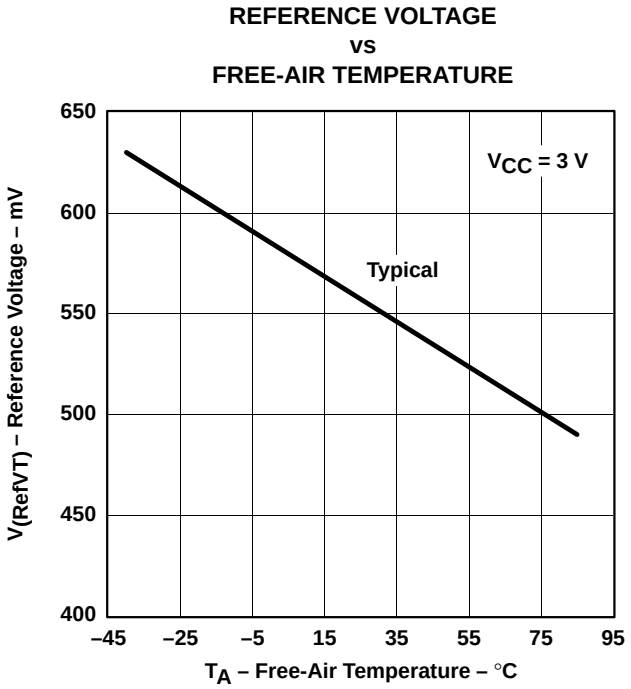


Figure 6

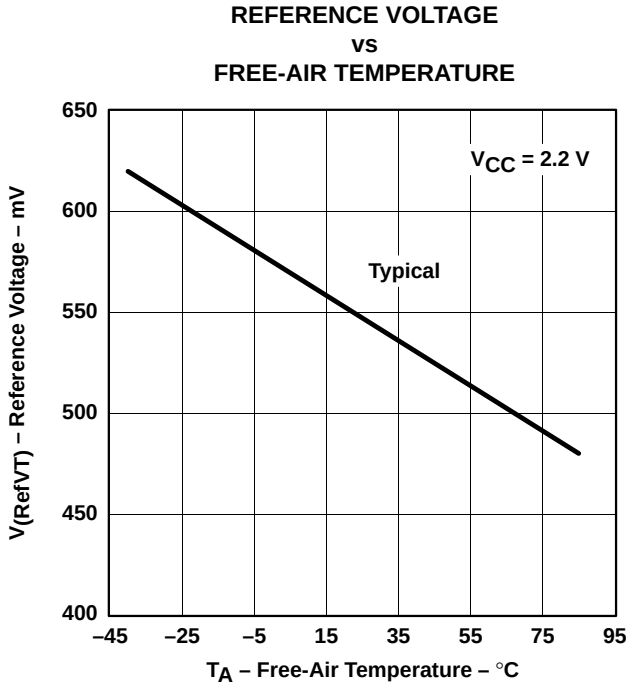


Figure 7

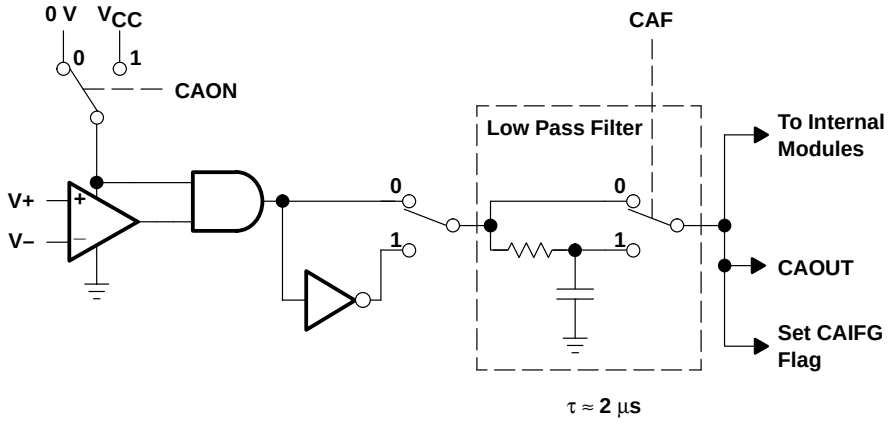


Figure 8. Block Diagram of Comparator_A Module

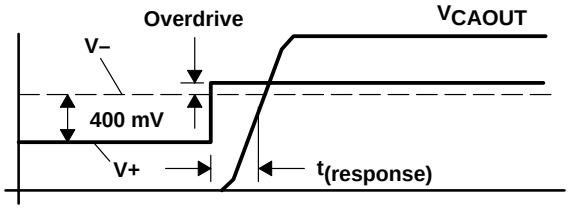


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR brownout, reset (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10, Figure 11, Figure 12)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout/SVS circuit.

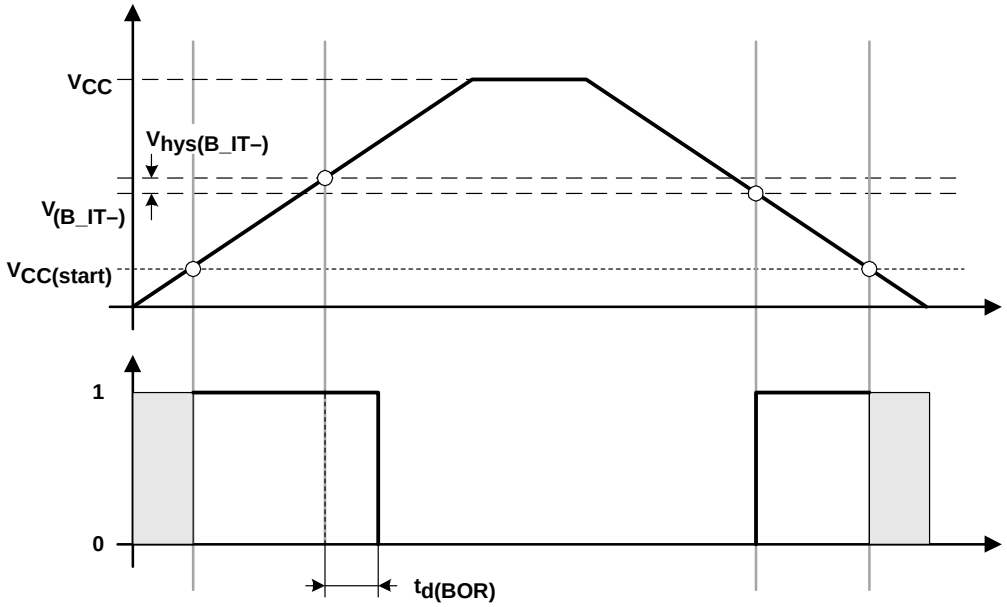


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

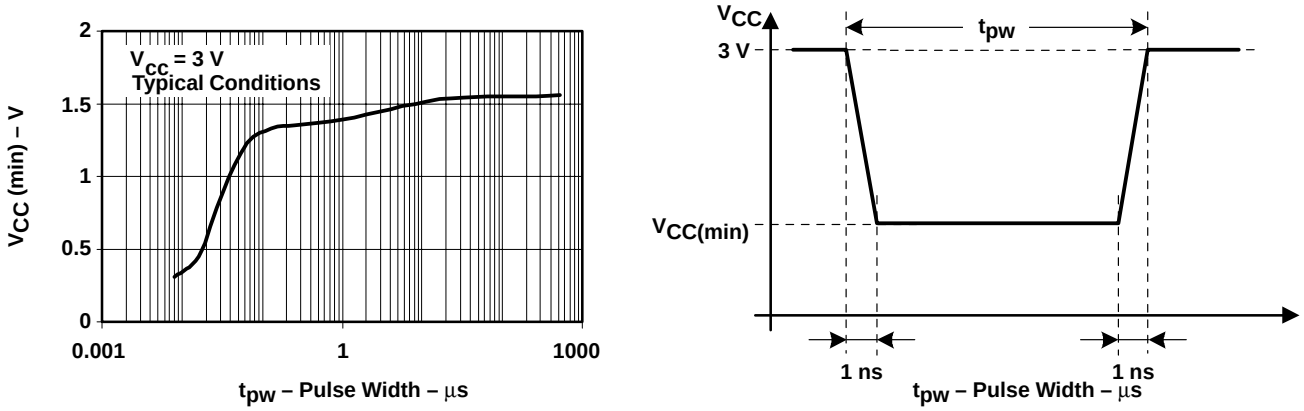


Figure 11. $V_{CC(min)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

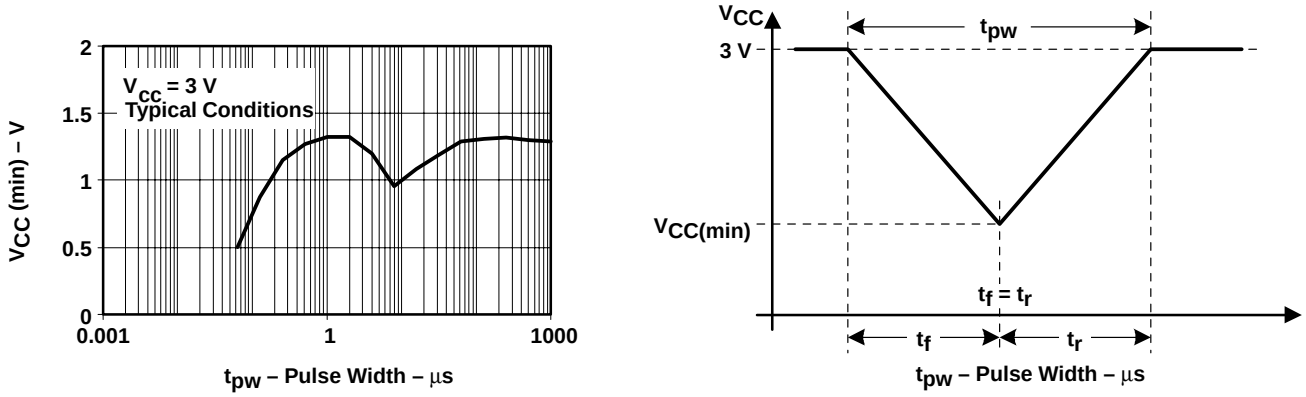


Figure 12. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

SVS (supply voltage supervisor), reset (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SVSR)}$	SVS	dV_{CC}/dt > 30V/ms (see Note 2)	5		150	μs
		$dV_{CC}/dt \le$ 30V/ms (see Note 2)			2000	μs
$t_{d(SVSon)}$		SVSon, switch from 0 to 1, V_{CC} = 3 V (see Note 2)	20		150	μs
$V_{(SVSstart)}$		$dV_{CC}/dt \le$ 3 V/s (see Figure 13)		1.55	1.7	V
$V_{(SVS\_IT-)}$		$dV_{CC}/dt \le$ 3 V/s (see Figure 13)	1.8	1.95	2.2	V
$V_{hys(SVS\_IT-)}$		$dV_{CC}/dt \le$ 3 V/s (see Figure 13)	70	100	155	mV
$I_{CC(SVS)}$ (see Note 1)		VLD ≠ 0 (VLD bits are in SVSCTL register), V_{CC} = 2.2V/ 3V		10	15	μA

NOTES: 1. The current consumption of the SVS module is not included in the I_{CC} current consumption data.
2. The SVS is not active at power up.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

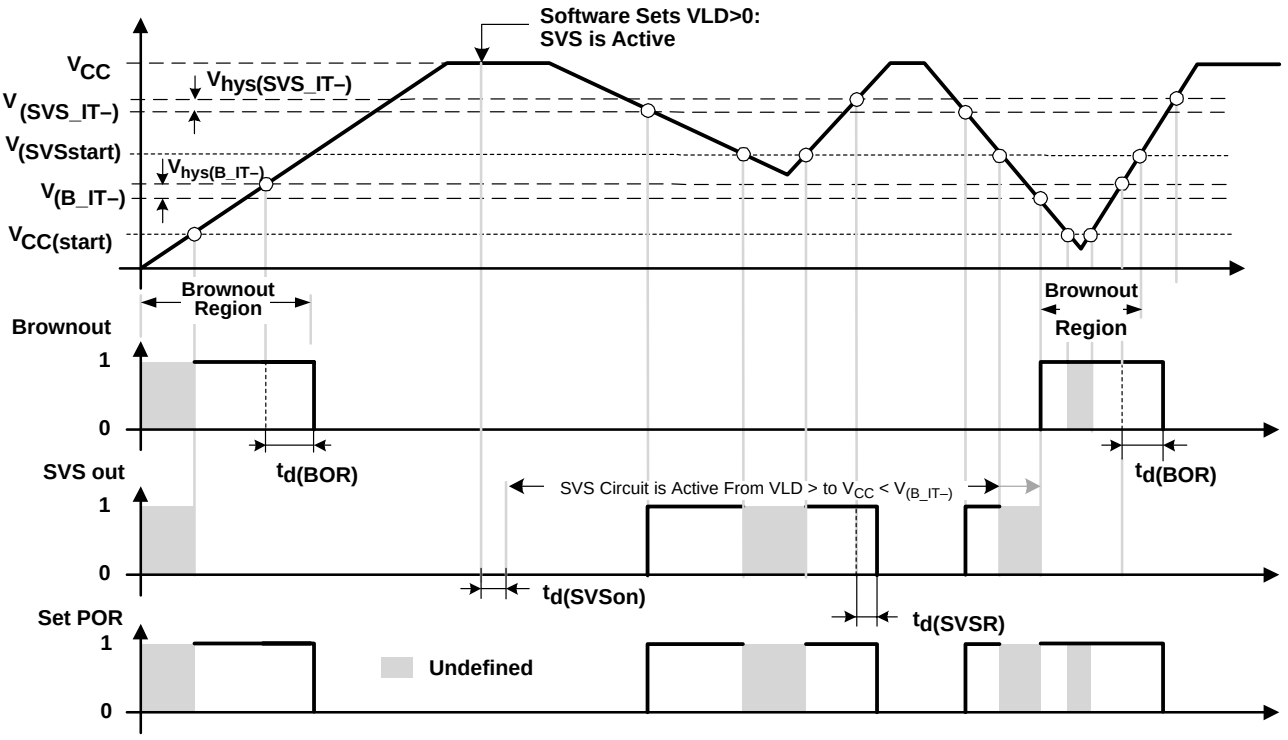


Figure 13. SVS Reset (SVSR) vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

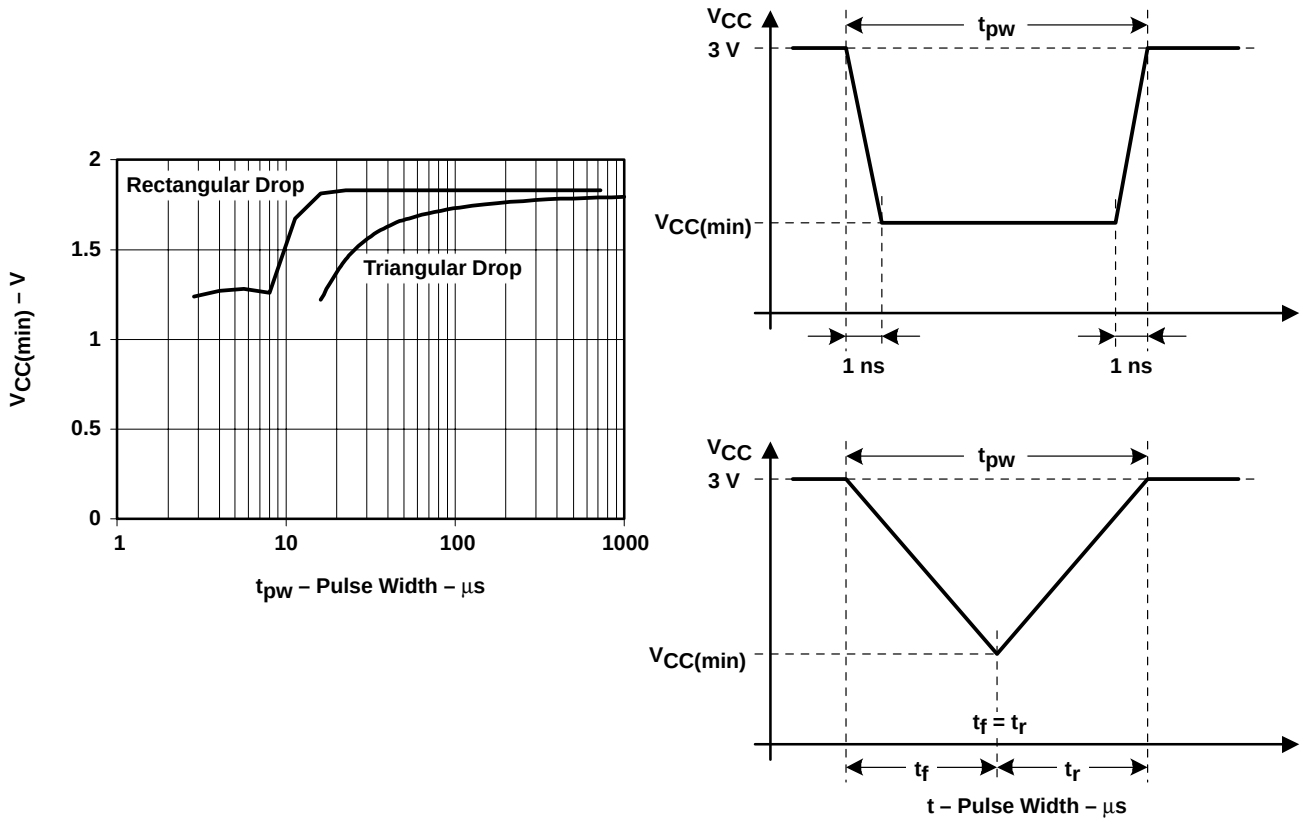


Figure 14. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01E0h, FN_8=FN_4=FN_3=FN_2=0, D = 2, DCOPLUS= 0	2.2 V/3 V		1		MHz
$f_{(DCO2)}$	FN_8=FN_4=FN_3=FN_2=0 , DCO+ = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=FN_2=0, DCO+ = 1, (see Note 1)	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCO+ = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCO+ = 1, (see Note 1)	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCO+ = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x;, DCO+ = 1, (see Note 1)	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCO+ = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCO+ = 1, (see Note 1)	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCO+ = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO27)}$	FN_8=1,FN_4=FN_3=FN_2=x,DCO+ = 1, (see Note 1)	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S	$f_{(NDCO)+1} = f_{(NDCO)}$	2 < TAP ≤ 20	1.07		1.13	
		TAP > 20	1.1		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2, DCO+ = 0, (see Note 2)	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2, DCO+ = 0 (see Note 2)		0	5	15	%/V

NOTES: 1. Do not exceed the maximum system frequency.
2. This parameter is not production tested.

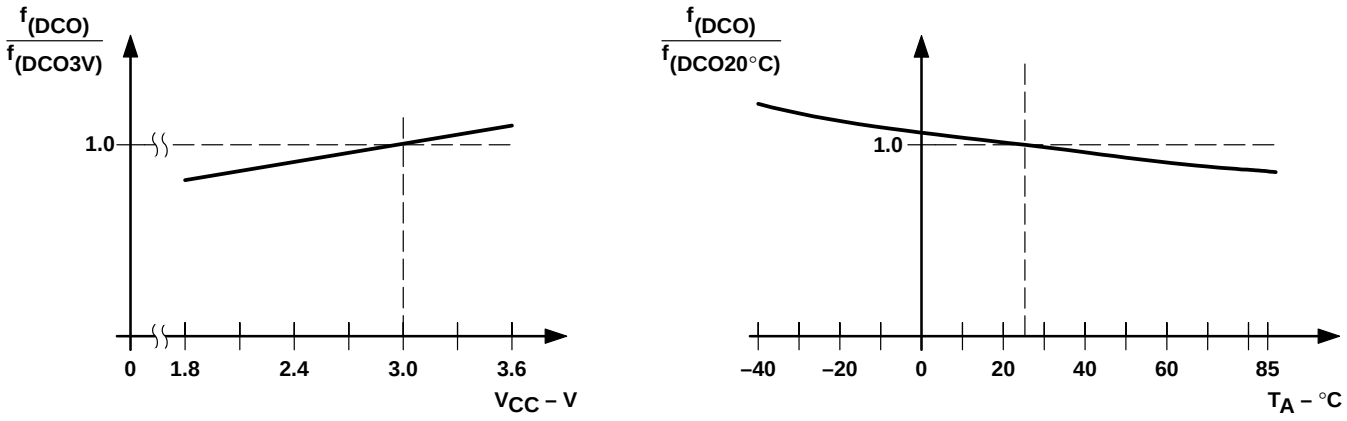


Figure 15. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

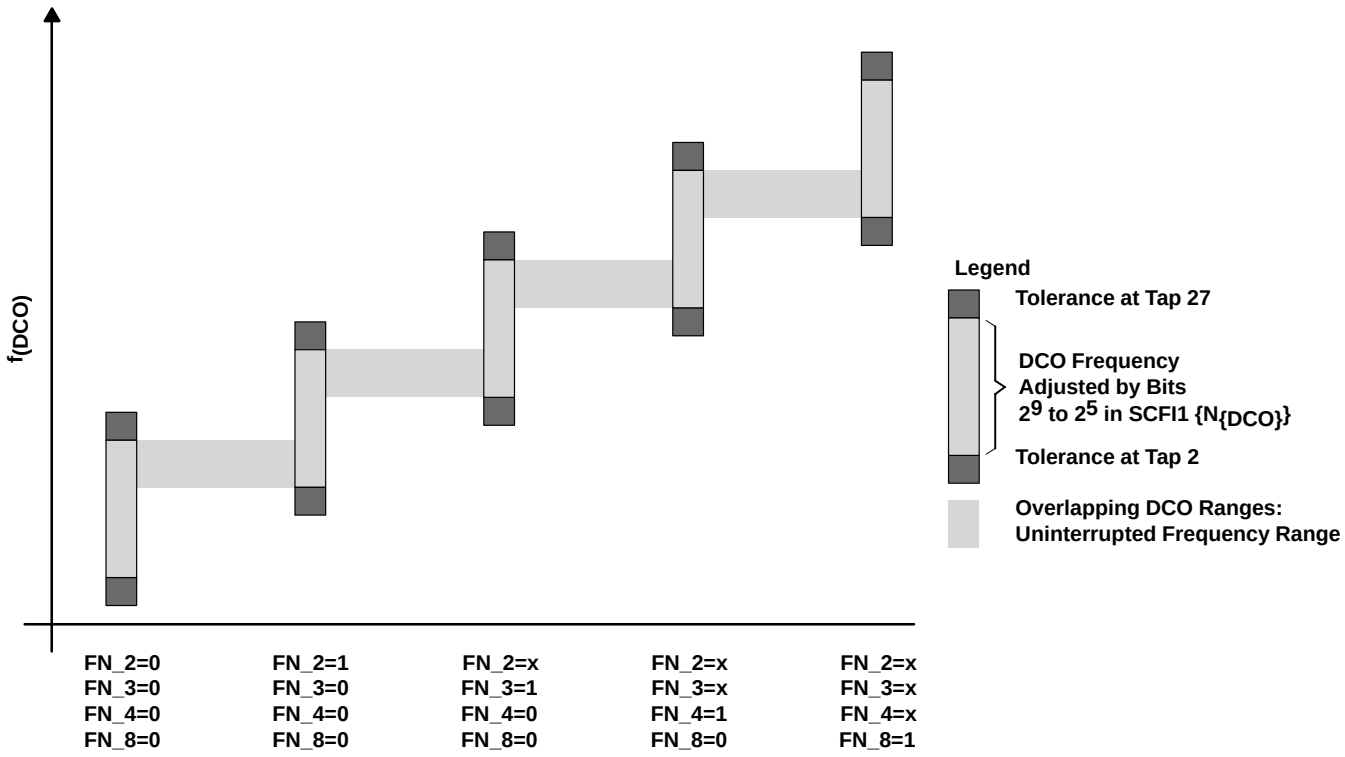


Figure 16. Five Overlapping DCO Ranges Controlled by FN_x Bits

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$C_{(XIN)}$	Integrated input capacitance	OSCCAP = 0	2.2 V / 3		0		pF
		OSCCAP = 1	2.2 V / 3		10		
		OSCCAP = 2	2.2 V / 3		14		
		OSCCAP = 3	2.2 V / 3		18		
$C_{(XOUT)}$	Integrated output capacitance	OSCCAP = 0	2.2 V / 3		0		pF
		OSCCAP = 1	2.2 V / 3		10		
		OSCCAP = 2	2.2 V / 3		14		
		OSCCAP = 3	2.2 V / 3		18		

NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2pF. The effective load capacitor for the crystal is $(X_{CIN} \times X_{COUT}) / (X_{CIN} + X_{COUT})$. It is independent of XST_FLL .

2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines must be observe:
   - Keep as short a trace as possible between the ’x41x and the crystal.
   - Design a good ground plane around oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to XIN an XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

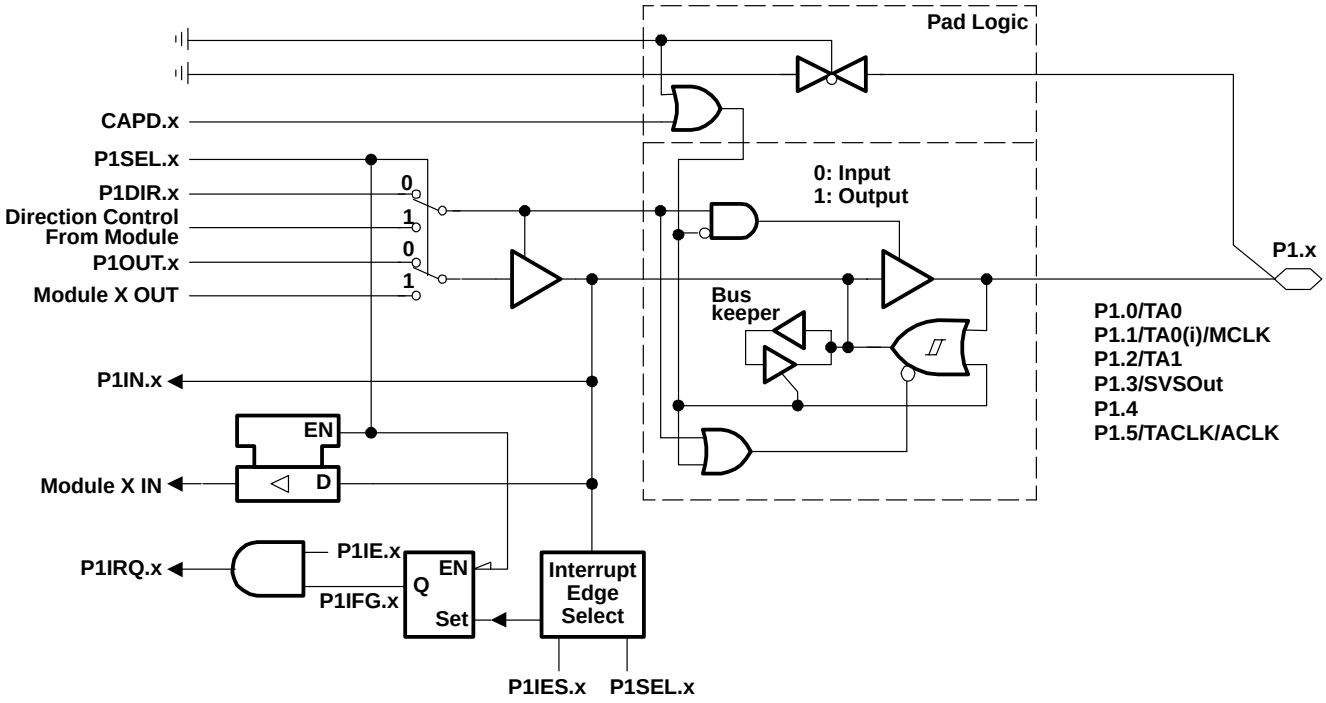
JTAG, program memory and fuse

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(TCK)}$	JTAG/Test	TCK frequency (see Note 5)	2.2 V	DC		5	MHz
			3 V	DC		10	
$R_{(TMS, TCK, TDI)}$		Pullup resistors on TMS, TCK, TDI (see Note 1)	2.2 V/ 3 V	25	60	90	kΩ
$V_{CC(FB)}$	JTAG/Fuse (see Note 2)	Supply voltage during fuse blow condition, T_A = 25°C		2.5			V
V_{FB}		Fuse blow voltage, C versions (see Note 4)		3.5		3.9	V
		Fuse blow voltage, F versions (see Note 3)		6.0		7.0	V
I_{FB}		Supply current on TDI during fuse is blown				100	mA
t_{FB}		Time to blow the fuse				1	ms
$I_{(DD-PGM)}$	F-versions only	Current from programming voltage source (see Note 6)	2.7 V/3.6 V		3	5	mA
$I_{(DD-Erase)}$	F-versions only	Programming time, single pulse (see Note 6)	2.7 V/3.6 V		3	5	mA
$t_{(retention)}$	F-versions only	Write/Erase cycles		10^4	10^5		cycles
		Data retention T_J = 25°C		100			years

NOTES:
1. TMS, TDI, and TCK pullup resistors are implemented in all C- and F-versions.
2. Once the fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.
3. The supply voltage to blow the fuse is applied to TDI pin.
4. The power source to blow the fuse is applied to the TDI pin.
5. $f_{(TCK)}$ may be restricted to meet the timing requirements of the module selected.
6. Duration of the program/erase cycle is determined by $f_{(FTG)}$ applied to the flash timing controller. It can be calculated as follows:
   $t_{(word\ write)} = 35 \times 1/f_{(FTG)}$
   $t_{(block\ write,\ byte\ 0)} = 30 \times 1/f_{(FTG)}$
   $t_{(block\ write,\ byte\ 1 – 63)} = 20 \times 1/f_{(FTG)}$
   $t_{(block\ write,\ sequence\ end)} = 6 \times 1/f_{(FTG)}$
   $t_{(mass\ erase)} = 5297 \times 1/f_{(FTG)}$
   $t_{(segment\ erase)} = 4819 \times 1/f_{(FTG)}$

input/output schematic

Port P1, P1.0 to P1.5, input/output with Schmitt-trigger



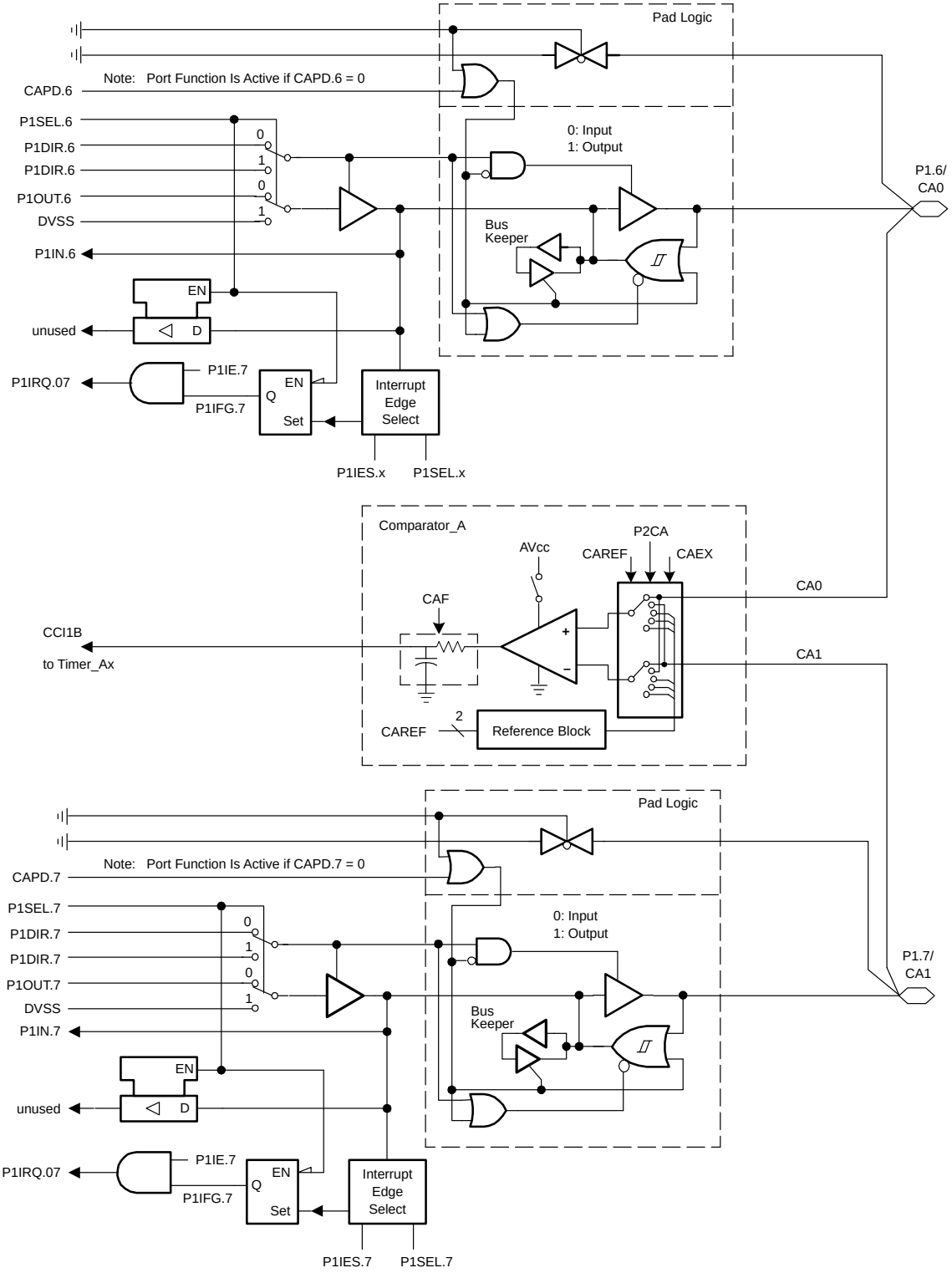
NOTE: $0 \le x \le 5$.
Port Function is Active if CAPD.x = 0

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1SEL.0	P1DIR.0	P1DIR.0	P1OUT.0	Out0 Sig.†	P1IN.0	CCI0A†	P1IE.0	P1IFG.0	P1IES.0
P1SEL.1	P1DIR.1	P1DIR.1	P1OUT.1	MCLK	P1IN.1	CCI0B†	P1IE.1	P1IFG.1	P1IES.1
P1SEL.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 Sig.†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1SEL.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOut	P1IN.3	Unused	P1IE.3	P1IFG.3	P1IES.3
P1SEL.4	P1DIR.4	P1DIR.4	P1OUT.4	DV_{SS}	P1IN.4	Unused	P1IE.4	P1IFG.4	P1IES.4
P1SEL.5	P1DIR.5	P1DIR.5	P1OUT.5	ACLK	P1IN.5	TACLK†	P1IE.5	P1IFG.5	P1IES.5

† Timer_A

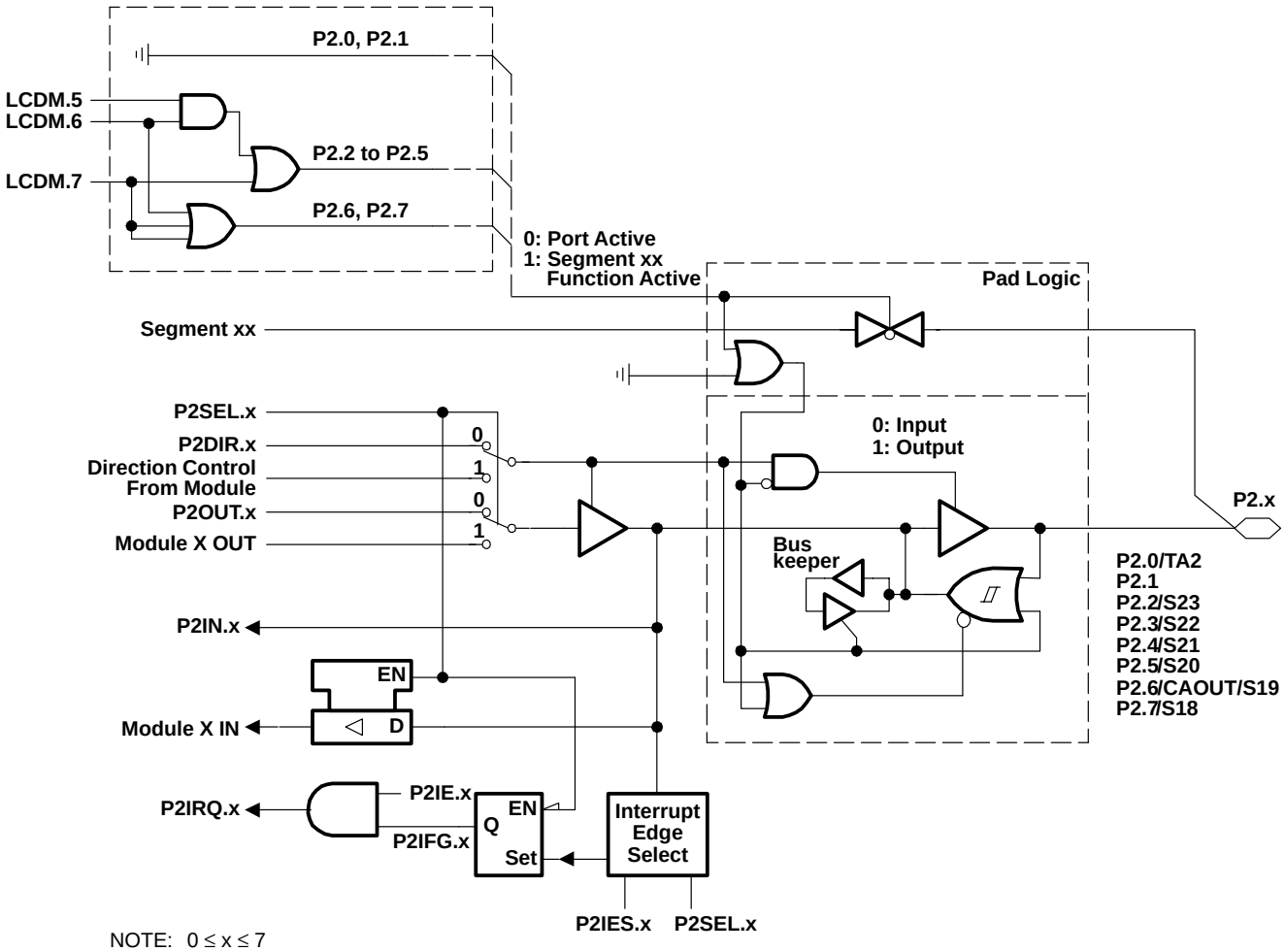
input/output schematic (continued)

Port P1, P1.6, P1.7 input/output with Schmitt-trigger



input/output schematic (continued)

port P2, P2.0 to P2.7, input/output with Schmitt-trigger



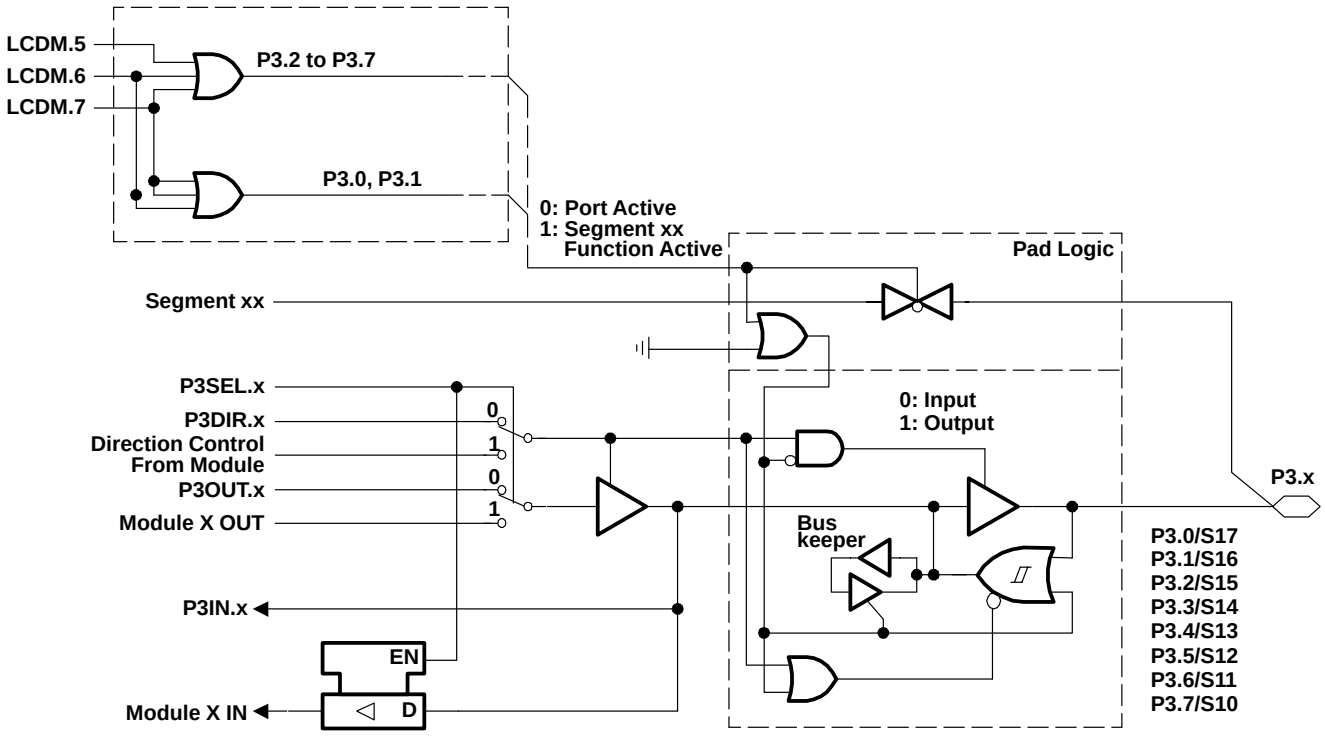
NOTE: $0 \le x \le 7$

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2SEL.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2 Sig.†	P2IN.0	CCI2A†	P2IE.0	P2IFG.0	P2IES.0
P2SEL.1	P2DIR.1	P2DIR.1	P2OUT.1	DVSS	P2IN.1	Unused	P2IE.1	P2IFG.1	P2IES.1
P2SEL.2	P2DIR.2	P2DIR.2	P2OUT.2	DVSS	P2IN.2	Unused	P2IE.2	P2IFG.2	P2IES.2
P2SEL.3	P2DIR.3	P2DIR.3	P2OUT.3	DVSS	P2IN.3	Unused	P2IE.3	P2IFG.3	P2IES.3
P2SEL.4	P2DIR.4	P2DIR.4	P2OUT.4	DVSS	P2IN.4	Unused	P2IE.4	P2IFG.4	P2IES.4
P2SEL.5	P2DIR.5	P2DIR.5	P2OUT.5	DVSS	P2IN.5	Unused	P2IE.5	P2IFG.5	P2IES.5
P2SEL.6	P2DIR.6	P2DIR.6	P2OUT.6	CAOUT	P2IN.6	Unused	P2IE.6	P2IFG.6	P2IES.6
P2SEL.7	P2DIR.7	P2DIR.7	P2OUT.7	DVSS	P2IN.7	Unused	P2IE.7	P2IFG.7	P2IES.7

† Timer_A

input/output schematic (continued)

port P3, P3.0, P3.7, input/output with Schmitt-trigger

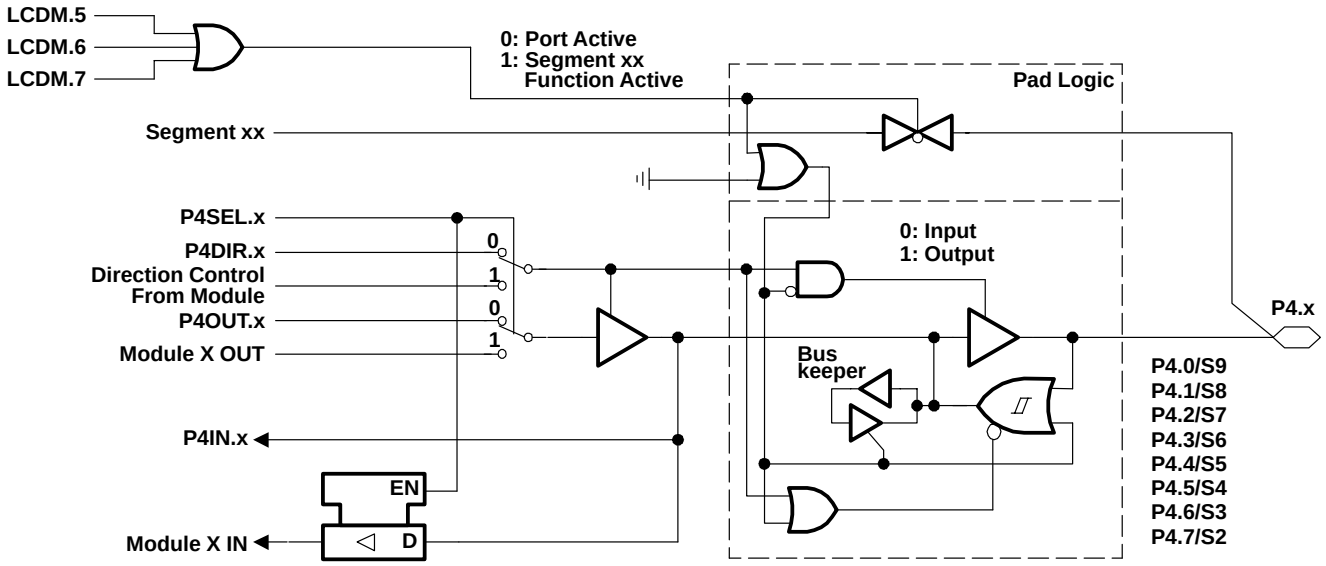


NOTE: $0 \le x \le 7$

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3SEL.0	P3DIR.0	P3DIR.0	P3OUT.0	DVSS	P3IN.0	Unused
P3SEL.1	P3DIR.1	P3DIR.1	P3OUT.1	DVSS	P3IN.1	Unused
P3SEL.2	P3DIR.2	P3DIR.2	P3OUT.2	DVSS	P3IN.2	Unused
P3SEL.3	P3DIR.3	P3DIR.3	P3OUT.3	DVSS	P3IN.3	Unused
P3SEL.4	P3DIR.4	P3DIR.4	P3OUT.4	DVSS	P3IN.4	Unused
P3SEL.5	P3DIR.5	P3DIR.5	P3OUT.5	DVSS	P3IN.5	Unused
P3SEL.6	P3DIR.6	P3DIR.6	P3OUT.6	DVSS	P3IN.6	Unused
P3SEL.7	P3DIR.7	P3DIR.7	P3OUT.7	DVSS	P3IN.7	Unused

input/output schematic (continued)

port P4, P4.0 to P4.7, input/output with Schmitt-trigger

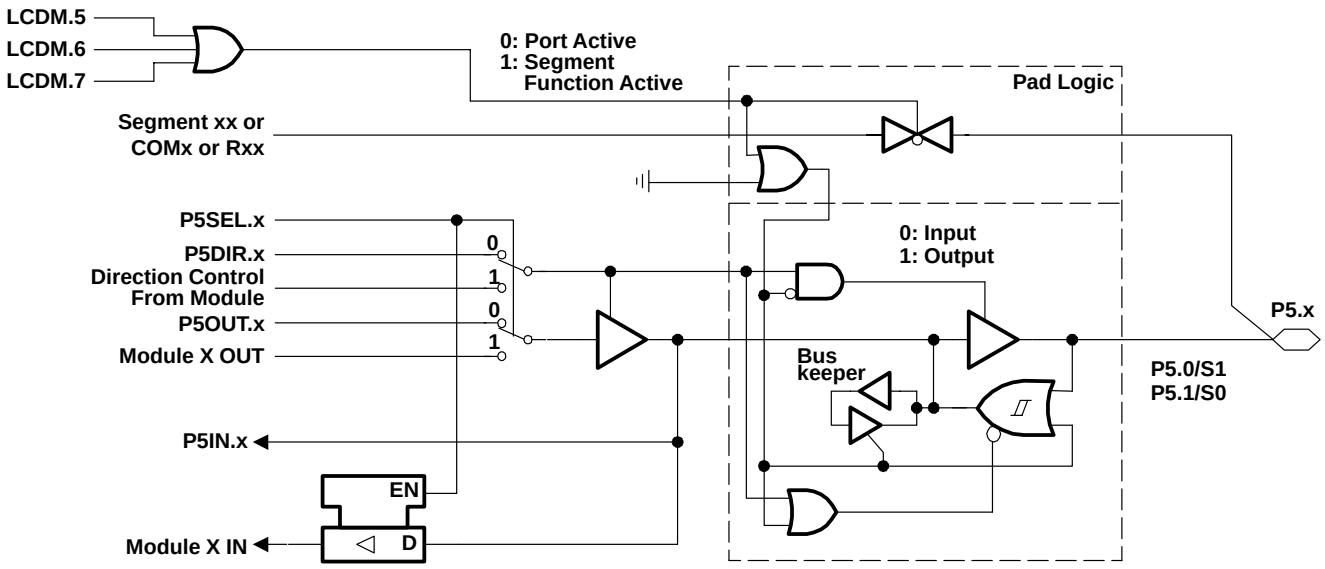


NOTE: $0 \le x \le 7$

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4SEL.0	P4DIR.0	P4DIR.0	P4OUT.0	DVSS	P4IN.0	Unused
P4SEL.1	P4DIR.1	P4DIR.1	P4OUT.1	DVSS	P4IN.1	Unused
P4SEL.2	P4DIR.2	P4DIR.2	P4OUT.2	DVSS	P4IN.2	Unused
P4SEL.3	P4DIR.3	P4DIR.3	P4OUT.3	DVSS	P4IN.3	Unused
P4SEL.4	P4DIR.4	P4DIR.4	P4OUT.4	DVSS	P4IN.4	Unused
P4SEL.5	P4DIR.5	P4DIR.5	P4OUT.5	DVSS	P4IN.5	Unused
P4SEL.6	P4DIR.6	P4DIR.6	P4OUT.6	DVSS	P4IN.6	Unused
P4SEL.7	P4DIR.7	P4DIR.7	P4OUT.7	DVSS	P4IN.7	Unused

input/output schematic (continued)

port P5, P5.0, P5.1, input/output with Schmitt-trigger

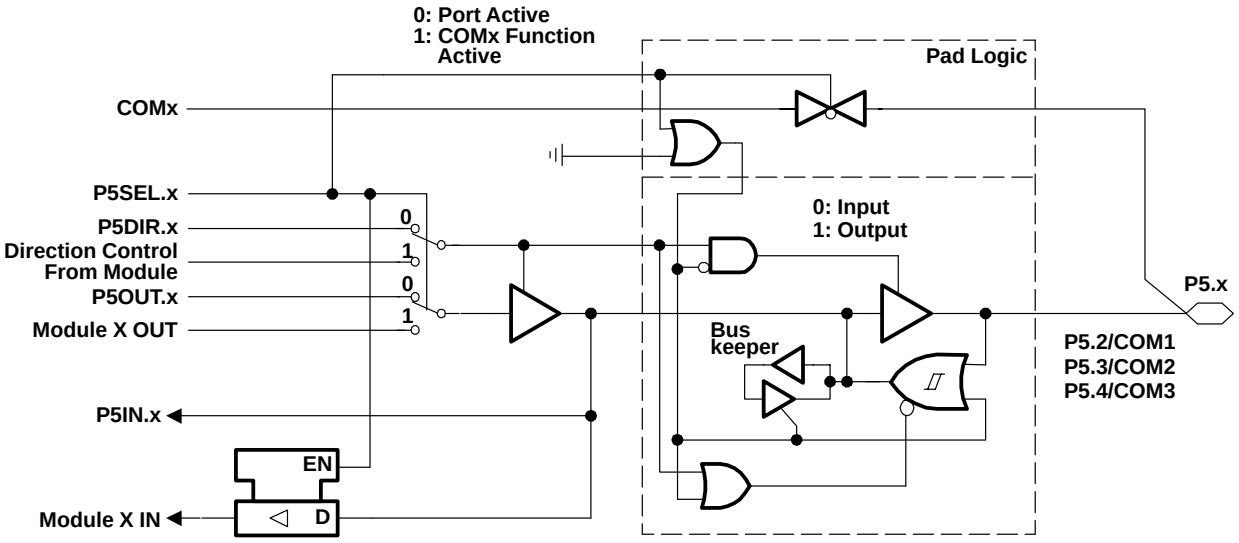


NOTE: x = 0, 1

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Segment
P5SEL.0	P5DIR.0	P5DIR.0	P5OUT.0	DVSS	P5IN.0	Unused	S1
P5SEL.1	P5DIR.1	P5DIR.1	P5OUT.1	DVSS	P5IN.1	Unused	S0

input/output schematic (continued)

port P5, P5.2, P5.4, input/output with Schmitt-trigger



NOTE: $2 \le x \le 4$

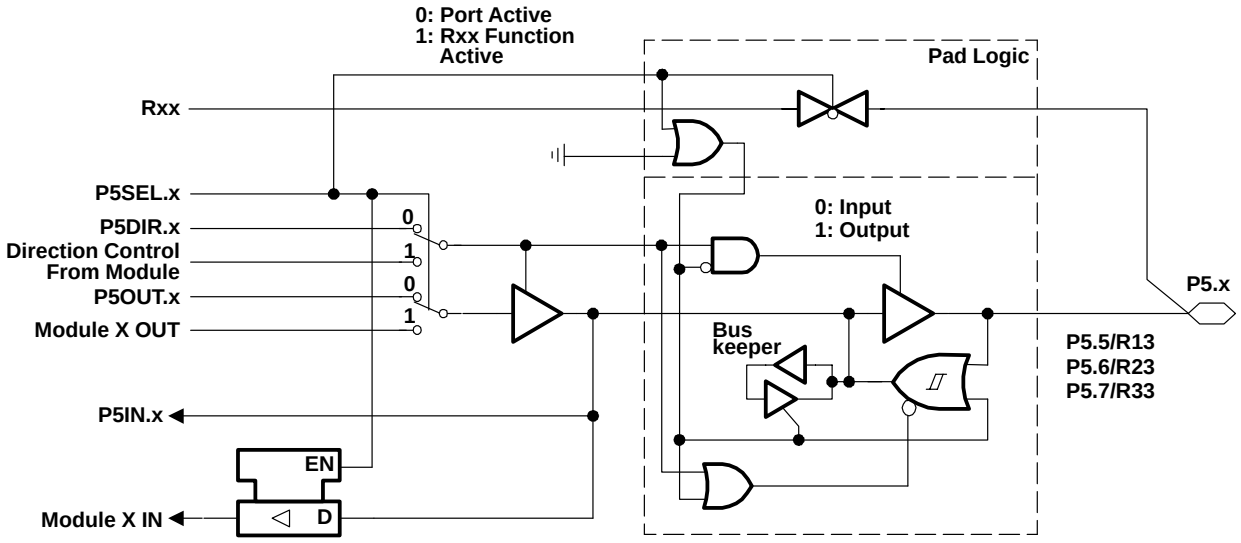
PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	COMx
P5SEL.2	P5DIR.2	P5DIR.2	P5OUT.2	DVSS	P5IN.2	Unused	COM1
P5SEL.3	P5DIR.3	P5DIR.3	P5OUT.3	DVSS	P5IN.3	Unused	COM2
P5SEL.4	P5DIR.4	P5DIR.4	P5OUT.4	DVSS	P5IN.4	Unused	COM3

NOTE:

The direction control bits P5SEL.2, P5SEL.3, and P5SEL.4 are used to distinguish between port and common functions. Note that a 4MUX LCD requires all common signals COM3 to COM0, a 3MUX LCD requires COM2 to COM0, 2MUX LCD requires COM1 to COM0, and a static LCD requires only COM0.

input/output schematic (continued)

port P5, P5.5 to P5.7, input/output with Schmitt-trigger



NOTE: $5 \le x \le 7$

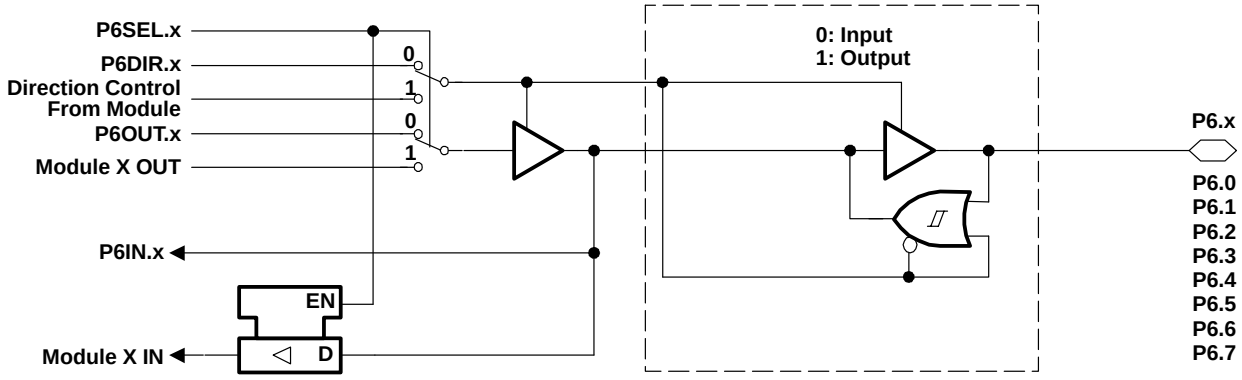
PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Rxx
P5SEL.5	P5DIR.5	P5DIR.5	P5OUT.5	DVSS	P5IN.5	Unused	R13
P5SEL.6	P5DIR.6	P5DIR.6	P5OUT.6	DVSS	P5IN.6	Unused	R23
P5SEL.7	P5DIR.7	P5DIR.7	P5OUT.7	DVSS	P5IN.7	Unused	R33

NOTE:

The direction control bits P5SEL.5, P5SEL.6, and P5SEL.7 are used to distinguish between port and LCD analog level functions. Note that 4MUX and 3MUX LCDs require all Rxx signals R33 to R03, a 2MUX LCD requires R33, R13, and R03, and a static LCD requires only R33 and R03.

input/output schematic (continued)

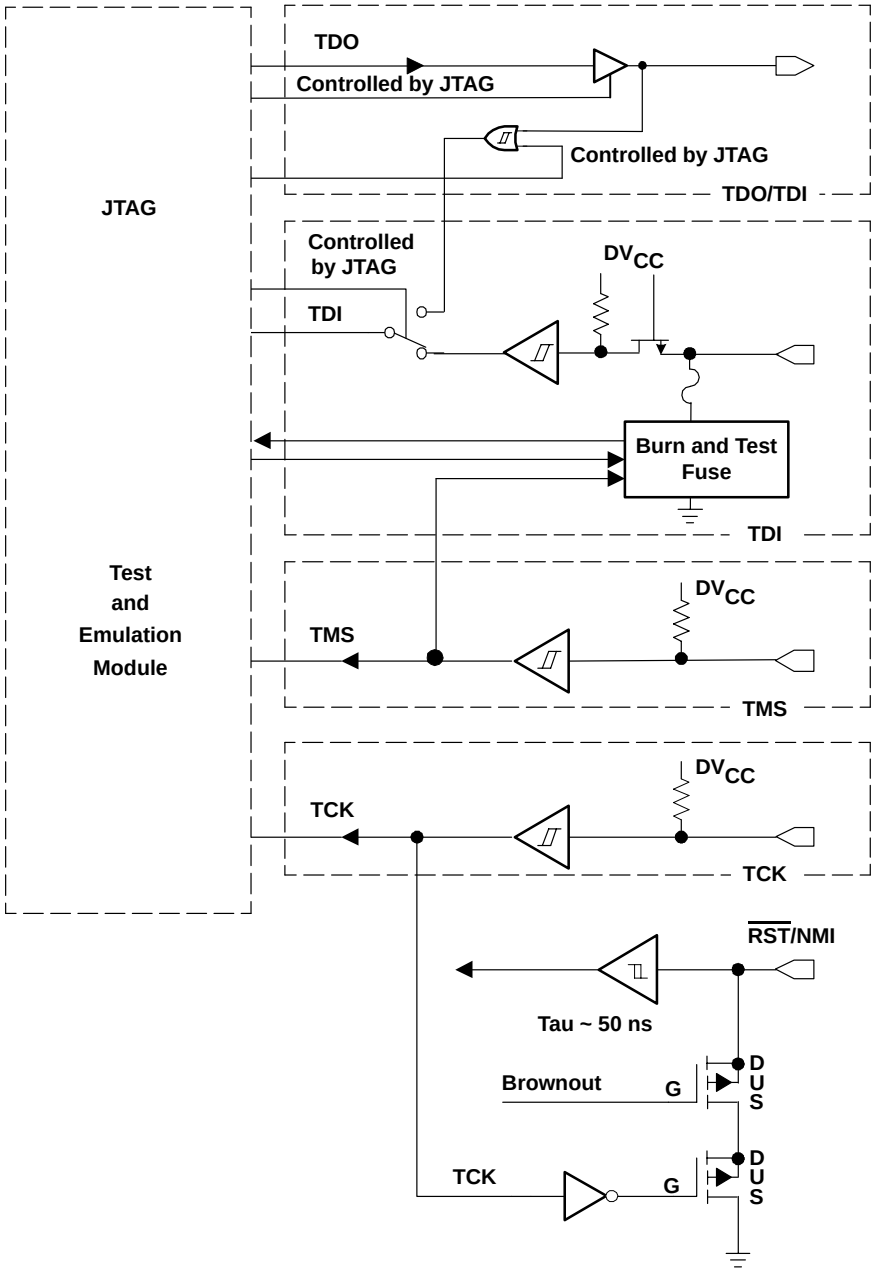
port P6, P6.0 to P6.7, input/output with Schmitt-trigger



NOTE: $0 \le x \le 7$

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6SEL.0	P6DIR.0	P6DIR.0	P6OUT.0	DVSS	P6IN.0	Unused
P6SEL.1	P6DIR.1	P6DIR.1	P6OUT.1	DVSS	P6IN.1	Unused
P6SEL.2	P6DIR.2	P6DIR.2	P6OUT.2	DVSS	P6IN.2	Unused
P6SEL.3	P6DIR.3	P6DIR.3	P6OUT.3	DVSS	P6IN.3	Unused
P6SEL.4	P6DIR.4	P6DIR.4	P6OUT.4	DVSS	P6IN.4	Unused
P6SEL.5	P6DIR.5	P6DIR.5	P6OUT.5	DVSS	P6IN.5	Unused
P6SEL.6	P6DIR.6	P6DIR.6	P6OUT.6	DVSS	P6IN.6	Unused
P6SEL.7	P6DIR.7	P6DIR.7	P6OUT.7	DVSS	P6IN.7	Unused

JTAG pins TMS, TCK, TDI, TDO/TDI, input/output with Schmitt-trigger or output



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1.8 mA at 3 V can flow from the TDI pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 17). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

The JTAG pins are terminated internally, and therefore do not require external termination.

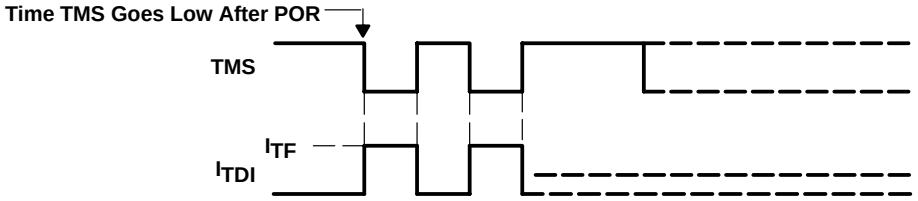
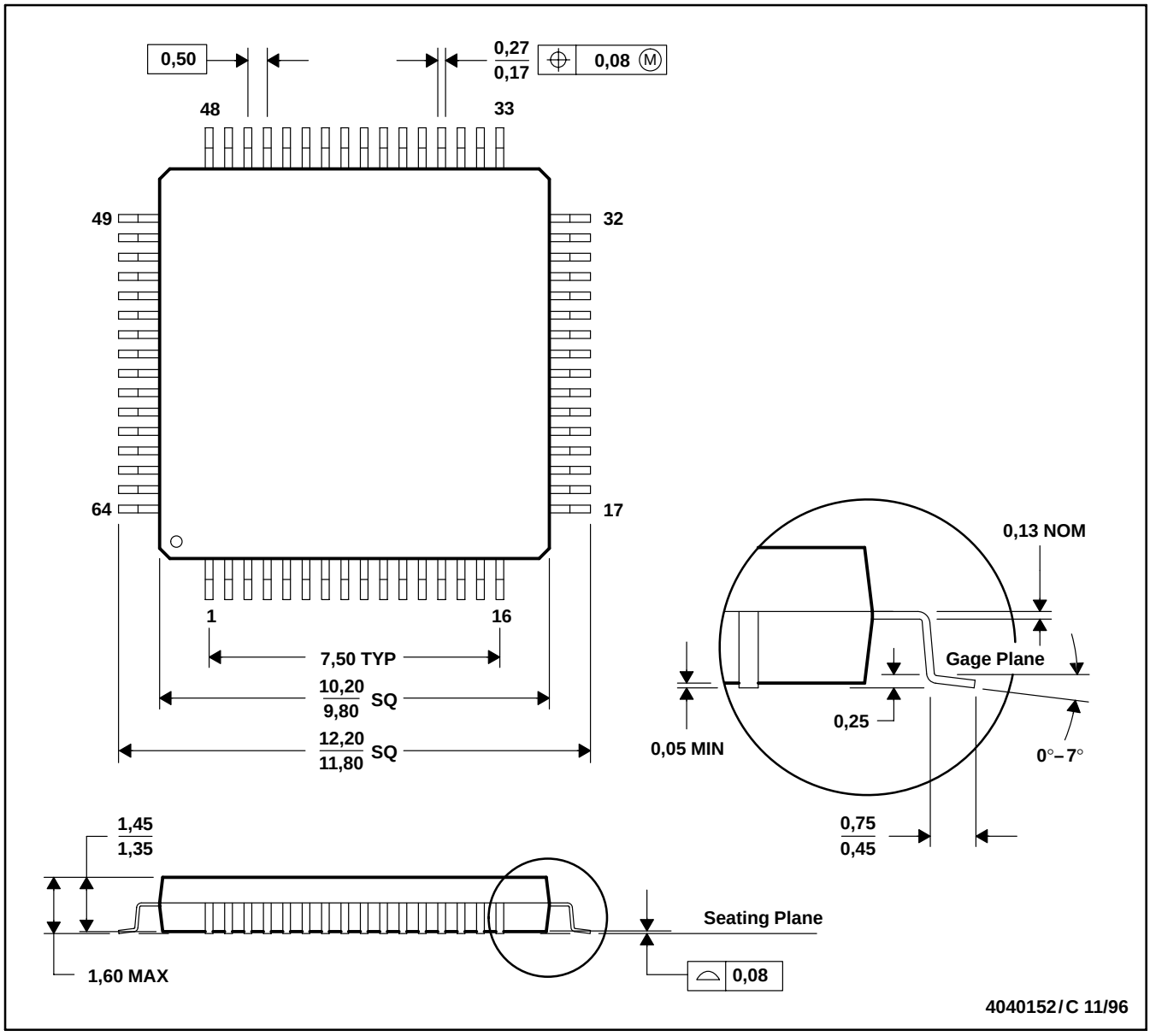


Figure 17. Fuse Check Mode Current, MSP430C41x, MSP430F41x

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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