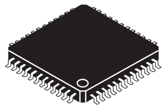
Burr-Brown Products from Texas Instruments



ADS8381

SLAS364B − APRIL 2002 − REVISED JUNE 2003

18-BIT, 580-kHz, UNIPOLAR INPUT, MICRO POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

FEATURES

- **580-kHz Sample Rate**
- **18-Bit NMC Ensured Over Temperature**
- **Zero Latency**
- **Low Power: 110 mW at 580 kHz**
- **Unipolar Input Range**
- **Onboard Reference Buffer**
- **High-Speed Parallel Interface**
- **Wide Digital Supply, 2.7 V to 5.25 V**
- **8-/16-/18-Bit Bus Transfer**
- **48-Pin TQFP Package**

APPLICATIONS

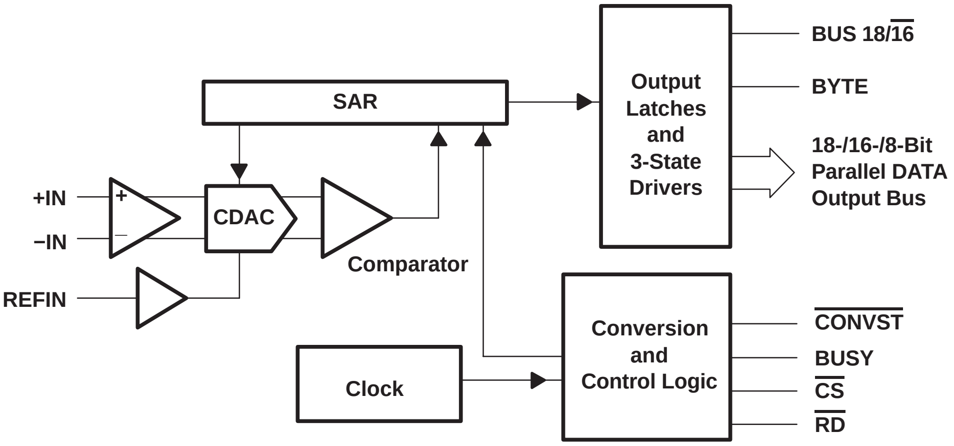
- **Medical Instruments**
- **Optical Networking**
- **Transducer Interface**
- **High Accuracy Data Acquisition Systems**
- **Magnetometers**

DESCRIPTION

The ADS8381 is an 18-bit, 580 kHz A/D converter. The device includes a 18-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8381 offers a full 18-bit interface, a 16-bit option where data is read using two read cycles, or an 8-bit bus option using three read cycles.

The ADS8381 is available in a 48-lead TQFP package and is characterized over the industrial −40°C to 85°C temperature range.

PRODUCT PREVIEW



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8381I	±10	−2~7	17	48 Pin TQFP	PFB	−40°C to 85°C	ADS8381IPFBT	Tape and reel 250
							ADS8381IPFBR	Tape and reel 1000
ADS8381IB	±7	−1~2.5	18	48 Pin TQFP	PFB	−40°C to 85°C	ADS8381IBPFBT	Tape and reel 250
							ADS8381IBPFBR	Tape and reel 1000

NOTE: For the most current specifications and package information, refer to our website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Voltage	+IN to AGND	−0.4 V to +VA + 0.1 V
	−IN to AGND	−0.4 V to 0.5 V
Voltage range	+VA to AGND	−0.3 V to 7 V
	+VBD to BDGND	−0.3 V to 7 V
	+VA to +VBD	−0.3 V to 2.55 V
Digital input voltage to BDGND		−0.3 V to +VBD + 0.3 V
Digital output voltage to BDGND		−0.3 V to +VBD + 0.3 V
Operating free-air temperature range, T_A		−40°C to 85°C
Storage temperature range, T_{stg}		−65°C to 150°C
Junction temperature (T_J max)		150°C
TQFP package	Power dissipation	$(T_J\text{Max} - T_A)/\theta_{JA}$
	θ_{JA} thermal impedance	86°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = −40°C to 85°C, +VA = 5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 580 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
Full-scale input voltage (see Note 1)		+IN − −IN	0		V_{ref}	V
Absolute input voltage		+IN	−0.2		V_{ref} + 0.2	V
		−IN	−0.2		0.2	
Input capacitance				45		pF
Input leakage current				1		nA
System Performance						
Resolution				18		Bits
No missing codes	ADS8381I	(+IN − −IN) < 0.5 FS	18			Bits
		(+IN − −IN) ≥ 0.5 FS	17			
	ADS8381IB		18			
Integral linearity (see Notes 2 and 3)	ADS8381I	(+IN − −IN) < 0.125 FS	−4		4	LSB (18 bit)
		(+IN − −IN) < 0.5 FS	−6		6	
		(+IN − −IN) ≥ 0.5 FS	−10		10	
	ADS8381IB		−7	−2/3	7	
Differential linearity	ADS8381I	(+IN − −IN) < 0.125 FS	−1		2	LSB (18 bit)
		(+IN − −IN) < 0.5 FS	−1		3	
		(+IN − −IN) ≥ 0.5 FS	−2		7	
	ADS8381IB		−1	−1/1.4	2.5	
Offset error (see Note 4)	ADS8381I		−1	±0.5	1	mV
	ADS8381IB		−0.75	±0.25	0.75	
Gain error (see Note 4)	ADS8381I	V_{ref} = 4.096 V	−0.1		0.1	%FS
	ADS8381IB	V_{ref} = 4.096 V	−0.06		0.06	%FS
Noise				60		µV RMS
Power supply rejection ratio		At 3FFFFh output code		75		dB
Sampling Dynamics						
Conversion time					1.3	µs
Acquisition time			0.35			µs
Throughput rate					570	kHz
Aperture delay				4		ns
Aperture jitter				15		ps
Step response				150		ns
Over voltage recovery				150		ns

(1) Ideal input span, does not include gain or offset error.
(2) LSB means least significant bit
(3) This is endpoint INL, not best fit.
(4) Measured relative to an ideal full-scale input (+IN − −IN) of 4.096 V

PRODUCT PREVIEW

SPECIFICATIONS (CONTINUED)

T_A = −40°C to 85°C, +VA = +5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 580 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics						
Total harmonic distortion (THD) (see Note 1)	ADS8381I	V_{IN} = 4 V_{pp} at 1 kHz		−110		dB
	ADS8381IB			−112		
	ADS8381I	V_{IN} = 4 V_{pp} at 10 kHz		−98		
	ADS8381IB			−108		
	ADS8381I	V_{IN} = 4 V_{pp} at 50 kHz		−98		
	ADS8381IB			−99		
	ADS8381I	V_{IN} = 4 V_{pp} at 100 kHz		−90		
	ADS8381IB			−91		
Signal to noise ratio (SNR) (see Note 1)	ADS8381I	V_{IN} = 4 V_{pp} at 1 kHz		87		dB
	ADS8381IB			88		
	ADS8381I	V_{IN} = 4 V_{pp} at 10 kHz		87		
	ADS8381IB			87		
	ADS8381I	V_{IN} = 4 V_{pp} at 50 kHz		87		
	ADS8381IB			87		
	ADS8381I	V_{IN} = 4 V_{pp} at 100 kHz		87		
	ADS8381IB			87		
Signal to noise + distortion (SINAD) (see Note 1)	ADS8381I	V_{IN} = 4 V_{pp} at 1 kHz		86		dB
	ADS8381IB			87		
	ADS8381I	V_{IN} = 4 V_{pp} at 10 kHz		86		
	ADS8381IB			86		
	ADS8381I	V_{IN} = 4 V_{pp} at 50 kHz		86		
	ADS8381IB			86		
	ADS8381I	V_{IN} = 4 V_{pp} at 100 kHz		85		
	ADS8381IB			85		
Spurious free dynamic range (SFDR) (see Note 1)	ADS8381I	V_{IN} = 4 V_{pp} at 1 kHz		110		dB
	ADS8381IB			112		
	ADS8381I	V_{IN} = 4 V_{pp} at 10 kHz		98		
	ADS8381IB			107		
	ADS8381I	V_{IN} = 4 V_{pp} at 50 kHz		98		
	ADS8381IB			98		
	ADS8381I	V_{IN} = 4 V_{pp} at 100 kHz		90		
	ADS8381IB			94		
−3dB Small signal bandwidth				3		MHz
Voltage Reference Input						
Reference voltage at REFIN, V_{ref}			2.5	4.096	4.2	V
Reference resistance (see Note 2)				500		kΩ
Reference current drain		f_S = 580 kHz			1	mA

(1) Calculated on the first nine harmonics of the input frequency
(2) Can vary ±20%

SPECIFICATIONS (CONTINUED)

T_A = −40°C to 85°C, +VA = +5 V, +VBD = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 580 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input/Output						
Logic family				CMOS		
Logic level	V_{IH}	I_{IH} = 5 µA	+VBD−1		$+V_{BD}$ + 0.3	V
	V_{IL}	I_{IL} = 5 µA	−0.3		0.8	
	V_{OH}	I_{OH} = 2 TTL loads	$+V_{BD}$ − 0.6			
	V_{OL}	I_{OL} = 2 TTL loads			0.4	
Data format				Straight Binary		
Power Supply Requirements						
Power supply voltage	+VBD		2.7	3.3	5.25	V
	+VA		4.75	5	5.25	V
Supply current, 500-kHz sample rate (see Note 1)				22	26	mA
Power dissipation, 500-kHz sample rate (see Note 1)				110	130	mW
Temperature Range						
Operating free-air			−40		85	°C

(1) This includes only +VA current. +VBD current is typical 1 mA with 5 pF load capacitance on all output pins.

TIMING CHARACTERISTICS

All specifications typical at −40°C to 85°C, +VA = +VBD = 5 V (see Notes 1, 2, and 3)

PARAMETER		MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time			1.3	µs
t_{ACQ}	Acquisition time	0.35			µs
t_{HOLD}	Sampling capacitor hold time			25	ns
t_{pd1}	$\overline{\text{CONVST}}$ low to conversion started (BUSY high)			45	ns
t_{pd2}	Propagation delay time, End of conversion to BUSY low			20	ns
t_{pd3}	Propagation delay time, from start of conversion (internal state) to rising edge of BUSY			20	ns
t_{w1}	Pulse duration, $\overline{\text{CONVST}}$ low	40			ns
t_{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t_{w2}	Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
	$\overline{\text{CONVST}}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	Min(t_{ACQ})			µs
t_{w4}	Pulse duration, BUSY signal high			1.3	µs
t_{h1}	Hold time, First data bus data transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE or BUS18/$\overline{16}$ input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t_{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5}	Pulse duration, $\overline{\text{RD}}$ low time	50			ns
t_{en}	Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid			20	ns
t_{d2}	Delay time, data hold from $\overline{\text{RD}}$ high	5			ns
t_{d3}	Delay time, BUS18/$\overline{16}$ or BYTE rising edge or falling edge to data valid	10		20	ns
t_{w6}	Pulse duration, $\overline{\text{RD}}$ high	20			ns
t_{w7}	Pulse duration, $\overline{\text{CS}}$ high time	20			ns
t_{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	125			ns
t_{pd4}	Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge	Max(t_{d5})			ns
t_{d4}	Delay time, BYTE edge to BUS18/$\overline{16}$ edge skew	0			ns
t_{su3}	Setup time, BYTE or BUS18/$\overline{16}$ transition to $\overline{\text{RD}}$ falling edge	10			ns
t_{h3}	Hold time, BYTE or BUS18/$\overline{16}$ transition to $\overline{\text{RD}}$ falling edge	10			ns
t_{dis}	Disable time, $\overline{\text{RD}}$ High ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus			20	ns
t_{d5}	Delay time, BUSY low to MSB data valid			30	ns
t_{su5}	Setup time, BYTE transition to next BYTE transition, or BUS18/$\overline{16}$ transition to next BUS18/$\overline{16}$ transition	50			ns
$t_{su(AB)}$	Setup time, from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when $\overline{\text{CS}}$ = 0 and $\overline{\text{CONVST}}$ used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort).	65		1000	ns

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

TIMING CHARACTERISTICS

All specifications typical at −40°C to 85°C, +VA = 5 V, +VBD = 3 V (see Notes 1, 2, and 3)

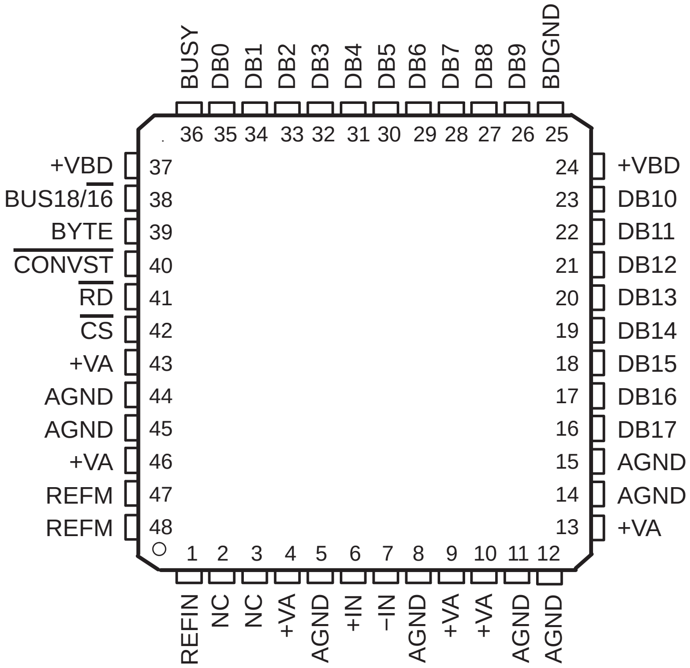
PARAMETER		MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time			1.3	µs
t_{ACQ}	Acquisition time	0.35			µs
t_{HOLD}	Sampling capacitor hold time			25	ns
t_{pd1}	$\overline{\text{CONVST}}$ low to conversion started (BUSY high)			50	ns
t_{pd2}	Propagation delay time, end of conversion to BUSY low			25	ns
t_{pd3}	Propagation delay time, from start of conversion (internal state) to rising edge of BUSY			25	ns
t_{w1}	Pulse duration, $\overline{\text{CONVST}}$ low	40			ns
t_{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t_{w2}	Pulse duration, $\overline{\text{CONVST}}$ high	20			ns
	$\overline{\text{CONVST}}$ falling edge jitter			10	ps
t_{w3}	Pulse duration, BUSY signal low	Min(t_{ACQ})			µs
t_{w4}	Pulse duration, BUSY signal high			1.3	µs
t_{h1}	Hold time, first data bus transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE or BUS 18/$\overline{\text{16}}$ input changes) after $\overline{\text{CONVST}}$ low	40			ns
t_{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t_{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t_{w5}	Pulse duration, $\overline{\text{RD}}$ low	50			ns
t_{en}	Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid			30	ns
t_{d2}	Delay time, data hold from $\overline{\text{RD}}$ high	10			ns
t_{d3}	Delay time, BUS18/$\overline{\text{16}}$ or BYTE rising edge or falling edge to data valid	10		30	ns
t_{w6}	Pulse duration, $\overline{\text{RD}}$ high time	20			ns
t_{w7}	Pulse duration, $\overline{\text{CS}}$ high time	20			ns
t_{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	125			ns
t_{pd4}	Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge	Max(td5)			ns
t_{d4}	Delay time, BYTE edge to BUS18/$\overline{\text{16}}$ edge skew	0			ns
t_{su3}	Setup time, BYTE or BUS18/$\overline{\text{16}}$ transition to $\overline{\text{RD}}$ falling edge	10			ns
t_{h3}	Hold time, BYTE or BUS18/$\overline{\text{16}}$ transition to $\overline{\text{RD}}$ falling edge	10			ns
t_{dis}	Disable time, $\overline{\text{RD}}$ High ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus			30	ns
t_{d5}	Delay time, BUSY low to MSB data valid delay time			40	ns
t_{su5}	Setup time, BYTE transition to next BYTE transition, or BUS18/$\overline{\text{16}}$ transition to next BUS18/$\overline{\text{16}}$ transition	50			ns
$t_{su(AB)}$	Setup time, from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when $\overline{\text{CS}}$ = 0 and $\overline{\text{CONVST}}$ used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort).	70		1000	ns

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.
(3) All timing are measured with 10 pF equivalent loads on all data bits and BUSY pins.

PRODUCT PREVIEW

PIN ASSIGNMENTS

PFB PACKAGE
(TOP VIEW)



NC − No connection.

TERMINAL FUNCTIONS

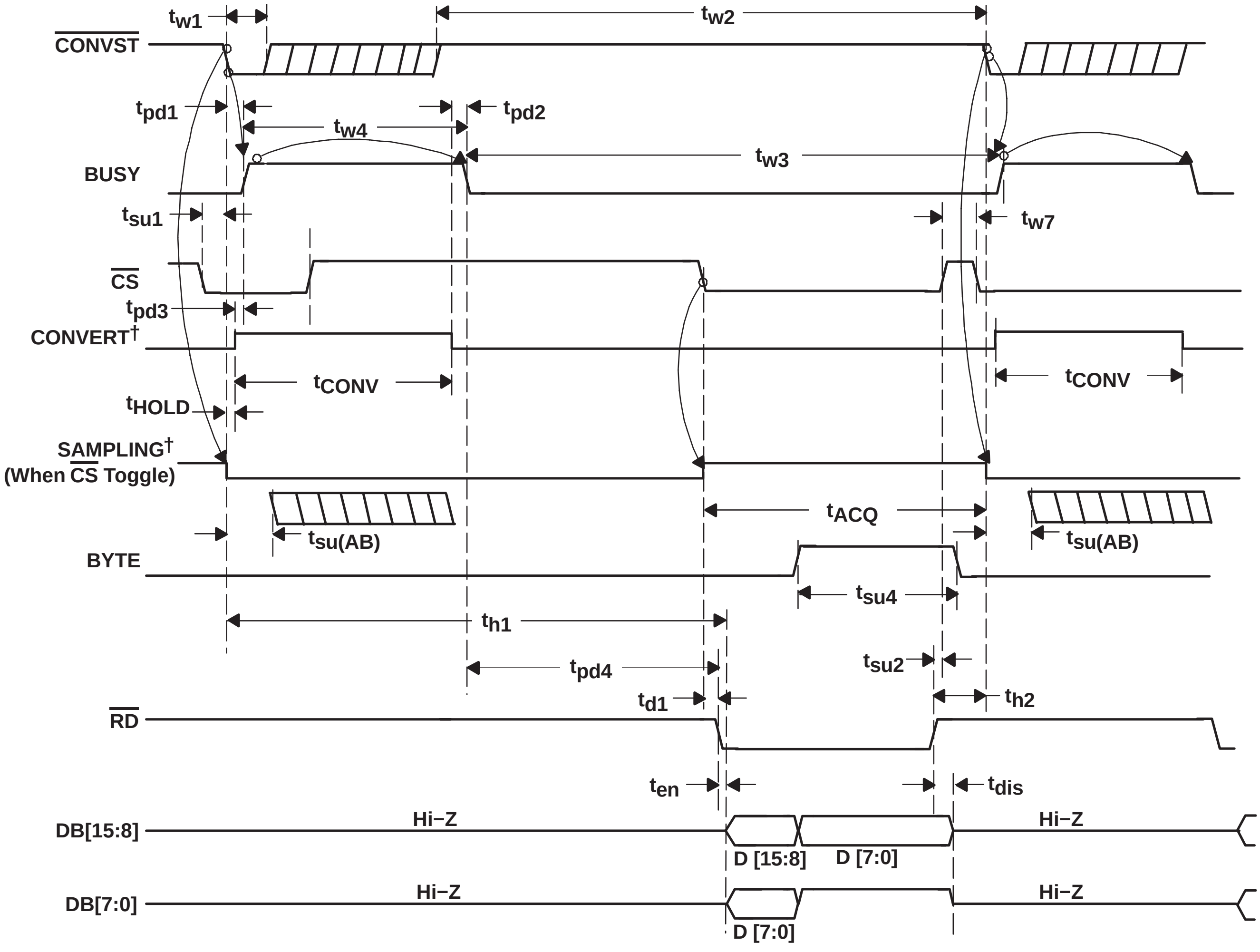
NAME	NO.	I/O	DESCRIPTION
AGND	5, 8, 11, 12, 14, 15, 44, 45	−	Analog ground
BDGND	25	−	Digital ground for bus interface digital supply
BUSY	36	O	Status output. High when a conversion is in progress.
BUS18/$\overline{16}$	38	I	Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer. 0: Data bits output on the 18-bit data bus pins DB[17:0]. 1: Last two data bits D[1:0] from 18-bit wide bus output on: a) the low byte pins DB[9:2] if BYTE = 0 b) the high byte pins DB[17:10] if BYTE = 1
BYTE	39	I	Byte select input. Used for 8-bit bus reading. 0: No fold back 1: Low byte D[9:2] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[17:10].
$\overline{\text{CONVST}}$	40	I	Convert start. The falling edge of this input ends the acquisition period and starts the hold period.
$\overline{\text{CS}}$	42	I	Chip select. The falling edge of this input starts the acquisition period.

Data Bus			8-Bit Bus			16-Bit Bus		18-Bit Bus
			BYTE = 0	BYTE = 1	BYTE = 1	BYTE = 0	BYTE = 0	BYTE = 0
			BUS18/$\overline{16}$ = 0	BUS18/$\overline{16}$ = 0	BUS18/$\overline{16}$ = 1	BUS18/$\overline{16}$ = 0	BUS18/$\overline{16}$ = 1	BUS18/$\overline{16}$ = 0
DB17	16	O	D17 (MSB)	D9	All ones	D17 (MSB)	All ones	D17 (MSB)
DB16	17	O	D16	D8	All ones	D16	All ones	D16
DB15	18	O	D15	D7	All ones	D15	All ones	D15
DB14	19	O	D14	D6	All ones	D14	All ones	D14
DB13	20	O	D13	D5	All ones	D13	All ones	D13
DB12	21	O	D12	D4	All ones	D12	All ones	D12
DB11	22	O	D11	D3	D1	D11	All ones	D11
DB10	23	O	D10	D2	D0(LSB)	D10	All ones	D10
DB9	26	O	D9	All ones	All ones	D9	All ones	D9
DB8	27	O	D8	All ones	All ones	D8	All ones	D8
DB7	28	O	D7	All ones	All ones	D7	All ones	D7
DB6	29	O	D6	All ones	All ones	D6	All ones	D6
DB5	30	O	D5	All ones	All ones	D5	All ones	D5
DB4	31	O	D4	All ones	All ones	D4	All ones	D4
DB3	32	O	D3	All ones	All ones	D3	D1	D3
DB2	33	O	D2	All ones	All ones	D2	D0 (LSB)	D2
DB1	34	O	D1	All ones	All ones	D1	All ones	D1
DB0	35	O	D0 (LSB)	All ones	All ones	D0 (LSB)	All ones	D0 (LSB)

−IN	7	I	Inverting input channel
+IN	6	I	Noninverting input channel
NC	2, 3	−	No connection
REFIN	1	I	Reference input.
REFM	47, 48	I	Reference ground.
$\overline{\text{RD}}$	41	I	Synchronization pulse for the parallel output. When $\overline{\text{CS}}$ is low, this serves as the output enable and puts the previous conversion result on the bus.
+VA	4, 9, 10, 13, 43, 46	−	Analog power supplies, 5-V dc
+VBD	24, 37	−	Digital power supply for bus

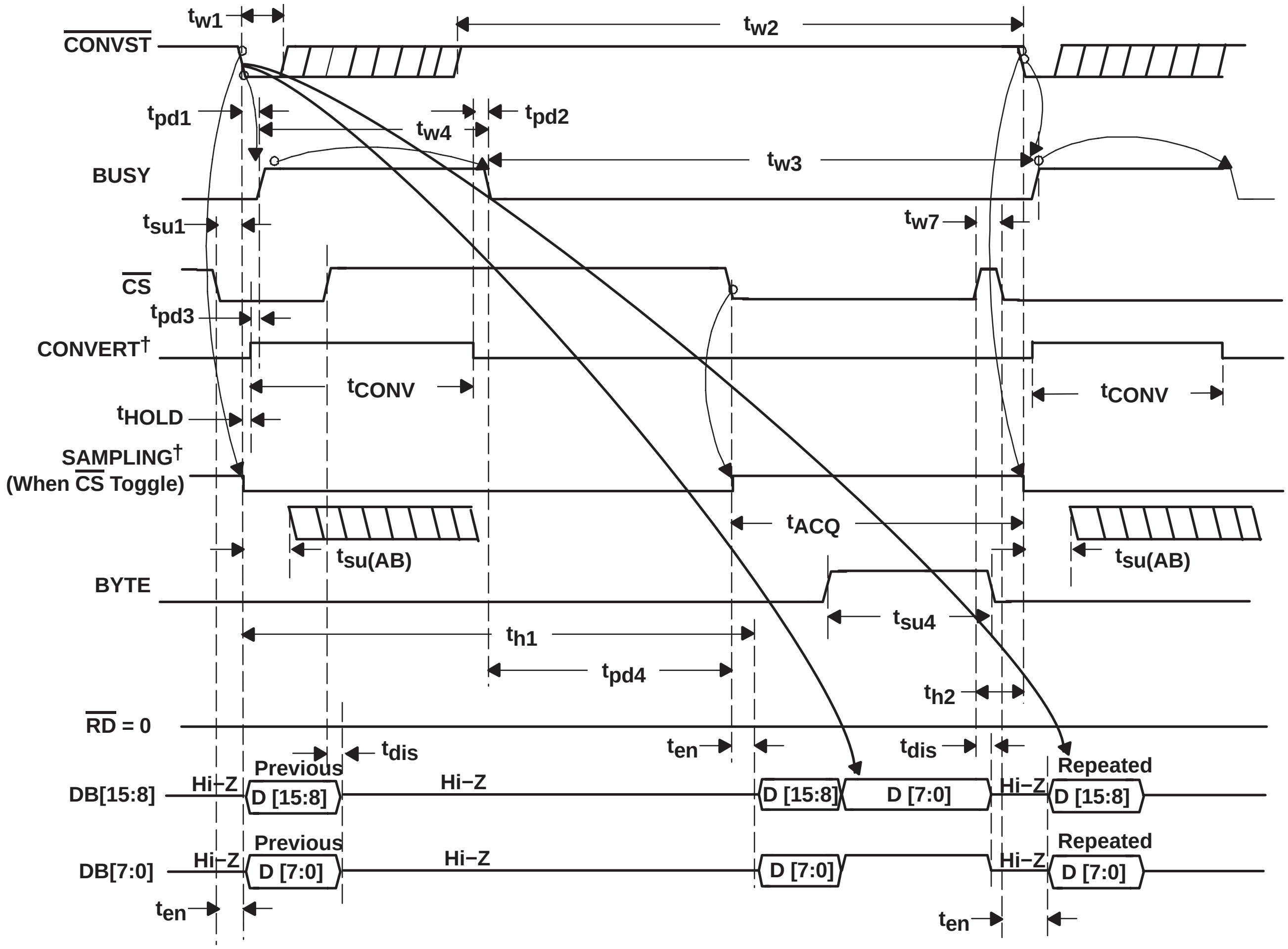
PRODUCT PREVIEW

TIMING DIAGRAMS



†Signal internal to device

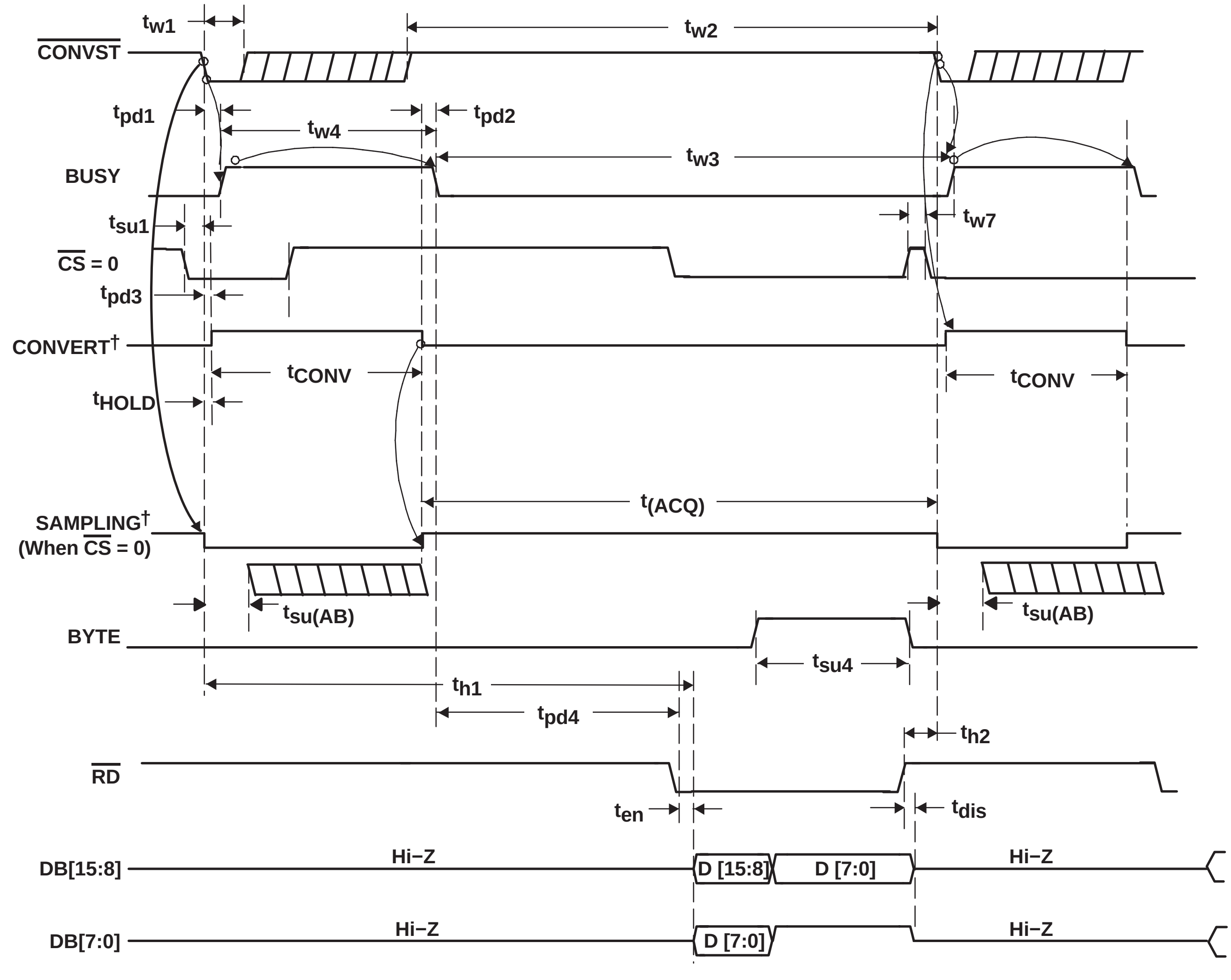
Figure 1. Timing for Conversion and Acquisition Cycles With $\overline{\text{CS}}$ and $\overline{\text{RD}}$ Toggling



†Signal internal to device

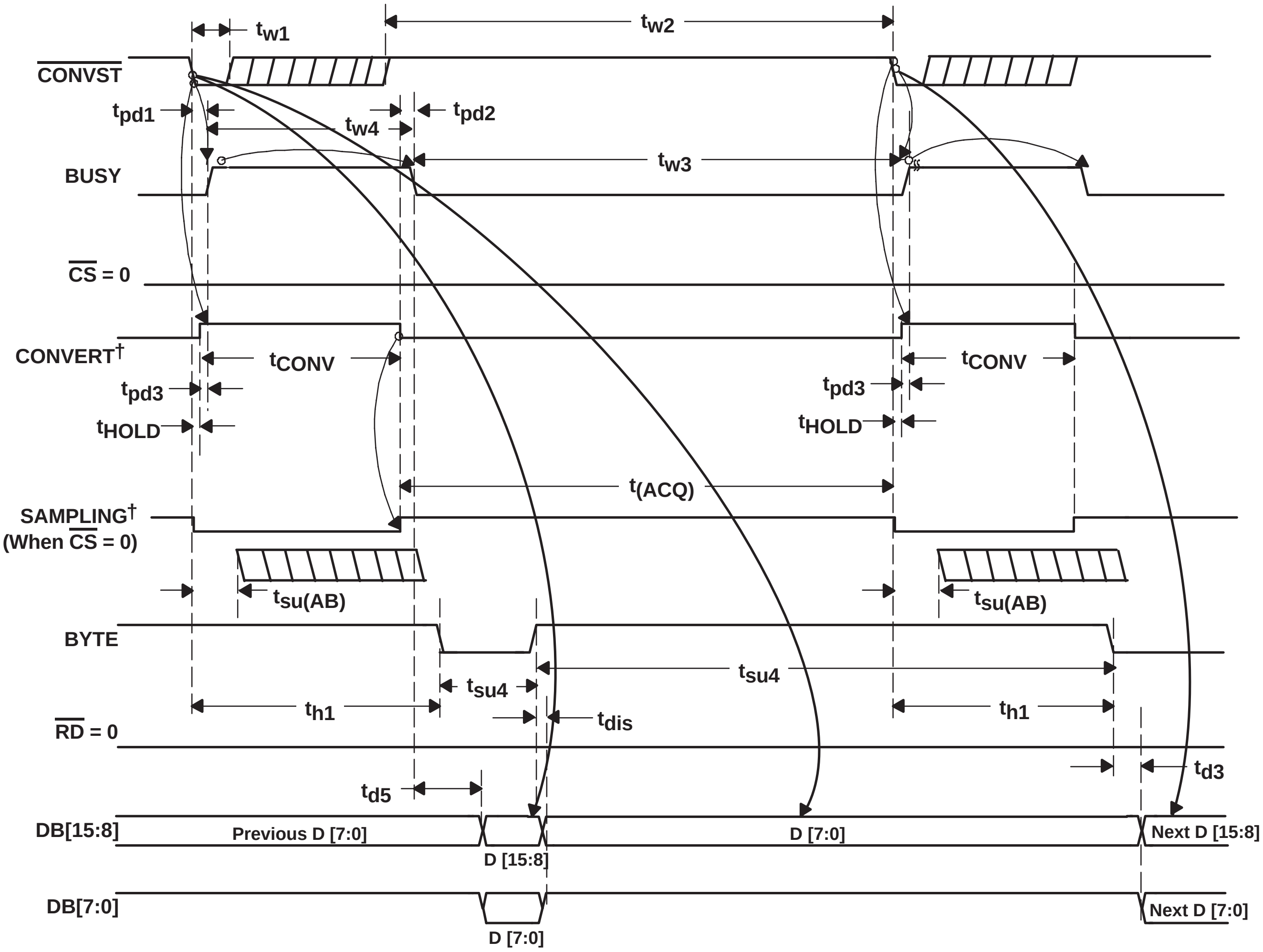
Figure 2. Timing for Conversion and Acquisition Cycles With CS Toggling, RD Tied to BDGND

PRODUCT PREVIEW



†Signal internal to device

Figure 3. Timing for Conversion and Acquisition Cycles With $\overline{\text{CS}}$ Tied to BDGND, $\overline{\text{RD}}$ Toggling



†Signal internal to device

Figure 4. Timing for Conversion and Acquisition Cycles With CS and RD Tied to BDGND—Auto Read

PRODUCT PREVIEW

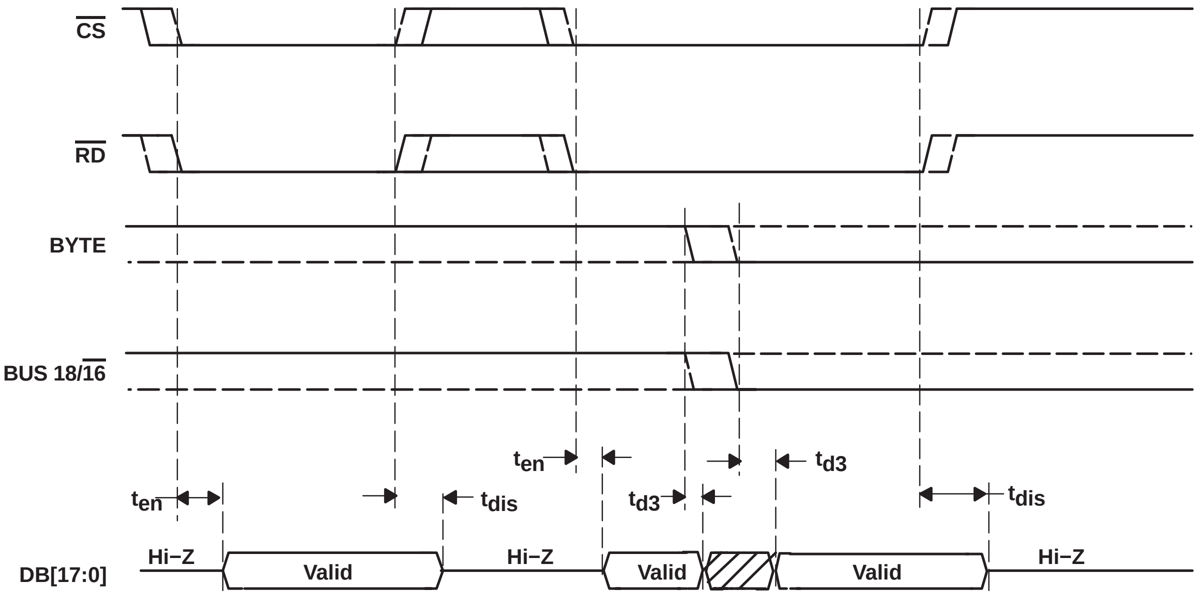


Figure 5. Detailed Timing for Read Cycles

APPLICATION INFORMATION

MICROCONTROLLER INTERFACING

ADS8381 to 8-Bit Microcontroller Interface

Figure 6 shows a parallel interface between the ADS8381 and a typical microcontroller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microcontroller.

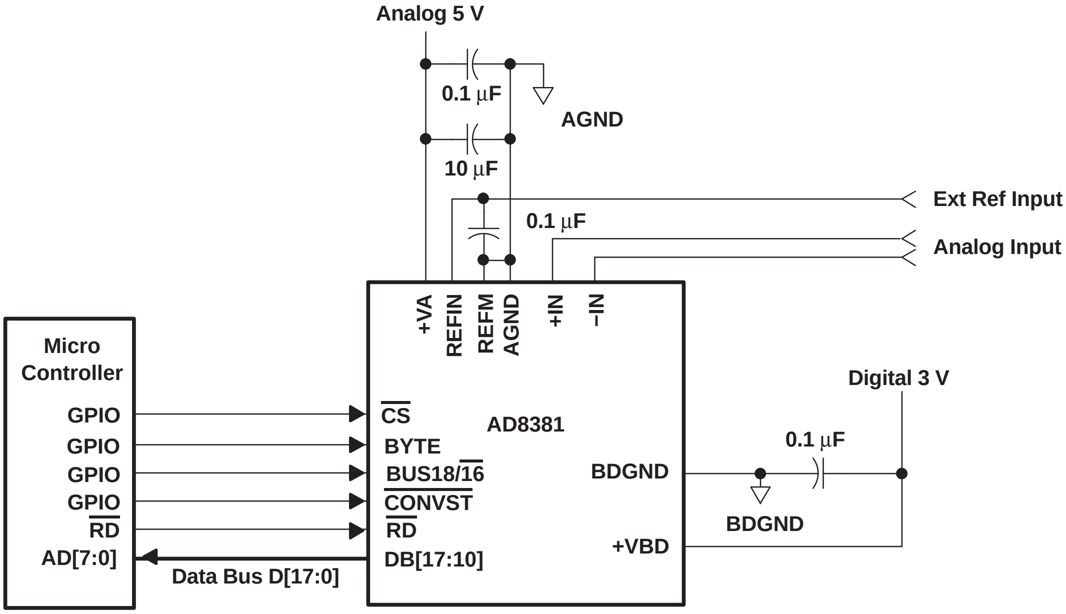


Figure 6. ADS8381 Application Circuitry

PRINCIPLES OF OPERATION

The ADS8381 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 6 for the application circuit for the ADS8381.

The conversion clock is generated internally. The conversion time of 1.3 µs is capable of sustaining a 580-kHz throughput.

The analog input is provided to two input pins: +IN and −IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8381 can operate with an external reference with a range from 2.5 V to 4.2 V.

ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and −IN inputs is captured on the internal capacitor array. The voltage on the −IN input is limited between –0.2 V and 0.2 V, allowing the input to reject small signals which are common to both the +IN and −IN inputs. The +IN input has a range of –0.2 V to V_{ref} + 0.2 V. The input span (+IN − (−IN)) is limited to 0 V to V_{ref}.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8381 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to an 18-bit settling level within the acquisition time (400 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and −IN inputs and the span (+IN − (−IN)) should be within the limits specified. Outside of these ranges, the converter’s linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

Care should be taken to ensure that the output impedance of the sources driving the +IN and −IN inputs are matched. If this is not observed, the two inputs could have different setting times. This may result in offset error, gain error, and linearity error which changes with temperature and input voltage.

DIGITAL INTERFACE

Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8381 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high), while $\overline{\text{CS}}$ is low. The ADS8381 switches from the sample to the hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY output is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high throughout the conversion process and returns low when the conversion has ended.

Sampling starts with the falling edge of the BUSY signal when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought low in order to enable the parallel output bus with the conversion.

Reading Data

The ADS8381 outputs full parallel data in straight binary format as shown in Table 1. The parallel output is active when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{\text{CONVST}}$. This is 125 ns prior to the falling edge of $\overline{\text{CONVST}}$ and 40 ns after the falling edge. No data read should attempted within this zone. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ sets the parallel output to 3-state. BYTE and BUS18/$\overline{\text{16}}$ are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/$\overline{\text{16}}$ is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 1 for ideal output codes.

Table 1. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
Full scale range	(+V_{ref})		
Least significant bit (LSB)	(+V_{ref})/262144	**BINARY CODE**	**HEX CODE**
+Full scale	(+V_{ref}) – 1 LSB	11 1111 1111 1111 1111	3FFFF
Midscale	(+V_{ref})/2	10 0000 0000 0000 0000	20000
Midscale – 1 LSB	(+V_{ref})/2 – 1 LSB	01 1111 1111 1111 1111	1FFFF
Zero	0 V	00 0000 0000 0000 0000	00000

The output data is a full 18-bit word (D17−D0) on DB17–DB0 pins (MSB−LSB) if both BUS18/$\overline{\text{16}}$ and BYTE are low.

The result may also be read on an 16-bit bus by using only pins DB17−DB2. In this case two reads are necessary: the first as before, leaving both BUS18/$\overline{\text{16}}$ and BYTE low and reading the 16 most significant bits (D17−D2) on pins DB17−DB2, then bringing BUS18/$\overline{\text{16}}$ high while holding BYTE low. When BUS18/$\overline{\text{16}}$ is high, the lower two bits (D1–D0) appear on pins DB3−DB2.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17−DB10. In this case three reads are necessary: the first as before, leaving both BUS18/$\overline{\text{16}}$ and BYTE low and reading the 8 most significant bits on pins DB17−DB10, then bringing BYTE high while holding BUS18/$\overline{\text{16}}$ low. When BYTE is high, the medium bits (D9−D2) appear on pins DB17−DB10. The last read is done by bringing BUS18/$\overline{\text{16}}$ high while holding BYTE high. When BUS18/$\overline{\text{16}}$ is high, the lower two bits (D1–D0) appear on pins DB11−DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active $\overline{\text{RD}}$ (toggling) or with $\overline{\text{RD}}$ held low for simplicity. This is referred to as the AUTO READ operation. Note that $\overline{\text{RD}}$ may not be tied to BDGND permanently due to the requirement of power-on initialization.

Table 2. Conversion Data Read Out

BYTE	BUS18/$\overline{\text{16}}$	DATA READ OUT				
		DB17−DB12 PINS	**DB11−DB10 PINS**	**DB9−DB4 PINS**	**DB3−DB2 PINS**	**DB1−DB0 PINS**
High	High	All One’s	D1−D0	All One’s	All One’s	All One’s
Low	High	All One’s	All One’s	All One’s	D1−D0	All One’s
High	Low	D9−D4	D3−D2	All One’s	All One’s	All One’s
Low	Low	D17−D12	D11−D10	D9−D4	D3−D2	D1−D0

RESET

The device can be reset through the use of the combination fo $\overline{\text{CS}}$ and $\overline{\text{CONVST}}$. Since the BUSY signal is held at high during the conversion, either one of these conditions triggers an internal self-clear reset to the converter.

- Issue a $\overline{\text{CONVST}}$ when $\overline{\text{CS}}$ is low and internal CONVERT state is high. The falling edge of $\overline{\text{CONVST}}$ starts a reset.
- Issue a $\overline{\text{CS}}$ (select the device) while internal CONVERT state is high. The falling edge of $\overline{\text{CS}}$ causes a reset.

Once the device is reset, all output latches are cleared (set to zeroes) and the BUSY signal is brought low. A new sampling period is started at the falling edge of the BUSY signal immediately after the instant of the internal reset.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8381 circuitry.

As the ADS8381 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8381 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-µF bypass capacitor is recommended from pin 1 (REFIN) directly to pin 48 (REFM). REFM and AGND should be shorted on the same ground plane under the device.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8381 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of the capacitor. In addition, a 1-µF to 10-µF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

Table 3. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
SUPPLY PINS		
Pin pairs that require shortest path to decoupling capacitors	(4,5), (8,9), (10,11), (13,15), (43,44), (45,46)	(24,25)
Pins that require no decoupling	12, 14	37

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated