



## 24-Bit ANALOG-TO-DIGITAL CONVERTER

### FEATURES

- 24 BITS NO MISSING CODES
- SIMULTANEOUS 50Hz AND 60Hz REJECTION (–90dB MINIMUM)
- 0.0015% INL
- 21 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)
- PGA GAINS FROM 1 TO 128
- SINGLE CYCLE SETTLING
- PROGRAMMABLE DATA OUTPUT RATES
- EXTERNAL DIFFERENTIAL REFERENCE OF 0.1V TO 5V
- ON-CHIP CALIBRATION
- SPI™ COMPATIBLE
- 2.7V TO 5.25V SUPPLY RANGE
- 600μW POWER CONSUMPTION
- UP TO EIGHT INPUT CHANNELS
- UP TO EIGHT DATA I/O

### APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- WEIGH SCALES
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTATION

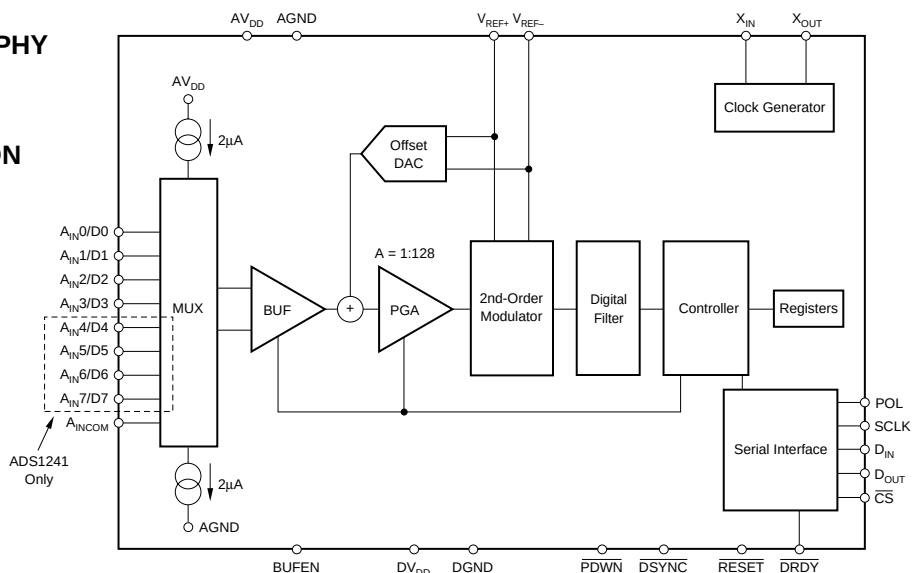
### DESCRIPTION

The ADS1240 and ADS1241 are precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converters with 24-bit resolution operating from 2.7V to 5.25V power supplies. The delta-sigma A/D converter provides up to 24 bits of no missing code performance and effective resolution of 21 bits.

The input channels are multiplexed. Internal buffering can be selected to provide very high input impedance for direct connection to transducers or low-level voltage signals. Burnout current sources are provided that allow for detection of an open or shorted sensor. An 8-bit Digital-to-Analog (D/A) converter provides an offset correction with a range of 50% of the Full-Scale Range (FSR).

The Programmable Gain Amplifier (PGA) provides selectable gains of 1 to 128, with an effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a 2nd-order delta-sigma modulator and programmable Finite-Impulse Response (FIR) filter that provides a simultaneous 50Hz and 60Hz notch. The reference input is differential and can be used for ratiometric conversion.

The serial interface is SPI compatible. Up to eight bits of data I/O are also provided that can be used for input or output. The ADS1240 and ADS1241 are designed for high-resolution measurement applications in smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|                                         |                                |
|-----------------------------------------|--------------------------------|
| $AV_{DD}$ to DGND .....                 | –0.3V to +6V                   |
| $DV_{DD}$ to DGND .....                 | –0.3V to +6V                   |
| Input Current .....                     | 100mA, Momentary               |
| DGND to AGND .....                      | –0.3V to 0.3V                  |
| Input Current .....                     | 10mA, Continuous               |
| $A_{IN}$ .....                          | AGND –0.5V to $AV_{DD}$ + 0.5V |
| Digital Input Voltage to DGND .....     | –0.3V to $DV_{DD}$ + 0.3V      |
| Digital Output Voltage to DGND .....    | –0.3V to $DV_{DD}$ + 0.3V      |
| Maximum Junction Temperature .....      | +150°C                         |
| Operating Temperature Range .....       | –40°C to +85°C                 |
| Storage Temperature Range .....         | –60°C to +150°C                |
| Lead Temperature (soldering, 10s) ..... | +300°C                         |

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## EVALUATION MODULE ORDERING INFORMATION

| PRODUCT    | DESCRIPTION                           |
|------------|---------------------------------------|
| ADS1241EVM | ADS1240 and ADS1241 Evaluation Module |

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR <sup>(1)</sup> | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---------|--------------|-----------------------------------|-----------------------------|-----------------|-----------------|---------------------------|
| ADS1240 | SSOP-24      | DB                                | –40°C to +85°C              | ADS1240E        | ADS1240E        | Rails, 60                 |
| "       | "            | "                                 | "                           | "               | ADS1240E/1K     | Tape and Reel, 1000       |
| ADS1241 | SSOP-28      | DB                                | –40°C to +85°C              | ADS1241E        | ADS1241E        | Rails, 48                 |
| "       | "            | "                                 | "                           | "               | ADS1241E/1K     | Tape and Reel, 1000       |

NOTE: (1) For the most current specifications and package information, refer to our web site at [www.ti.com](http://www.ti.com).

## DIGITAL CHARACTERISTICS: –40°C to +85°C, $DV_{DD}$ 2.7V to 5.25V

| PARAMETER                      | CONDITIONS            | MIN                 | TYP  | MAX                 | UNITS         |
|--------------------------------|-----------------------|---------------------|------|---------------------|---------------|
| Digital Input/Output           |                       |                     |      |                     |               |
| Logic Family                   |                       |                     | CMOS |                     |               |
| Logic Level: $V_{IH}$          |                       | $0.8 \cdot DV_{DD}$ |      | $DV_{DD}$           | V             |
| $V_{IL}$                       |                       | DGND                |      | $0.2 \cdot DV_{DD}$ | V             |
| $V_{OH}$                       | $I_{OH} = 1\text{mA}$ | $DV_{DD} - 0.4$     |      |                     | V             |
| $V_{OL}$                       | $I_{OL} = 1\text{mA}$ | DGND                |      | DGND + 0.4          | V             |
| Input Leakage: $I_{IH}$        | $V_I = DV_{DD}$       |                     |      | 10                  | $\mu\text{A}$ |
| $I_{IL}$                       | $V_I = 0$             | –10                 |      |                     | $\mu\text{A}$ |
| Master Clock Rate: $f_{OSC}$   |                       | 1                   |      | 5                   | MHz           |
| Master Clock Period: $t_{OSC}$ | $1/f_{OSC}$           | 200                 |      | 1000                | ns            |

# ELECTRICAL CHARACTERISTICS: $AV_{DD} = 5V$

All specifications  $T_{MIN}$  to  $T_{MAX}$ ,  $AV_{DD} = +5V$ ,  $DV_{DD} = +2.7V$  to  $5.25V$ ,  $f_{MOD} = 19.2kHz$ ,  $PGA = 1$ , Buffer ON,  $f_{DATA} = 15Hz$ , and  $V_{REF} = +2.5V$ , unless otherwise specified.

| PARAMETER                                                                    | CONDITIONS                                                                                                                                                          | ADS1240<br>ADS1241        |                                                            |                                                  | UNITS                                          |
|------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------------------------------------------------------------|--------------------------------------------------|------------------------------------------------|
|                                                                              |                                                                                                                                                                     | MIN                       | TYP                                                        | MAX                                              |                                                |
| <b>ANALOG INPUT (<math>A_{IN0} - A_{IN7}</math>, <math>A_{INCOM}</math>)</b> |                                                                                                                                                                     |                           |                                                            |                                                  |                                                |
| Analog Input Range                                                           | Buffer OFF<br>Buffer ON                                                                                                                                             | AGND – 0.1<br>AGND + 0.05 |                                                            | $AV_{DD} + 0.1$<br>$AV_{DD} - 1.5$               | V<br>V                                         |
| Full-Scale Input Range                                                       | (In+) – (In–), See Block Diagram, RANGE = 0<br>RANGE = 1                                                                                                            |                           |                                                            | $\pm V_{REF}/PGA$<br>$\pm V_{REF}/(2 \cdot PGA)$ | V<br>V                                         |
| Differential Input Impedance                                                 | Buffer OFF<br>Buffer ON                                                                                                                                             |                           | 5/PGA<br>5                                                 |                                                  | M $\Omega$<br>G $\Omega$                       |
| Bandwidth                                                                    |                                                                                                                                                                     |                           |                                                            |                                                  |                                                |
| $f_{DATA} = 3.75Hz$                                                          | –3dB                                                                                                                                                                |                           | 1.65                                                       |                                                  | Hz                                             |
| $f_{DATA} = 7.50Hz$                                                          | –3dB                                                                                                                                                                |                           | 3.44                                                       |                                                  | Hz                                             |
| $f_{DATA} = 15.00Hz$                                                         | –3dB                                                                                                                                                                |                           | 14.6                                                       |                                                  | Hz                                             |
| Programmable Gain Amplifier                                                  | User-Selectable Gain Ranges                                                                                                                                         | 1                         |                                                            | 128                                              |                                                |
| Input Capacitance                                                            |                                                                                                                                                                     |                           | 9                                                          |                                                  | pF                                             |
| Input Leakage Current                                                        | Modulator OFF, T = 25°C                                                                                                                                             |                           | 5                                                          |                                                  | pA                                             |
| Burnout Current Sources                                                      |                                                                                                                                                                     |                           | 2                                                          |                                                  | $\mu A$                                        |
| <b>OFFSET DAC</b>                                                            |                                                                                                                                                                     |                           |                                                            |                                                  |                                                |
| Offset DAC Range                                                             | RANGE = 0<br>RANGE = 1                                                                                                                                              |                           | $\pm V_{REF}/(2 \cdot PGA)$<br>$\pm V_{REF}/(4 \cdot PGA)$ |                                                  | V<br>V                                         |
| Offset Monotonicity                                                          |                                                                                                                                                                     | 8                         |                                                            |                                                  | Bits                                           |
| Offset DAC Gain Error                                                        |                                                                                                                                                                     |                           | $\pm 10$                                                   |                                                  | %                                              |
| Offset DAC Gain Error Drift                                                  |                                                                                                                                                                     |                           | 1                                                          |                                                  | ppm/°C                                         |
| <b>SYSTEM PERFORMANCE</b>                                                    |                                                                                                                                                                     |                           |                                                            |                                                  |                                                |
| Resolution                                                                   | No Missing Codes                                                                                                                                                    | 24                        |                                                            |                                                  | Bits                                           |
| Integral Nonlinearity                                                        | End Point Fit                                                                                                                                                       |                           |                                                            | $\pm 0.0015$                                     | % of FS                                        |
| Offset Error <sup>(1)</sup>                                                  |                                                                                                                                                                     |                           | 7.5                                                        |                                                  | ppm of FS                                      |
| Offset Drift <sup>(1)</sup>                                                  |                                                                                                                                                                     |                           | 0.02                                                       |                                                  | ppm of FS/°C                                   |
| Gain Error                                                                   |                                                                                                                                                                     |                           | 0.005                                                      |                                                  | %                                              |
| Gain Error Drift <sup>(1)</sup>                                              |                                                                                                                                                                     |                           | 0.5                                                        |                                                  | ppm/°C                                         |
| Common-Mode Rejection                                                        | at DC<br>$f_{CM} = 60Hz$ , $f_{DATA} = 15Hz$<br>$f_{CM} = 50Hz$ , $f_{DATA} = 15Hz$<br>$f_{SIG} = 50Hz$ , $f_{DATA} = 15Hz$<br>$f_{SIG} = 60Hz$ , $f_{DATA} = 15Hz$ | 100                       | 130<br>120<br>100<br>100                                   |                                                  | dB<br>dB<br>dB<br>dB                           |
| Normal-Mode Rejection                                                        |                                                                                                                                                                     |                           |                                                            |                                                  |                                                |
| Output Noise                                                                 |                                                                                                                                                                     |                           | See Typical Characteristics                                |                                                  |                                                |
| Power-Supply Rejection                                                       | at DC, dB = $-20 \log(\Delta V_{OUT}/\Delta V_{DD})^{(2)}$                                                                                                          | 80                        | 95                                                         |                                                  | dB                                             |
| <b>VOLTAGE REFERENCE INPUT</b>                                               |                                                                                                                                                                     |                           |                                                            |                                                  |                                                |
| $V_{REF}$                                                                    | $V_{REF} \equiv (REF\ IN+) - (REF\ IN-)$ , RANGE = 0                                                                                                                | 0.1                       | 2.5                                                        | 2.6                                              | V                                              |
| Reference Input Range                                                        | REF IN+, REF IN–<br>RANGE = 1                                                                                                                                       | 0<br>0.1                  |                                                            | $AV_{DD}$<br>$AV_{DD}$                           | V<br>V                                         |
| Common-Mode Rejection                                                        | at DC                                                                                                                                                               |                           | 120                                                        |                                                  | dB                                             |
| Common-Mode Rejection                                                        | $f_{VREFCM} = 60Hz$ , $f_{DATA} = 15Hz$                                                                                                                             |                           | 120                                                        |                                                  | dB                                             |
| Bias Current <sup>(3)</sup>                                                  | $V_{REF} = 2.5V$                                                                                                                                                    |                           | 1.3                                                        |                                                  | $\mu A$                                        |
| <b>POWER-SUPPLY REQUIREMENTS</b>                                             |                                                                                                                                                                     |                           |                                                            |                                                  |                                                |
| Power-Supply Voltage                                                         | $AV_{DD}$                                                                                                                                                           | 4.75                      |                                                            | 5.25                                             | V                                              |
| Analog Current                                                               | PDWN = 0, or SLEEP<br>PGA = 1, Buffer OFF<br>PGA = 128, Buffer OFF<br>PGA = 1, Buffer ON<br>PGA = 128, Buffer ON                                                    |                           | 1<br>120<br>400<br>160<br>760                              |                                                  | nA<br>$\mu A$<br>$\mu A$<br>$\mu A$<br>$\mu A$ |
| Digital Current                                                              | Normal Mode, $DV_{DD} = 5V$<br>SLEEP Mode, $DV_{DD} = 5V$<br>Read Data Continuous Mode, $DV_{DD} = 5V$<br>PDWN                                                      |                           | 80<br>60<br>230<br>0.5                                     | 125                                              | $\mu A$<br>$\mu A$<br>$\mu A$<br>nA            |
| Power Dissipation                                                            | PGA = 1, Buffer OFF, $DV_{DD} = 5V$                                                                                                                                 |                           | 1.1                                                        | 1.9                                              | mW                                             |

NOTES: (1) Calibration can minimize these errors to the level of the noise.

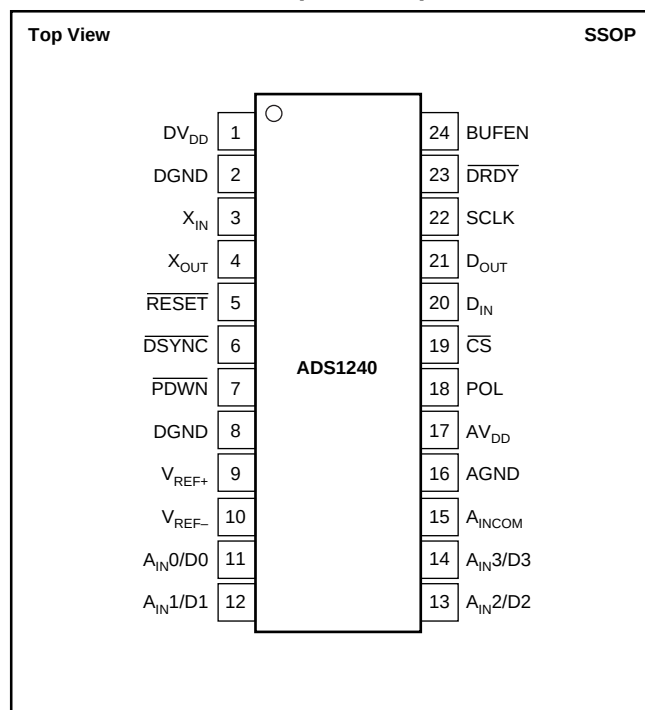
(2)  $\Delta V_{OUT}$  is a change in digital result.

(3) 12pF switched capacitor at  $f_{SAMP}$  clock frequency.

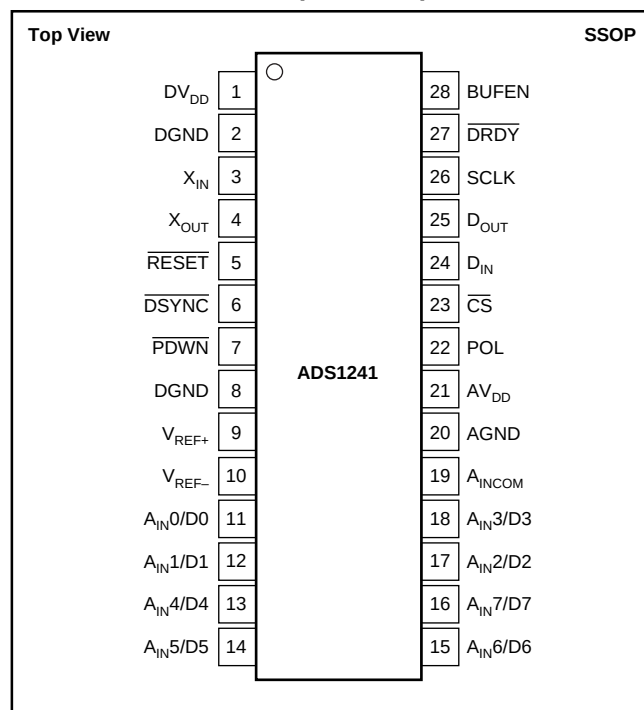
All specifications  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $\text{AV}_{\text{DD}} = +3\text{V}$ ,  $\text{DV}_{\text{DD}} = +2.7\text{V}$  to  $5.25\text{V}$ ,  $f_{\text{MOD}} = 19.2\text{kHz}$ ,  $\text{PGA} = 1$ , Buffer ON,  $f_{\text{DATA}} = 15\text{Hz}$ , and  $\text{V}_{\text{REF}} = +1.25\text{V}$ , unless otherwise specified.

NOTES: (1) Calibration can minimize these errors to the level of the noise.  
(2)  $\Delta V_{OUT}$  is a change in digital result.  
(3) 12pF switched capacitor at  $f_{SAMP}$  clock frequency.

## PIN CONFIGURATION (ADS1240)



## PIN CONFIGURATION (ADS1241)



## PIN DESCRIPTIONS (ADS1240)

| PIN NUMBER | NAME                 | DESCRIPTION                                                                                 |
|------------|----------------------|---------------------------------------------------------------------------------------------|
| 1          | DV <sub>DD</sub>     | Digital Power Supply                                                                        |
| 2          | DGND                 | Digital Ground                                                                              |
| 3          | X <sub>IN</sub>      | Clock Input                                                                                 |
| 4          | X <sub>OUT</sub>     | Clock Output, used with external crystals.                                                  |
| 5          | RESET                | Active LOW, resets the entire device.                                                       |
| 6          | DSYNC                | Active LOW, Synchronization Control                                                         |
| 7          | PDWN                 | Active LOW, Power Down. The power down function shuts down the analog and digital circuits. |
| 8          | DGND                 | Digital Ground                                                                              |
| 9          | V <sub>REF+</sub>    | Positive Differential Reference Input                                                       |
| 10         | V <sub>REF-</sub>    | Negative Differential Reference Input                                                       |
| 11         | A <sub>IN</sub> 0/D0 | Analog Input 0 / Data I/O 0                                                                 |
| 12         | A <sub>IN</sub> 1/D1 | Analog Input 1 / Data I/O 1                                                                 |
| 13         | A <sub>IN</sub> 2/D2 | Analog Input 2 / Data I/O 2                                                                 |
| 14         | A <sub>IN</sub> 3/D3 | Analog Input 3 / Data I/O 3                                                                 |
| 15         | A <sub>IN</sub> COM  | Analog Input Common, connect to AGND if unused.                                             |
| 16         | AGND                 | Analog Ground                                                                               |
| 17         | AV <sub>DD</sub>     | Analog Power Supply                                                                         |
| 18         | POL                  | Serial Clock Polarity                                                                       |
| 19         | CS                   | Active LOW, Chip Select                                                                     |
| 20         | D <sub>IN</sub>      | Serial Data Input, Schmitt Trigger                                                          |
| 21         | D <sub>OUT</sub>     | Serial Data Output                                                                          |
| 22         | SCLK                 | Serial Clock, Schmitt Trigger                                                               |
| 23         | DRDY                 | Active LOW, Data Ready                                                                      |
| 24         | BUFEN                | Buffer Enable                                                                               |

## PIN DESCRIPTIONS (ADS1241)

| PIN NUMBER | NAME                 | DESCRIPTION                                                                                 |
|------------|----------------------|---------------------------------------------------------------------------------------------|
| 1          | DV <sub>DD</sub>     | Digital Power Supply                                                                        |
| 2          | DGND                 | Digital Ground                                                                              |
| 3          | X <sub>IN</sub>      | Clock Input                                                                                 |
| 4          | X <sub>OUT</sub>     | Clock Output, used with external crystals.                                                  |
| 5          | RESET                | Active LOW, resets the entire device.                                                       |
| 6          | DSYNC                | Active LOW, Synchronization Control                                                         |
| 7          | PDWN                 | Active LOW, Power Down. The power down function shuts down the analog and digital circuits. |
| 8          | DGND                 | Digital Ground                                                                              |
| 9          | V <sub>REF+</sub>    | Positive Differential Reference Input                                                       |
| 10         | V <sub>REF-</sub>    | Negative Differential Reference Input                                                       |
| 11         | A <sub>IN</sub> 0/D0 | Analog Input 0 / Data I/O 0                                                                 |
| 12         | A <sub>IN</sub> 1/D1 | Analog Input 1 / Data I/O 1                                                                 |
| 13         | A <sub>IN</sub> 4/D4 | Analog Input 4 / Data I/O 4                                                                 |
| 14         | A <sub>IN</sub> 5/D5 | Analog Input 5 / Data I/O 5                                                                 |
| 15         | A <sub>IN</sub> 6/D6 | Analog Input 6 / Data I/O 6                                                                 |
| 16         | A <sub>IN</sub> 7/D7 | Analog Input 7 / Data I/O 7                                                                 |
| 17         | A <sub>IN</sub> 2/D2 | Analog Input 2 / Data I/O 2                                                                 |
| 18         | A <sub>IN</sub> 3/D3 | Analog Input 3 / Data I/O 3                                                                 |
| 19         | A <sub>IN</sub> COM  | Analog Input Common, connect to AGND if unused.                                             |
| 20         | AGND                 | Analog Ground                                                                               |
| 21         | AV <sub>DD</sub>     | Analog Power Supply                                                                         |
| 22         | POL                  | Serial Clock Polarity                                                                       |
| 23         | CS                   | Active LOW, Chip Select                                                                     |
| 24         | D <sub>IN</sub>      | Serial Data Input, Schmitt Trigger                                                          |
| 25         | D <sub>OUT</sub>     | Serial Data Output                                                                          |
| 26         | SCLK                 | Serial Clock, Schmitt Trigger                                                               |
| 27         | DRDY                 | Active LOW, Data Ready                                                                      |
| 28         | BUFEN                | Buffer Enable                                                                               |

## TIMING DIAGRAMS

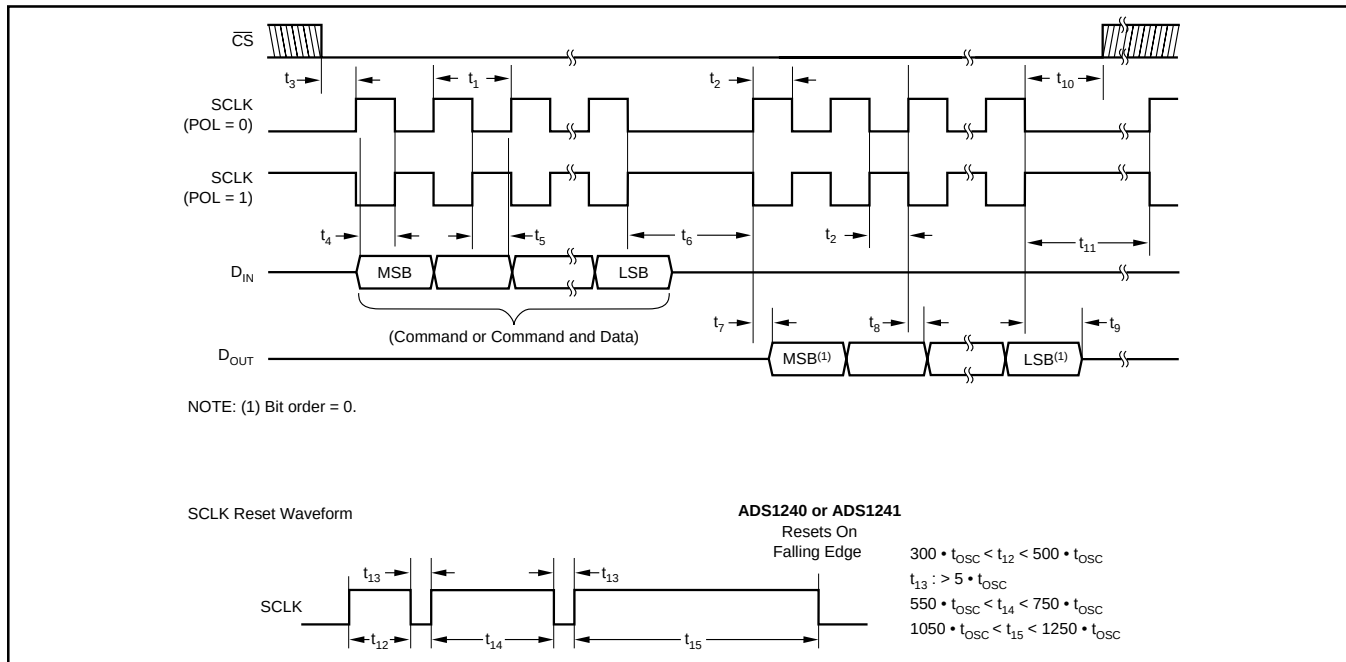


DIAGRAM 1.

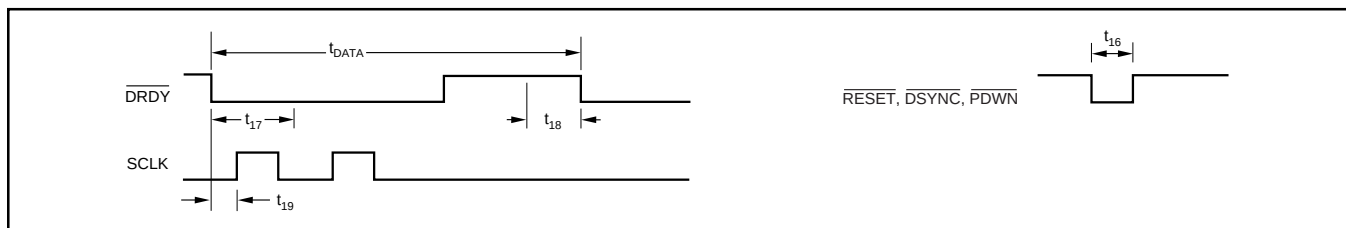


DIAGRAM 2.

## TIMING CHARACTERISTICS TABLES

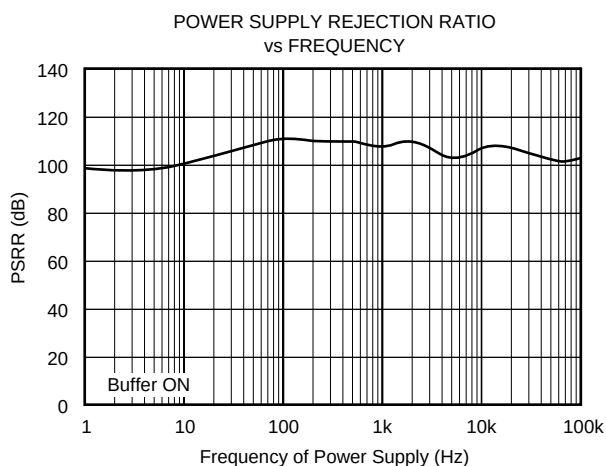
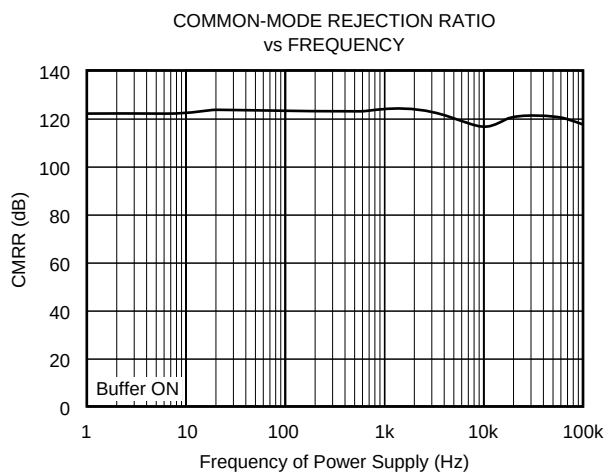
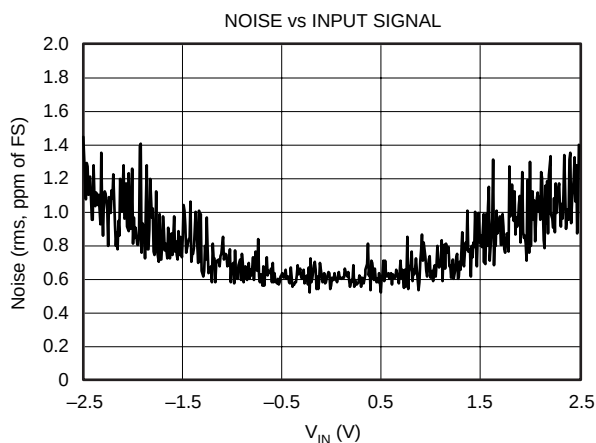
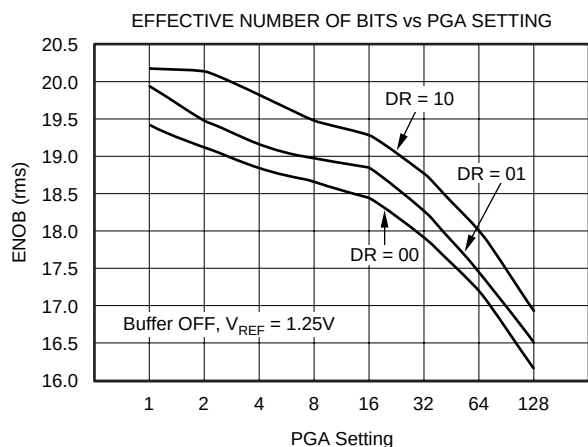
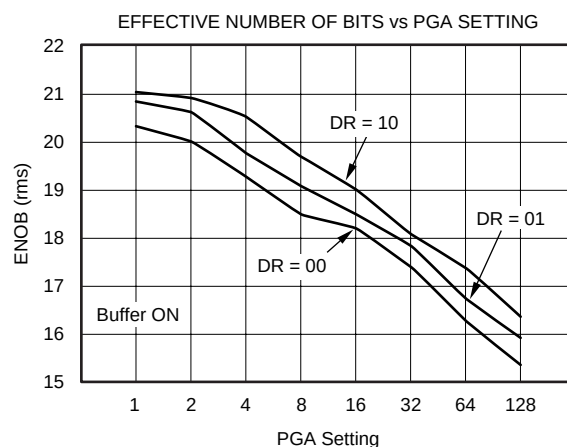
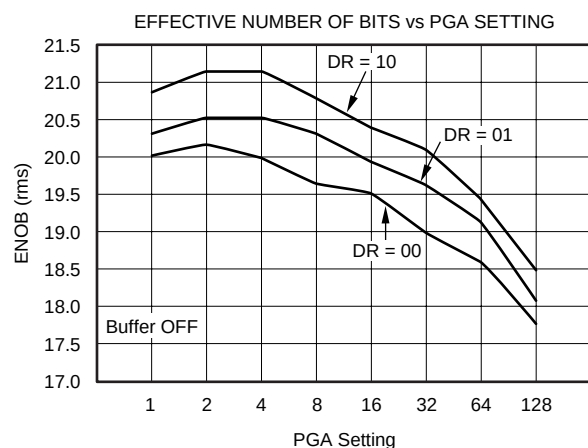
| SPEC        | DESCRIPTION                                                                                                                                                                                                                     | MIN               | MAX  | UNITS                                                                                            |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------|--------------------------------------------------------------------------------------------------|
| $t_1$       | SCLK Period                                                                                                                                                                                                                     | 4                 | 3    | $t_{OSC}$ Periods<br>$\overline{DRDY}$ Periods                                                   |
| $t_2$       | SCLK Pulse Width, HIGH and LOW                                                                                                                                                                                                  | 200               |      | ns                                                                                               |
| $t_3$       | $\overline{CS}$ low to first SCLK Edge; Setup Time <sup>(2)</sup>                                                                                                                                                               | 0                 |      | ns                                                                                               |
| $t_4$       | $D_{IN}$ Valid to SCLK Edge; Setup Time                                                                                                                                                                                         | 50                |      | ns                                                                                               |
| $t_5$       | Valid $D_{IN}$ to SCLK Edge; Hold Time                                                                                                                                                                                          | 50                |      | ns                                                                                               |
| $t_6$       | Delay between last SCLK edge for $D_{IN}$ and first SCLK edge for $D_{OUT}$ :<br>RDATA, RDATA, RREG, WREG                                                                                                                       | 50                |      | $t_{OSC}$ Periods                                                                                |
| $t_7^{(1)}$ | SCLK Edge to Valid New $D_{OUT}$                                                                                                                                                                                                |                   | 50   | ns                                                                                               |
| $t_8^{(1)}$ | SCLK Edge to $D_{OUT}$ , Hold Time                                                                                                                                                                                              | 0                 |      | ns                                                                                               |
| $t_9$       | Last SCLK Edge to $D_{OUT}$ Tri-State<br>NOTE: $D_{OUT}$ goes tri-state immediately when $\overline{CS}$ goes HIGH.                                                                                                             | 6                 | 10   | $t_{OSC}$ Periods                                                                                |
| $t_{10}$    | $\overline{CS}$ LOW time after final SCLK edge.                                                                                                                                                                                 | 0                 |      | ns                                                                                               |
| $t_{11}$    | Final SCLK edge of one command until first edge SCLK of next command:<br>RREG, WREG, DSYNC, SLEEP, RDATA, RDATA, STOPC<br>SELFGCAL, SELFGCAL, SYSOCAL, SYSOCAL<br>SELFGCAL<br>RESET (also SCLK Reset or $\overline{RESET}$ Pin) | 4<br>2<br>4<br>16 |      | $t_{OSC}$ Periods<br>$\overline{DRDY}$ Periods<br>$\overline{DRDY}$ Periods<br>$t_{OSC}$ Periods |
| $t_{16}$    | Pulse Width                                                                                                                                                                                                                     | 4                 |      | $t_{OSC}$ Periods                                                                                |
| $t_{17}$    | Allowed analog input change for next valid conversion.                                                                                                                                                                          |                   | 5000 | $t_{OSC}$ Periods                                                                                |
| $t_{18}$    | DOR update, DOR data not valid.                                                                                                                                                                                                 | 4                 |      | $t_{OSC}$ Periods                                                                                |
| $t_{19}$    | First SCLK after $\overline{DRDY}$ goes LOW:<br>RDATA Mode<br>Any other mode                                                                                                                                                    | 10<br>0           |      | $t_{OSC}$ Periods<br>$t_{OSC}$ Periods                                                           |

NOTES: (1) Load = 20pF || 10kΩ to DGND.

(2)  $\overline{CS}$  may be tied LOW.

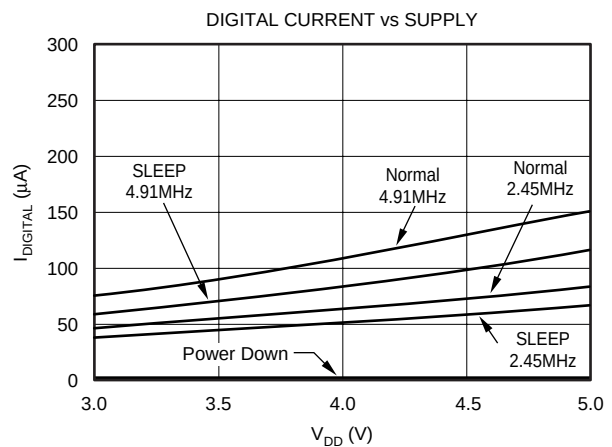
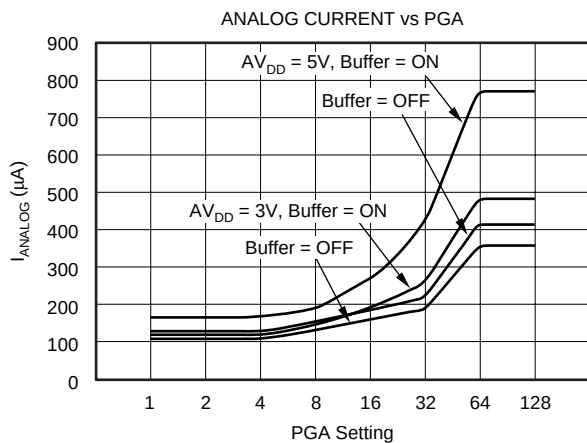
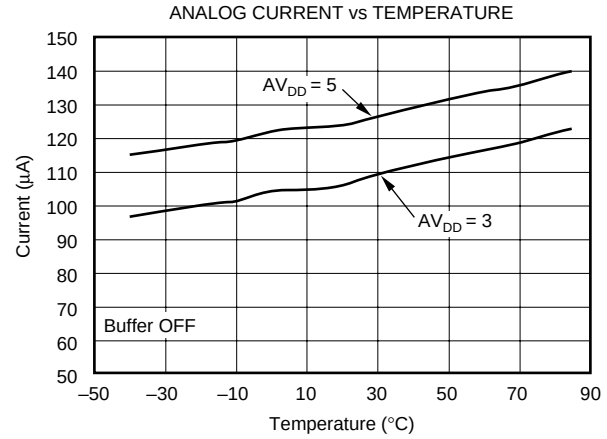
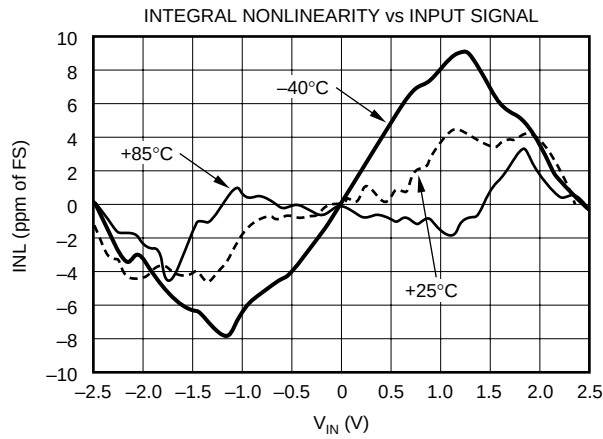
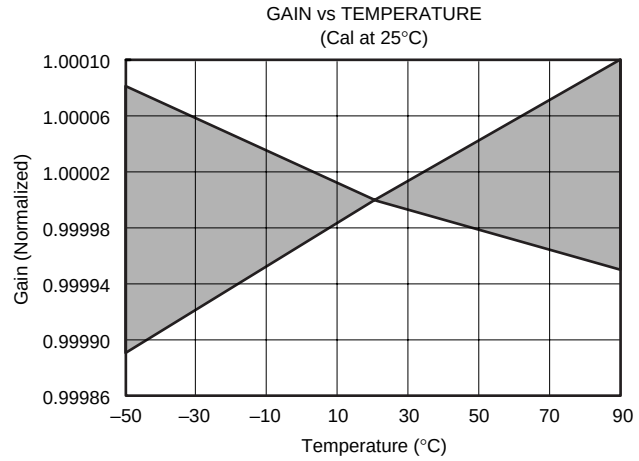
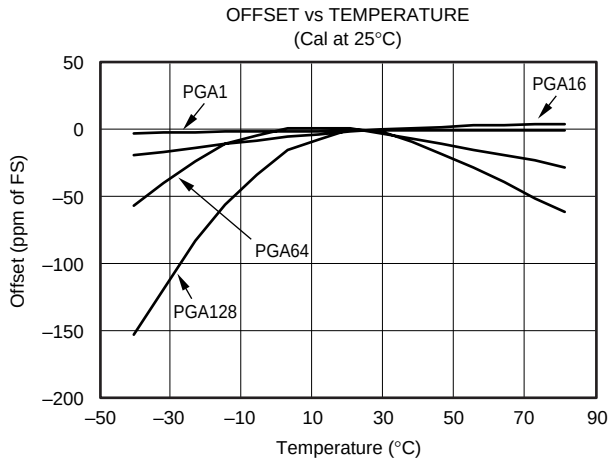
# TYPICAL CHARACTERISTICS

All specifications,  $AV_{DD} = +5V$ ,  $DV_{DD} = +5V$ ,  $f_{OSC} = 2.4576MHz$ ,  $PGA = 1$ ,  $f_{DATA} = 15Hz$ , and  $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +2.5V$ , unless otherwise specified.



# TYPICAL CHARACTERISTICS (Cont.)

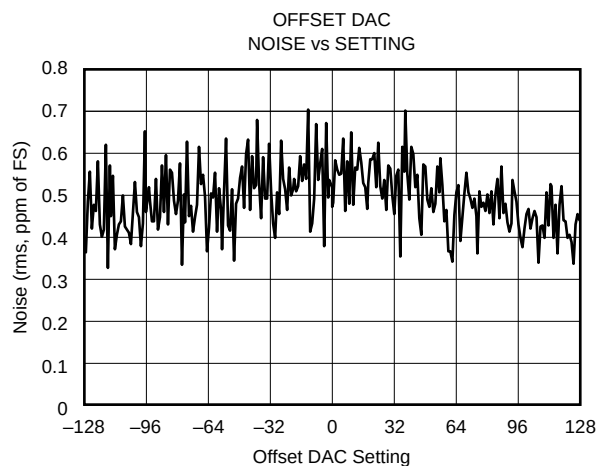
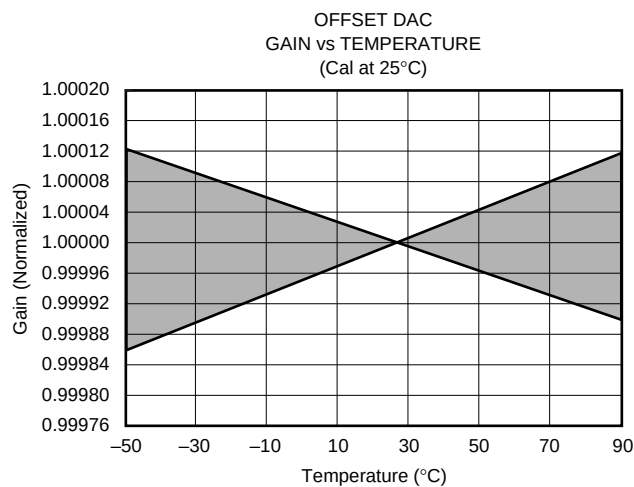
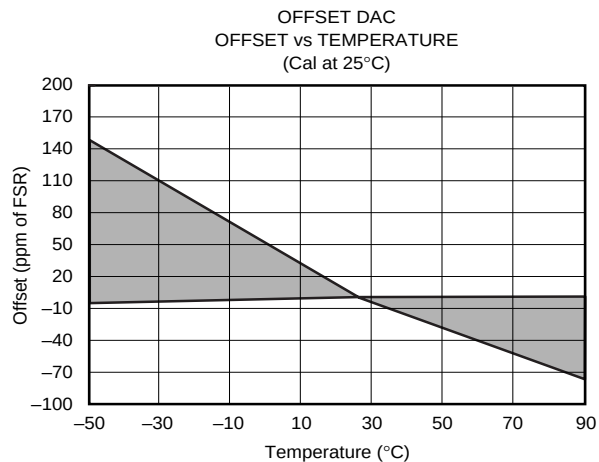
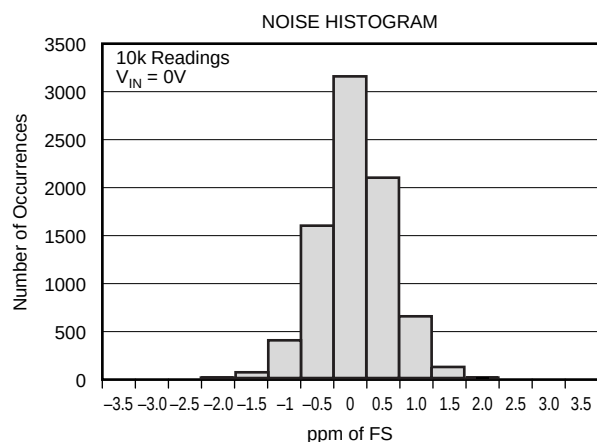
All specifications,  $AV_{DD} = +5V$ ,  $DV_{DD} = +5V$ ,  $f_{OSC} = 2.4576MHz$ ,  $PGA = 1$ ,  $f_{DATA} = 15Hz$ , and  $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +2.5V$ , unless otherwise specified.





# TYPICAL CHARACTERISTICS (Cont.)

All specifications,  $AV_{DD} = +5V$ ,  $DV_{DD} = +5V$ ,  $f_{OSC} = 2.4576MHz$ ,  $PGA = 1$ ,  $f_{DATA} = 15Hz$ , and  $V_{REF} \equiv (REF\ IN+) - (REF\ IN-) = +2.5V$ , unless otherwise specified.



# OVERVIEW

## INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 1. For example, if  $A_{IN}0$  is selected as the positive differential input channel, any other channel can be selected as the negative terminal for the differential input

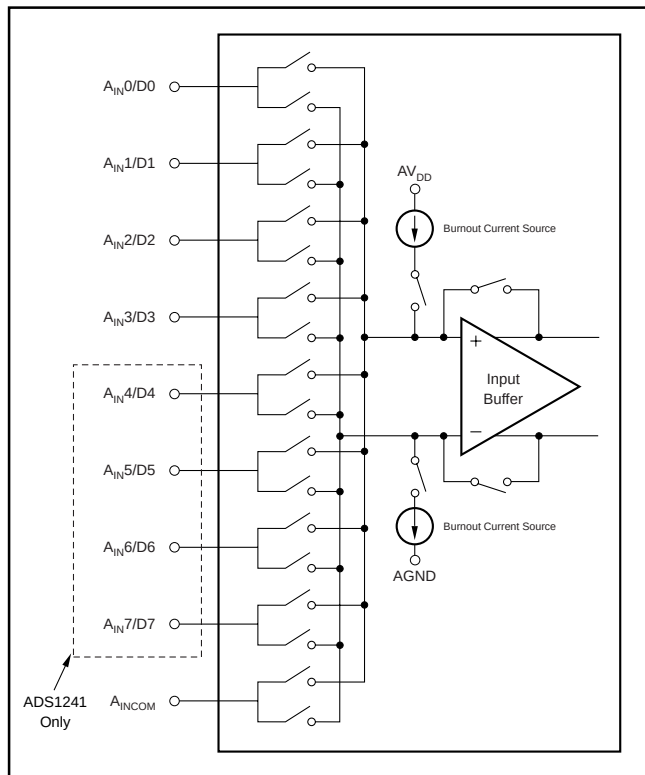


FIGURE 1. Input Multiplexer Configuration.

channel. With this method, it is possible to have up to eight single-ended input channels or four independent differential input channels for the ADS1241, and four single-ended input channels or two independent differential input channels for the ADS1240. Note that  $A_{INCOM}$  can be treated as an input channel.

The ADS1240 and ADS1241 feature a single-cycle settling digital filter that provides valid data on the first conversion after a new channel selection. In order to minimize the settling error, synchronize MUX changes to the conversion beginning, which is indicated by the falling edge of  $\overline{DRDY}$ . In other words, issuing a MUX change through the WREG command immediately after  $\overline{DRDY}$  goes LOW minimizes the settling error. Increasing the time between the conversion beginning ( $\overline{DRDY}$  goes LOW) and the MUX change command ( $t_{DELAY}$ ) results in a settling error in the conversion data, as shown in Figure 2.

## BURNOUT CURRENT SOURCES

The Burnout Current Sources can be used to detect sensor short-circuit or open-circuit conditions. Setting the Burnout Current Sources (BOCS) bit in the SETUP register activates two  $2\mu A$  current sources called burnout current sources. One of the current sources is connected to the converter's negative input and the other is connected to the converter's positive input.

Figure 3 shows the situation for an open-circuit sensor. This is a potential failure mode for many kinds of remotely connected sensors. The current source on the positive input acts as a pull-up, causing the positive input to go to the positive analog supply, and the current source on the negative input acts as a pull-down, causing the negative input to go to ground. The ADS1240/41 therefore outputs full-scale (7FFFF Hex).

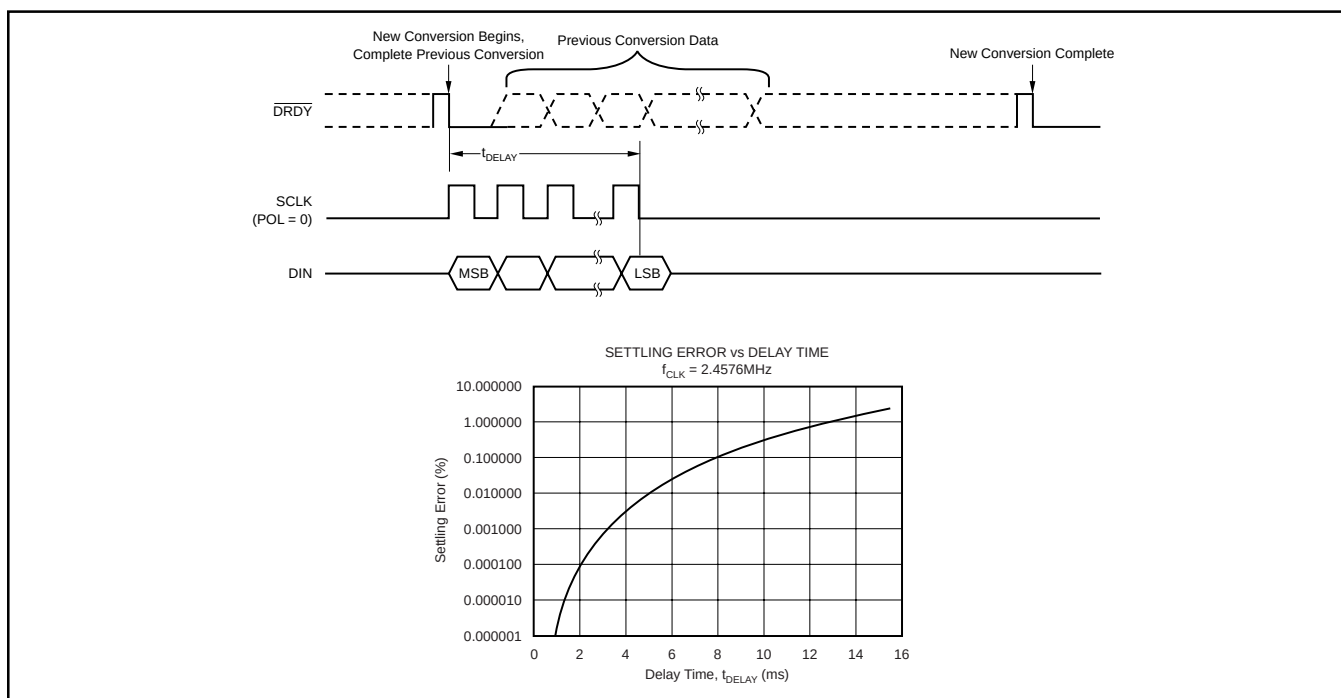


FIGURE 2. Input Multiplexer Configuration.

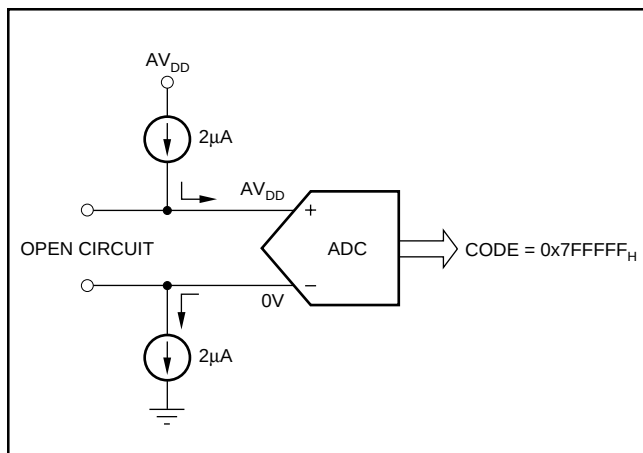


FIGURE 3. Burnout detection while sensor is open-circuited.

Figure 4 shows a short-circuited sensor. Since the inputs are shorted and at the same potential, the ADS1240/41 signal outputs are approximately zero. (Note that the code for shorted inputs is not exactly zero due to internal series resistance, low-level noise and other error sources.)

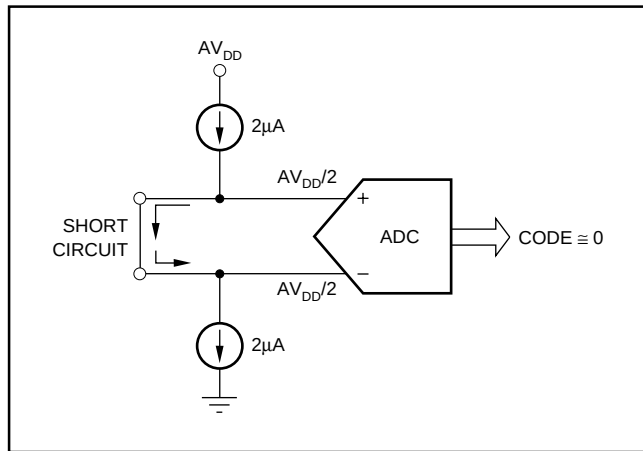


FIGURE 4. Burnout detection while sensor is short-circuited.

## INPUT BUFFER

The input impedance of the ADS1240/41 without the buffer enabled is approximately  $5M\Omega/PGA$ . For systems requiring very high input impedance, the ADS1240/41 provides a chopper-stabilized differential FET-input voltage buffer. When activated, the buffer raises the ADS1240/41 input impedance to approximately  $5G\Omega$ .

The buffer's input range is approximately 50mV to  $AV_{DD} - 1.5V$ . The buffer's linearity will degrade beyond this range. Differential signals should be adjusted so that both signals are within the buffer's input range.

The buffer can be enabled using the BUFEN pin or the BUFEN bit in the ACR register. The buffer is on when the BUFEN pin is high and the BUFEN bit is set to one. If the BUFEN pin is low, the buffer is disabled. If the BUFEN bit is set to zero, the buffer is also disabled.

The buffer draws additional current when activated. The current required by the buffer depends on the PGA setting. When the PGA is set to 1, the buffer uses approximately 50µA; when the PGA is set to 128, the buffer uses approximately 500µA.

## PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 5V full-scale signal, the A/D converter can resolve down to 1µV. With a PGA of 128 and a full-scale signal of 39mV, the A/D converter can resolve down to 75nV.  $AV_{DD}$  current increases with PGA settings higher than 4.

## OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA using the Offset DAC (ODAC) register. The ODAC register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Using the offset DAC does not reduce the performance of the A/D converter. For more details on the ODAC, please refer to TI application report SBAA077.

## MODULATOR

The modulator is a single-loop second-order system. The modulator runs at a clock speed ( $f_{MOD}$ ) that is derived from the external clock ( $f_{OSC}$ ). The frequency division is determined by the SPEED bit in the SETUP register, as shown in Table I.

| $f_{OSC}$ | SPEED<br>BIT | $f_{MOD}$ | DR BITS |        |         | 1st NOTCH<br>FREQ. |
|-----------|--------------|-----------|---------|--------|---------|--------------------|
|           |              |           | 00      | 01     | 10      |                    |
| 2.4576MHz | 0            | 19,200Hz  | 15Hz    | 7.5Hz  | 3.75Hz  | 50/60Hz            |
|           | 1            | 9,600Hz   | 7.5Hz   | 3.75Hz | 1.875Hz | 25/30Hz            |
| 4.9152MHz | 0            | 38,400Hz  | 30Hz    | 15Hz   | 7.5Hz   | 100/120Hz          |
|           | 1            | 19,200Hz  | 15Hz    | 7.5Hz  | 3.75Hz  | 50/60Hz            |

TABLE I. Output Configuration.

## CALIBRATION

The offset and gain errors can be minimized with calibration. The ADS1240 and ADS1241 support both self and system calibration.

Self-calibration of the ADS1240 and ADS1241 corrects internal offset and gain errors and is handled by three commands: SELFCAL, SELFGAL, and SLEFOCAL. The SELFCAL command performs both an offset and gain calibration. SELFGAL performs a gain calibration and SLEFOCAL performs an offset calibration, each of which takes two  $t_{DATA}$  periods to complete. During self-calibration, the ADC inputs are disconnected internally from the input pins. The PGA must be set to 1 prior to issuing a SELFCAL or SELFGAL command. Any PGA is allowed when issuing a SLEFOCAL command. For example, if using  $PGA = 64$ , first set  $PGA = 1$  and issue

SELF CAL. Afterwards set PGA = 64 and issue SELF CAL. For operation with a reference voltage greater than ( $AV_{DD} - 1.5$ ) volts, the buffer must also be turned off during gain self-calibration to avoid exceeding the buffer input range.

System calibration corrects both internal and external offset and gain errors. While performing system calibration, the appropriate signal must be applied to the inputs. The system offset calibration command (SYSOCAL) requires a zero input differential signal (see Table IV, page 18). It then computes the offset that nullifies the offset in the system. The system gain calibration command (SYSGCAL) requires a positive full-scale input signal. It then computes a value to nullify the gain error in the system. Each of these calibrations takes two  $t_{DATA}$  periods to complete. System gain calibration is recommended for the best gain calibration at higher PGAs.

Calibration should be performed after power on, a change in temperature, or a change of the PGA. The RANGE bit (ACR bit 2) must be zero during calibration.

Calibration removes the effects of the ODAC; therefore, disable the ODAC during calibration, and enable again after calibration is complete.

At the completion of calibration, the  $\overline{DRDY}$  signal goes low, indicating the calibration is finished. The first data after calibration should be discarded since it may be corrupt from calibration data remaining in the filter. The second data is always valid.

## EXTERNAL VOLTAGE REFERENCE

The ADS1240 and ADS1241 require an external voltage reference. The selection for the voltage reference value is made through the ACR register.

The external voltage reference is differential and is represented by the voltage difference between the pins:  $+V_{REF}$  and  $-V_{REF}$ . The absolute voltage on either pin,  $+V_{REF}$  or  $-V_{REF}$ , can range from AGND to  $AV_{DD}$ . However, the following limitations apply:

For  $AV_{DD} = 5.0V$  and RANGE = 0 in the ACR, the differential  $V_{REF}$  must not exceed 2.5V.

For  $AV_{DD} = 5.0V$  and RANGE = 1 in the ACR, the differential  $V_{REF}$  must not exceed 5V.

For  $AV_{DD} = 3.0V$  and RANGE = 0 in the ACR, the differential  $V_{REF}$  must not exceed 1.25V.

For  $AV_{DD} = 3.0V$  and RANGE = 1 in the ACR, the differential  $V_{REF}$  must not exceed 2.5V.

## CLOCK GENERATOR

The clock source for the ADS1240 and ADS1241 can be provided from a crystal, oscillator, or external clock. When the clock source is a crystal, external capacitors must be provided to ensure start-up and stable clock frequency. This is shown in both Figure 5 and Table II.  $X_{OUT}$  is only for use with external crystals and it should not be used as a clock driver for external circuitry.

## DIGITAL FILTER

The ADS1240 and ADS1241 have a 1279 tap linear phase

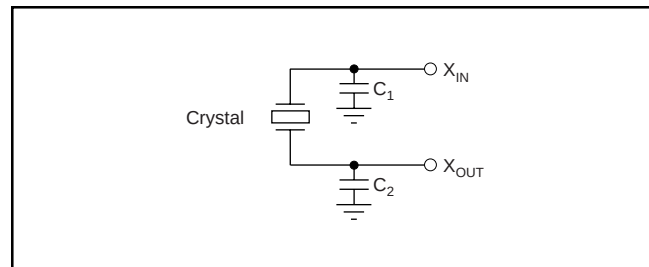


FIGURE 5. Crystal Connection.

| CLOCK SOURCE | FREQUENCY | C <sub>1</sub> | C <sub>2</sub> | PART NUMBER         |
|--------------|-----------|----------------|----------------|---------------------|
| Crystal      | 2.4576    | 0-20pF         | 0-20pF         | ECS, ECSD 2.45 - 32 |
| Crystal      | 4.9152    | 0-20pF         | 0-20pF         | ECS, ECSL 4.91      |
| Crystal      | 4.9152    | 0-20pF         | 0-20pF         | ECS, ECSD 4.91      |
| Crystal      | 4.9152    | 0-20pF         | 0-20pF         | CTS, MP 042 4M9182  |

TABLE II. Recommended Crystals.

Finite Impulse Response (FIR) digital filter that a user can configure for various output data rates. When a 2.4576MHz crystal is used, the device can be programmed for an output data rate of 15Hz, 7.5Hz, or 3.75Hz. Under these conditions, the digital filter rejects both 50Hz and 60Hz interference. Figure 6 shows the digital filter frequency response for data output rates of 15Hz, 7.5Hz, and 3.75Hz.

If a different data output rate is desired, a different crystal frequency can be used. However, the rejection frequencies shift accordingly. For example, a 3.6864MHz master clock with the default register condition has:

$$(3.6864MHz/2.4576MHz) \cdot 15Hz = 22.5Hz \text{ data output rate}$$

and the first and second notch is:

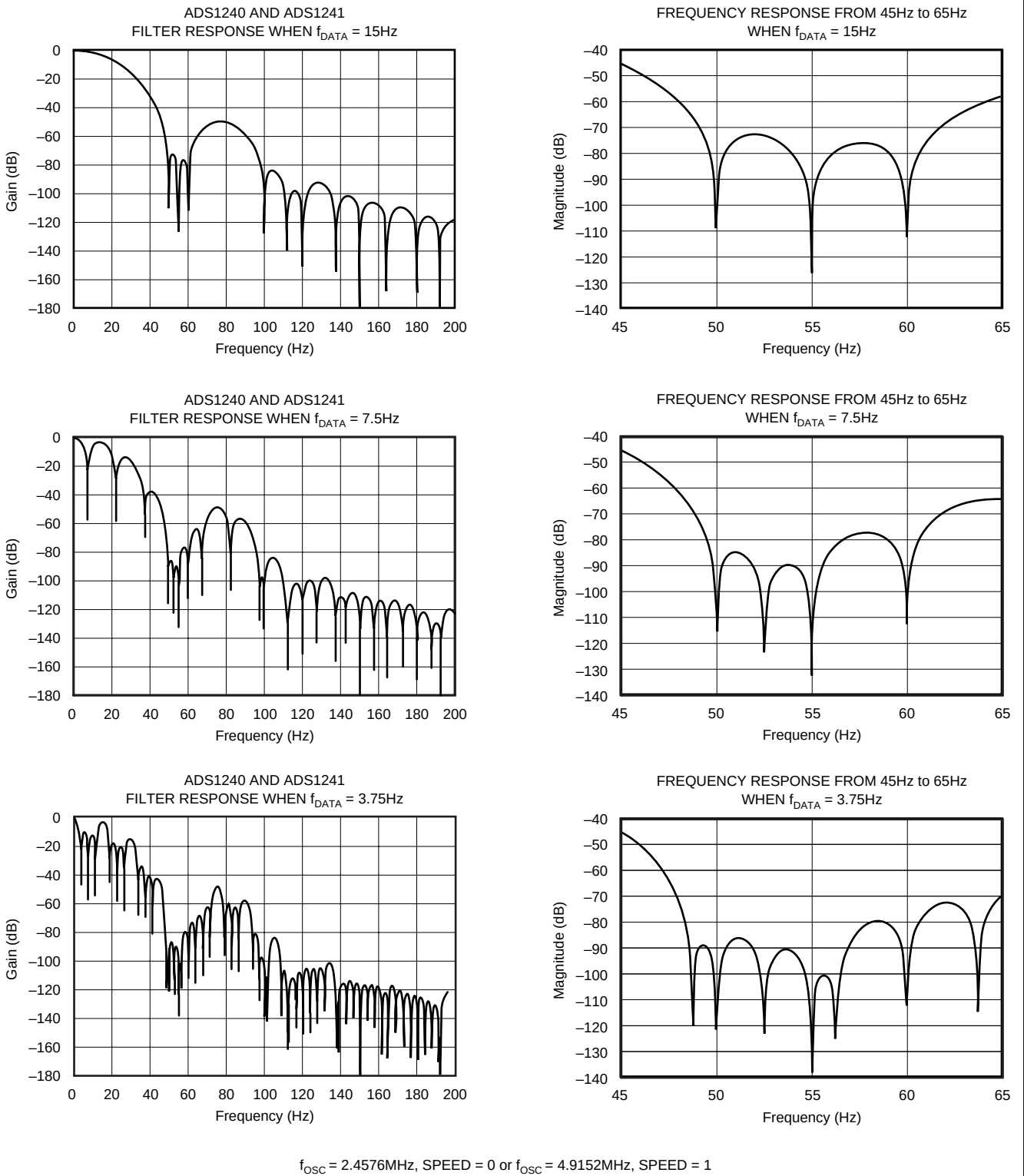
$$1.5 \cdot (50Hz \text{ and } 60Hz) = 75Hz \text{ and } 90Hz$$

## DATA I/O INTERFACE

The ADS1240 has four pins and the ADS1241 has eight pins that serve a dual purpose as both analog inputs and data I/O. These pins are powered from  $AV_{DD}$  and are configured through the IOCON, DIR, and DIO registers. These pins can be individually configured as either analog inputs or data I/O. See Figure 7 (page 14) for the equivalent schematic of an Analog/Data I/O pin.

The IOCON register defines the pin as either an analog input or data I/O. The power-up state is an analog input. If the pin is configured as an analog input in the IOCON register, the DIR and DIO registers have no effect on the state of the pin.

If the pin is configured as data I/O in the IOCON register, then DIR and DIO are used to control the state of the pin. The DIR register controls the direction of the data pin, either as an input or output. If the pin is configured as an input in the DIR register, then the corresponding DIO register bit reflects the state of the pin. Make sure the pin is driven to a logic one or zero when configured as an input to prevent



| DATA<br>OUTPUT RATE | -3dB<br>BANDWIDTH | ATTENUATION                           |                                       |                                     |                                     |
|---------------------|-------------------|---------------------------------------|---------------------------------------|-------------------------------------|-------------------------------------|
|                     |                   | $f_{\text{IN}} = 50 \pm 0.3\text{Hz}$ | $f_{\text{IN}} = 60 \pm 0.3\text{Hz}$ | $f_{\text{IN}} = 50 \pm 1\text{Hz}$ | $f_{\text{IN}} = 60 \pm 1\text{Hz}$ |
| 15Hz                | 14.6Hz            | -80.8dB                               | -87.3dB                               | -68.5dB                             | -76.1dB                             |
| 7.5Hz               | 3.44Hz            | -85.9dB                               | -87.4dB                               | -71.5dB                             | -76.2dB                             |
| 3.75Hz              | 1.65Hz            | -93.8dB                               | -88.6dB                               | -86.8dB                             | -77.3dB                             |

FIGURE 6. Filter Frequency Responses.

excess current dissipation. If the pin is configured as an output in the DIR register, then the corresponding DIO register bit value determines the state of the output pin (0 = AGND, 1 = AV<sub>DD</sub>).

It is still possible to perform A/D conversions on a pin configured as data I/O. This may be useful as a test mode, where the data I/O pin is driven and an A/D conversion is done on the pin.

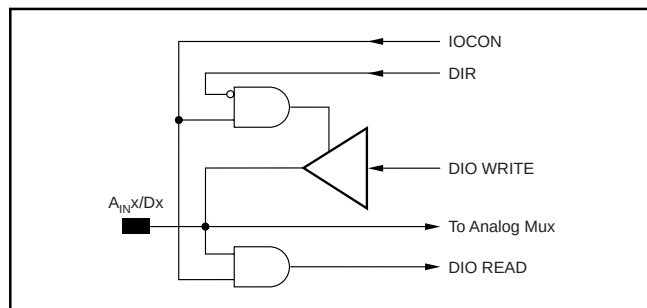


FIGURE 7. Analog/Data Interface Pin.

## SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) allows a controller to communicate synchronously with the ADS1240 and ADS1241. The ADS1240 and ADS1241 operate in slave-only mode. The serial interface is a standard four-wire SPI ( $\overline{CS}$ , SCLK, D<sub>IN</sub> and D<sub>OUT</sub>) interface that supports both serial clock polarities (POL pin).

### Chip Select ( $\overline{CS}$ )

The chip select ( $\overline{CS}$ ) input must be externally asserted before communicating with the ADS1240 or ADS1241.  $\overline{CS}$  must stay LOW for the duration of the communication. Whenever  $\overline{CS}$  goes HIGH, the serial interface is reset.  $\overline{CS}$  may be hard-wired LOW.

### Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock D<sub>IN</sub> and D<sub>OUT</sub> data. Make sure to have a clean SCLK to prevent accidental double-shifting of the data. If SCLK is not toggled within 3  $\overline{DRDY}$  pulses, the serial interface resets on the next SCLK pulse and starts a new communication cycle. A special pattern on SCLK resets the entire chip; see the RESET section for additional information.

### Clock Polarity (POL)

The clock polarity input (POL) controls the polarity of SCLK. When POL is LOW, data is clocked on the falling edge of SCLK and SCLK should be idled LOW. Likewise, when POL is HIGH, the data is clocked on the rising edge of SCLK and SCLK should be idled HIGH.

### Data Input (D<sub>IN</sub>) and Data Output (D<sub>OUT</sub>)

The data input (D<sub>IN</sub>) and data output (D<sub>OUT</sub>) receive and send data from the ADS1240 and ADS1241. D<sub>OUT</sub> is high impedance when not in use to allow D<sub>IN</sub> and D<sub>OUT</sub> to be connected together and driven by a bidirectional bus. Note: the Read Data Continuous Mode (RDATAC) command should not be

issued when D<sub>IN</sub> and D<sub>OUT</sub> are connected. While in RDATAC mode, D<sub>IN</sub> looks for the STOPC or RESET command. If either of these 8-bit bytes appear on D<sub>OUT</sub> (which is connected to D<sub>IN</sub>), the RDATAC mode ends.

## DATA READY $\overline{DRDY}$ PIN

The  $\overline{DRDY}$  line is used as a status signal to indicate when data is ready to be read from the internal data register.  $\overline{DRDY}$  goes LOW when a new data word is available in the DOR register. It is reset HIGH when a read operation from the data register is complete. It also goes HIGH prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

The status of  $\overline{DRDY}$  can also be obtained by interrogating bit 7 of the ACR register (address 2<sub>H</sub>). The serial interface can operate in 3-wire mode by tying the  $\overline{CS}$  input LOW. In this case, the SCLK, D<sub>IN</sub>, and D<sub>OUT</sub> lines are used to communicate with the ADS1240 and ADS1241. This scheme is suitable for interfacing to microcontrollers. If  $\overline{CS}$  is required as a decoding signal, it can be generated from a port bit of the microcontroller.

## DSYNC OPERATION

Synchronization can be achieved either through the  $\overline{DSYNC}$  pin or the DSYNC command. When the  $\overline{DSYNC}$  pin is used, the digital circuitry is reset on the falling edge of  $\overline{DSYNC}$ . While  $\overline{DSYNC}$  is LOW, the serial interface is deactivated. Reset is released when  $\overline{DSYNC}$  is taken HIGH. Synchronization occurs on the next rising edge of the system clock after  $\overline{DSYNC}$  is taken HIGH.

When the DSYNC command is sent, the digital filter is reset on the edge of the last SCLK of the DSYNC command. The modulator is held in RESET until the next edge of SCLK is detected. Synchronization occurs on the next rising edge of the system clock after the first SCLK following the DSYNC command.

## POWER-UP—SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry was designed to accommodate digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically.

## RESET

The user can reset the registers to their default values in three different ways: by asserting the RESET pin; by issuing the RESET command; or by applying a special waveform on the SCLK (the *SCLK Reset Waveform*, as shown in the Timing Diagram). Note: if both POL and SCLK pins are held high, applying the SCLK Reset Waveform to the  $\overline{CS}$  pin also resets the part.

## APPLICATION EXAMPLES

# ADS1240 AND ADS1241 REGISTER

The operation of the device is set up through individual registers. Collectively, the registers contain all the informa-

tion needed to configure the part, such as data format, multiplexer settings, calibration settings, data rate, etc. The set of the 16 registers are shown in Table III.

| ADDRESS         | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3     | BIT 2 | BIT 1 | BIT 0 |
|-----------------|----------|-------|-------|-------|-------|-----------|-------|-------|-------|
| 00 <sub>H</sub> | SETUP    | ID    | ID    | ID    | ID    | BOCS      | PGA2  | PGA1  | PGA0  |
| 01 <sub>H</sub> | MUX      | PSEL3 | PSEL2 | PSEL1 | PSEL0 | NSEL3     | NSEL2 | NSEL1 | NSEL0 |
| 02 <sub>H</sub> | ACR      | DRDY  | U/B   | SPEED | BUFEN | BIT ORDER | RANGE | DR1   | DR0   |
| 03 <sub>H</sub> | ODAC     | SIGN  | OSET6 | OSET5 | OSET4 | OSET3     | OSET2 | OSET1 | OSET0 |
| 04 <sub>H</sub> | DIO      | DIO_7 | DIO_6 | DIO_5 | DIO_4 | DIO_3     | DIO_2 | DIO_1 | DIO_0 |
| 05 <sub>H</sub> | DIR      | DIR_7 | DIR_6 | DIR_5 | DIR_4 | DIR_3     | DIR_2 | DIR_1 | DIR_0 |
| 06 <sub>H</sub> | IOCON    | IO7   | IO6   | IO5   | IO4   | IO3       | IO2   | IO1   | IO0   |
| 07 <sub>H</sub> | OCR0     | OCR07 | OCR06 | OCR05 | OCR04 | OCR03     | OCR02 | OCR01 | OCR00 |
| 08 <sub>H</sub> | OCR1     | OCR15 | OCR14 | OCR13 | OCR12 | OCR11     | OCR10 | OCR09 | OCR08 |
| 09 <sub>H</sub> | OCR2     | OCR23 | OCR22 | OCR21 | OCR20 | OCR19     | OCR18 | OCR17 | OCR16 |
| 0A <sub>H</sub> | FSR0     | FSR07 | FSR06 | FSR05 | FSR04 | FSR03     | FSR02 | FSR01 | FSR00 |
| 0B <sub>H</sub> | FSR1     | FSR15 | FSR14 | FSR13 | FSR12 | FSR11     | FSR10 | FSR09 | FSR08 |
| 0C <sub>H</sub> | FSR2     | FSR23 | FSR22 | FSR21 | FSR20 | FSR19     | FSR18 | FSR17 | FSR16 |
| 0D <sub>H</sub> | DOR2     | DOR23 | DOR22 | DOR21 | DOR20 | DOR19     | DOR18 | DOR17 | DOR16 |
| 0E <sub>H</sub> | DOR1     | DOR15 | DOR14 | DOR13 | DOR12 | DOR11     | DOR10 | DOR09 | DOR08 |
| 0F <sub>H</sub> | DOR0     | DOR07 | DOR06 | DOR05 | DOR04 | DOR03     | DOR02 | DOR01 | DOR00 |

TABLE III. Registers.

## DETAILED REGISTER DEFINITIONS

### SETUP (Address 00<sub>H</sub>) Setup Register

Reset Value = iii0000

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ID    | ID    | ID    | ID    | BOCS  | PGA2  | PGA1  | PGA0  |

bit 7-4 Factory Programmed Bits

bit 3 BOCS: Burnout Current Source  
0 = Disabled (default)  
1 = Enabled

bit 2-0 PGA2: PGA1: PGA0: Programmable Gain Amplifier Gain Selection  
000 = 1 (default)  
001 = 2  
010 = 4  
011 = 8  
100 = 16  
101 = 32  
110 = 64  
111 = 128

### MUX (Address 01<sub>H</sub>) Multiplexer Control Register

Reset Value = 01<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PSEL3 | PSEL2 | PSEL1 | PSEL0 | NSEL3 | NSEL2 | NSEL1 | NSEL0 |

bit 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select

0000 = A<sub>IN</sub>0 (default)

0001 = A<sub>IN</sub>1

0010 = A<sub>IN</sub>2

0011 = A<sub>IN</sub>3

0100 = A<sub>IN</sub>4

0101 = A<sub>IN</sub>5

0110 = A<sub>IN</sub>6

0111 = A<sub>IN</sub>7

1xxx = AINCOM (except when xxx = 111)

1111 = Reserved

bit 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select

0000 = A<sub>IN</sub>0

0001 = A<sub>IN</sub>1 (default)

0010 = A<sub>IN</sub>2

0011 = A<sub>IN</sub>3

0100 = A<sub>IN</sub>4

0101 = A<sub>IN</sub>5

0110 = A<sub>IN</sub>6

0111 = A<sub>IN</sub>7

1xxx = AINCOM (except when xxx = 111)

1111 = Reserved



**ACR (Address 02<sub>H</sub>) Analog Control Register**Reset Value = X0<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3     | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-----------|-------|-------|-------|
| DRDY  | U/B   | SPEED | BUFEN | BIT ORDER | RANGE | DR1   | DR0   |

bit 7 **DRDY: Data Ready (Read Only)**  
This bit duplicates the state of the  $\overline{\text{DRDY}}$  pin.

bit 6 **U/B: Data Format**  
0 = Bipolar (default)  
1 = Unipolar

| U/B | ANALOG INPUT | DIGITAL OUTPUT (Hex) |
|-----|--------------|----------------------|
| 0   | +FSR         | 0x7FFFFFFF           |
|     | Zero         | 0x000000             |
|     | -FSR         | 0x800000             |
| 1   | +FSR         | 0xFFFFFFFF           |
|     | Zero         | 0x000000             |
|     | -FSR         | 0x000000             |

bit 5 **SPEED: Modulator Clock Speed**

0 =  $f_{\text{MOD}} = f_{\text{OSC}}/128$  (default)

1 =  $f_{\text{MOD}} = f_{\text{OSC}}/256$

bit 4 **BUFEN: Buffer Enable**  
0 = Buffer Disabled (default)  
1 = Buffer Enabled

bit 3 **BIT ORDER: Data Output Bit Order**  
0 = Most Significant Bit Transmitted First (default)  
1 = Least Significant Bit Transmitted First  
This configuration bit controls only the bit order within the byte of data that is shifted out. Data is always shifted out of the part most significant byte first. Data is always shifted into the part most significant bit first.

bit 2 **RANGE: Range Select**  
0 = Full-Scale Input Range equal to  $\pm V_{\text{REF}}$  (default).  
1 = Full-Scale Input Range equal to  $\pm 1/2 V_{\text{REF}}$   
NOTE: This allows reference voltages as high as  $AV_{\text{DD}}$ , but even with a 5V reference voltage the calibration must be performed with this bit set to 0.

bit 1-0 **DR1: DR0: Data Rate**  
( $f_{\text{OSC}} = 2.4576\text{MHz}$ , SPEED = 0)  
00 = 15Hz (default)  
01 = 7.5Hz  
10 = 3.75Hz  
11 = Reserved

**ODAC (Address 03 ) Offset DAC**Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SIGN  | OSET6 | OSET5 | OSET4 | OSET3 | OSET2 | OSET1 | OSET0 |

bit 7 **Sign**  
0 = Positive  
1 = Negative

$$\text{Offset} = \frac{V_{\text{REF}}}{2 \bullet \text{PGA}} \bullet \left( \frac{\text{OSET}[6:0]}{127} \right) \quad \text{RANGE} = 0$$

$$\text{Offset} = \frac{V_{\text{REF}}}{4 \bullet \text{PGA}} \bullet \left( \frac{\text{OSET}[6:0]}{127} \right) \quad \text{RANGE} = 1$$

NOTE: The offset DAC must be enabled after calibration or the calibration nullifies the effects.

**DIO (Address 04<sub>H</sub>) Data I/O**Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DIO 7 | DIO 6 | DIO 5 | DIO 4 | DIO 3 | DIO 2 | DIO 1 | DIO 0 |

If the IOCON register is configured for data, a value written to this register appears on the data I/O pins if the pin is configured as an output in the DIR register. Reading this register returns the value of the data I/O pins.

Bit 4 to bit 7 is not used in ADS1240.

**DIR (Address 05<sub>H</sub>) Direction Control for Data I/O**Reset Value = FF<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DIR7  | DIR6  | DIR5  | DIR4  | DIR3  | DIR2  | DIR1  | DIR0  |

Each bit controls whether the corresponding data I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

Bit 4 to bit 7 is not used in ADS1240.

**IOCON (Address 06<sub>H</sub>) I/O Configuration Register**Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IO7   | IO6   | IO5   | IO4   | IO3   | IO2   | IO1   | IO0   |

bit 7-0 **IO7: IO0: Data I/O Configuration**  
0 = Analog (default)  
1 = Data

Configuring the pin as a data I/O pin allows it to be controlled through the DIO and DIR registers.

Bit 4 to bit 7 is not used in ADS1240.

**OCR0 (Address 07<sub>H</sub>) Offset Calibration Coefficient**

(Least Significant Byte)

Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OCR07 | OCR06 | OCR05 | OCR04 | OCR03 | OCR02 | OCR01 | OCR00 |



**OCR1** (Address 08<sub>H</sub>) Offset Calibration Coefficient  
(Middle Byte)

Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OCR15 | OCR14 | OCR13 | OCR12 | OCR11 | OCR10 | OCR09 | OCR08 |

**OCR2** (Address 09<sub>H</sub>) Offset Calibration Coefficient  
(Most Significant Byte)

Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OCR23 | OCR22 | OCR21 | OCR20 | OCR19 | OCR18 | OCR17 | OCR16 |

**FSR0** (Address 0A<sub>H</sub>) Full-Scale Register  
(Least Significant Byte)

Reset Value = 59<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| FSR07 | FSR06 | FSR05 | FSR04 | FSR03 | FSR02 | FSR01 | FSR00 |

**FSR1** (Address 0B<sub>H</sub>) Full-Scale Register  
(Middle Byte)

Reset Value = 55<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| FSR15 | FSR14 | FSR13 | FSR12 | FSR11 | FSR10 | FSR09 | FSR08 |

**FSR2** (Address 0C<sub>H</sub>) Full-Scale Register  
(Most Significant Byte)

Reset Value = 55<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| FSR23 | FSR22 | FSR21 | FSR20 | FSR19 | FSR18 | FSR17 | FSR16 |

**DOR2** (Address 0D<sub>H</sub>) Data Output Register  
(Most Significant Byte) (Read Only)

Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DOR23 | DOR22 | DOR21 | DOR20 | DOR19 | DOR18 | DOR17 | DOR16 |

**DOR1** (Address 0E<sub>H</sub>) Data Output Register  
(Middle Byte) (Read Only)

Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DOR15 | DOR14 | DOR13 | DOR12 | DOR11 | DOR10 | DOR09 | DOR08 |

**DOR0** (Address 0F<sub>H</sub>) Data Output Register  
(Least Significant Byte) (Read Only)

Reset Value = 00<sub>H</sub>

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DOR07 | DOR06 | DOR05 | DOR04 | DOR03 | DOR02 | DOR01 | DOR00 |

# ADS1240 AND ADS1241 CONTROL COMMAND DEFINITIONS

The commands listed in Table IV control the operations of the ADS1240 and ADS1241. Some of the commands are stand-alone commands (e.g., RESET) while others require additional bytes (e.g., WREG requires the count and data bytes).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

| COMMANDS  | DESCRIPTION                   | OP CODE                      | 2 <sup>nd</sup> COMMAND BYTE |
|-----------|-------------------------------|------------------------------|------------------------------|
| RDATA     | Read Data                     | 0000 0001 (01 <sub>H</sub> ) | —                            |
| RDATA C   | Read Data Continuously        | 0000 0011 (03 <sub>H</sub> ) | —                            |
| STOPC     | Stop Read Data Continuously   | 0000 1111 (0F <sub>H</sub> ) | —                            |
| RREG      | Read from REG “rrrr”          | 0001 rrrr (1x <sub>H</sub> ) | xxxx_nnnn (# of regs-1)      |
| WREG      | Write to REG “rrrr”           | 0101 rrrr (5x <sub>H</sub> ) | xxxx_nnnn (# of regs-1)      |
| SELF CAL  | Offset and Gain Self Cal      | 1111 0000 (F0 <sub>H</sub> ) | —                            |
| SELF OCAL | Self Offset Cal               | 1111 0001 (F1 <sub>H</sub> ) | —                            |
| SELF GCAL | Self Gain Cal                 | 1111 0010 (F2 <sub>H</sub> ) | —                            |
| SYSOCAL   | Sys Offset Cal                | 1111 0011 (F3 <sub>H</sub> ) | —                            |
| SYS GCAL  | Sys Gain Cal                  | 1111 0100 (F4 <sub>H</sub> ) | —                            |
| WAKEUP    | Wakeup from SLEEP Mode        | 1111 1011 (FB <sub>H</sub> ) | —                            |
| DSYNC     | Sync $\overline{\text{DRDY}}$ | 1111 1100 (FC <sub>H</sub> ) | —                            |
| SLEEP     | Put in SLEEP Mode             | 1111 1101 (FD <sub>H</sub> ) | —                            |
| RESET     | Reset to Power-Up Values      | 1111 1110 (FE <sub>H</sub> ) | —                            |

NOTE: The received data format is always MSB First; the data out format is set by the BIT ORDER bit in the ACR register.

TABLE IV. Command Summary.

## RDATA–Read Data

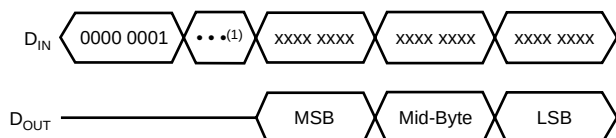
**Description:** Read the most recent conversion result from the Data Output Register (DOR). This is a 24-bit value.

**Operands:** None

**Bytes:** 1

**Encoding:** 0000 0001

**Data Transfer Sequence:**



NOTE: (1) For wait time, refer to timing specification.

## RDATA C–Read Data Continuous

**Description:** Read Data Continuous mode enables the continuous output of new data on each  $\overline{\text{DRDY}}$ . This command eliminates the need to send the Read Data Command on each  $\overline{\text{DRDY}}$ . This mode may be terminated by either the STOPC command or the RESET command. Wait at least 10 f<sub>OSC</sub> after  $\overline{\text{DRDY}}$  falls before reading.

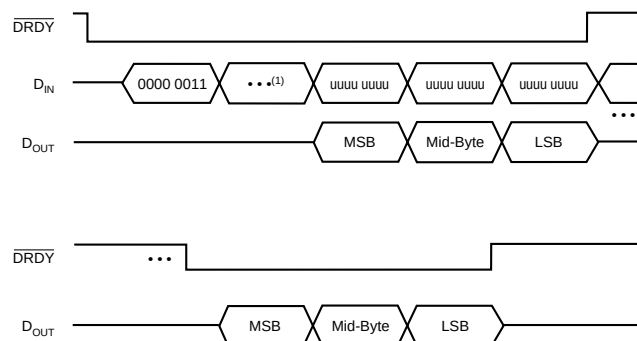
**Operands:** None

**Bytes:** 1

**Encoding:** 0000 0011

**Data Transfer Sequence:**

Command terminated when “uuuu uuuu” equals STOPC or RESET.



NOTE: (1) For wait time, refer to timing specification.

## STOPC–Stop Continuous

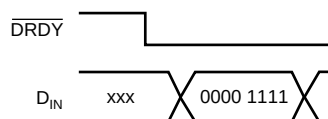
**Description:** Ends the continuous data output mode. Issue after  $\overline{\text{DRDY}}$  goes LOW.

**Operands:** None

**Bytes:** 1

**Encoding:** 0000 1111

**Data Transfer Sequence:**



## RREG–Read from Registers

**Description:** Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte count. If the count exceeds the remaining registers, the addresses wrap back to the beginning.

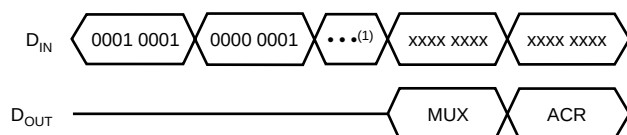
**Operands:** r, n

**Bytes:** 2

**Encoding:** 0001 rrrr xxxx nnnn

**Data Transfer Sequence:**

Read Two Registers Starting from Register 01<sub>H</sub> (MUX)



NOTE: (1) For wait time, refer to timing specification.

## WREG–Write to Registers

**Description:** Write to the registers starting with the register address specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

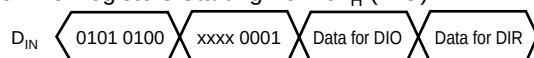
**Operands:** r, n

**Bytes:** 2

**Encoding:** 0101 rrrr xxxx nnnn

**Data Transfer Sequence:**

Write Two Registers Starting from 04<sub>H</sub> (DIO)



## SELFAL–Offset and Gain Self Calibration

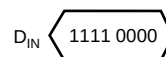
**Description:** Starts the process of self calibration. The Offset Calibration Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 0000

**Data Transfer Sequence:**



## SELFOCAL–Offset Self Calibration

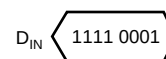
**Description:** Starts the process of self-calibration for offset. The Offset Calibration Register (OCR) is updated after this operation.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 0001

**Data Transfer Sequence:**



## SELFGCAL–Gain Self Calibration

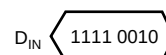
**Description:** Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 0010

**Data Transfer Sequence:**



## SYSOCAL–System Offset Calibration

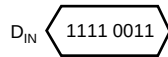
**Description:** Initiates a system offset calibration. The input should be set to 0V, and the ADS1240 and ADS1241 compute the OCR value that compensates for offset errors. The Offset Calibration Register (OCR) is updated after this operation. The user must apply a zero input signal to the appropriate analog inputs. The OCR register is automatically updated afterwards.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 0011

**Data Transfer Sequence:**



## SYSGCAL–System Gain Calibration

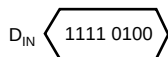
**Description:** Starts the system gain calibration process. For a system gain calibration, the input should be set to the reference voltage and the ADS1240 and ADS1241 compute the FSR value that will compensate for gain errors. The FSR is updated after this operation. To initiate a system gain calibration, the user must apply a full-scale input signal to the appropriate analog inputs. FCR register is updated automatically.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 0100

**Data Transfer Sequence:**



## WAKEUP

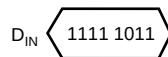
**Description:** Wakes the ADS1240 and ADS1241 from SLEEP mode.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 1011

**Data Transfer Sequence:**



## DSYNC–Sync $\overline{\text{DRDY}}$

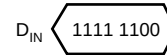
**Description:** Synchronizes the ADS1240 and ADS1241 to an external event.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 1100

**Data Transfer Sequence:**



## SLEEP–Sleep Mode

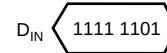
**Description:** Puts the ADS1240 and ADS1241 into a low power sleep mode. To exit sleep mode, issue the WAKEUP command.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 1101

**Data Transfer Sequence:**



## RESET–Reset to Default Values

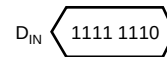
**Description:** Restore the registers to their power-up values. This command stops the Read Continuous mode.

**Operands:** None

**Bytes:** 1

**Encoding:** 1111 1110

**Data Transfer Sequence:**



## GENERAL-PURPOSE WEIGH SCALE

Figure 8 shows a typical schematic of a general-purpose weigh scale application using the ADS1240. In this example, the internal PGA is set to either 64 or 128 (depending on the maximum output voltage of the load cell) so that the load cell output can be directly applied to the differential inputs of ADS1240.

weigh scale application using the ADS1240. The front-end differential amplifier helps maximize the dynamic range.

## DEFINITION OF TERMS

An attempt has been made to be consistent with the termi-

## HIGH PRECISION WEIGH SCALE

Figure 9 shows the typical schematic of a high-precision

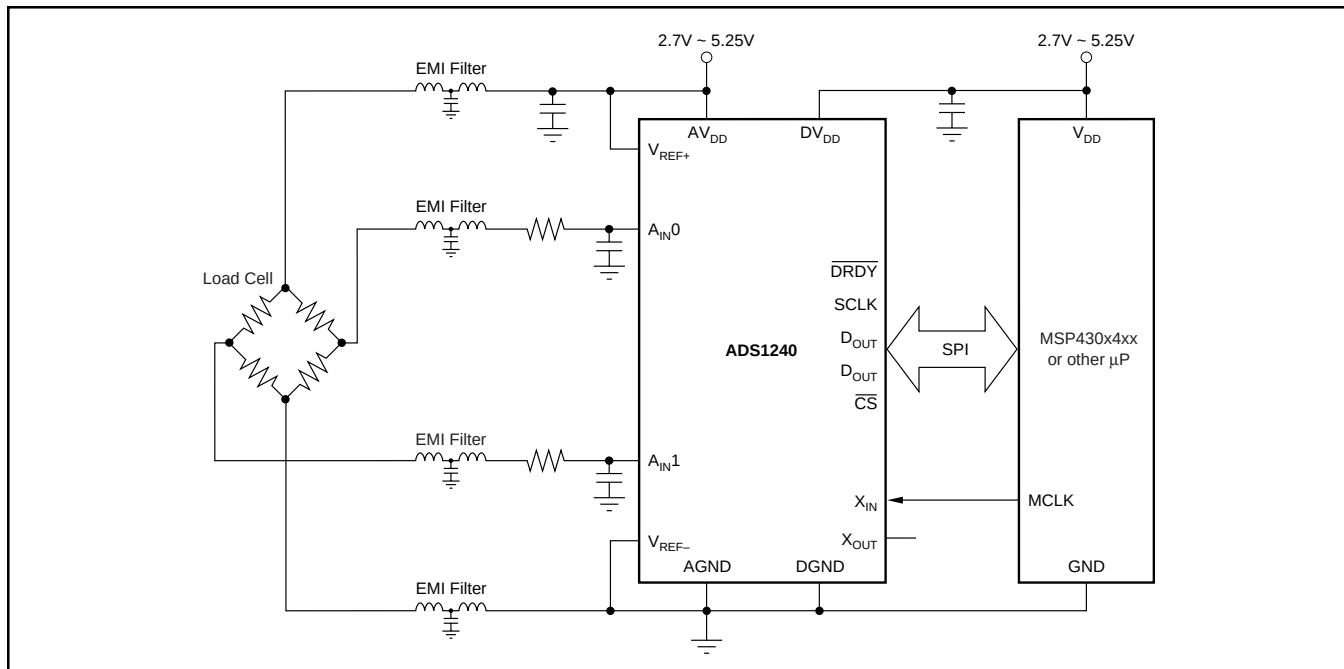


FIGURE 8. Schematic of a General-Purpose Weigh Scale.

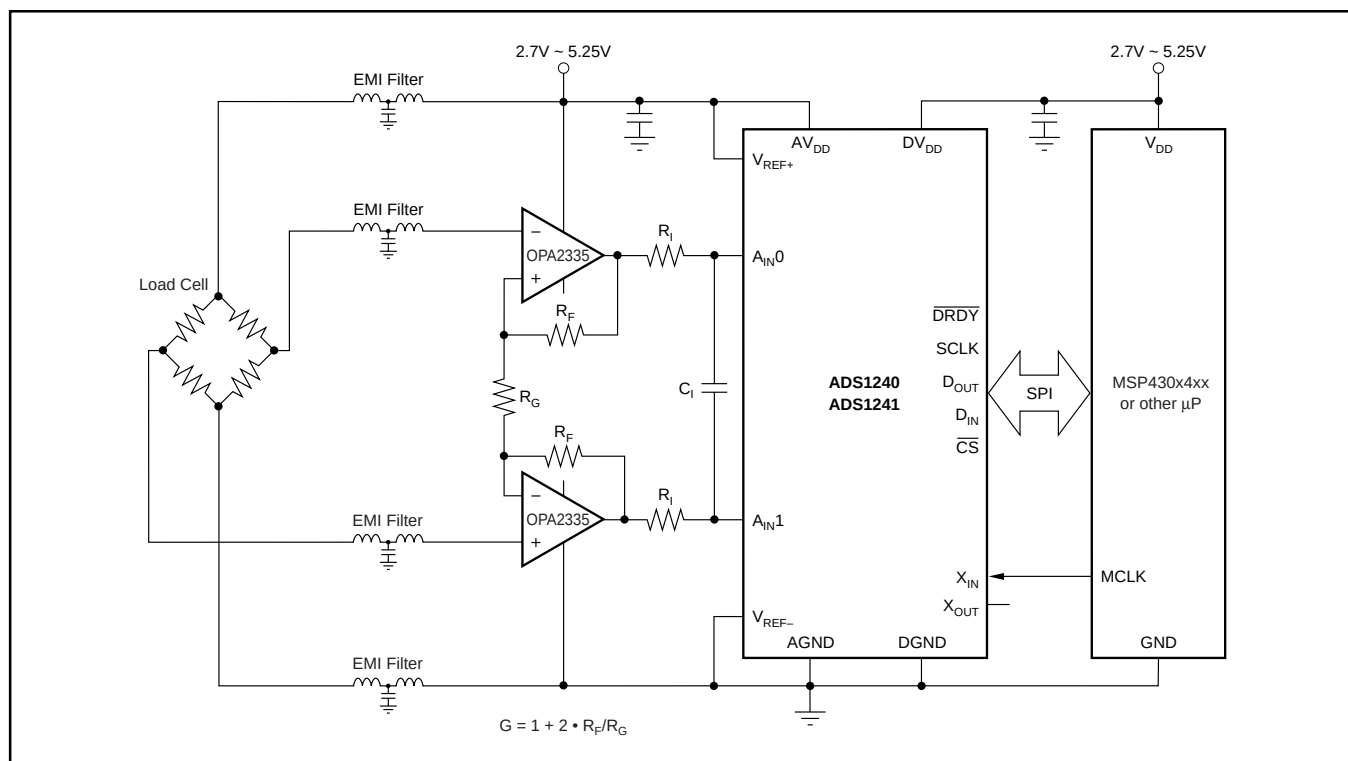


FIGURE 9. Block Diagram for a High-Precision Weigh Scale.

nology used in this data sheet. In that regard, the definition of each term is given as follows:

**Analog Input Voltage**—the voltage at any one analog input relative to AGND.

**Analog Input Differential Voltage**—given by the following equation: (IN+) – (IN–). Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is –2.5V. In each case, the actual input voltages must remain within the AGND to AV<sub>DD</sub> range.

**Conversion Cycle**—the term *conversion cycle* usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t<sub>DATA</sub> time period.

**Data Rate**—The rate at which conversions are completed. See definition for f<sub>DATA</sub>.

$$f_{\text{DATA}} = \frac{f_{\text{OSC}}}{128 \cdot 2^{\text{SPEED}} \cdot 1280 \cdot 2^{\text{DR}}}$$

SPEED = 0, 1  
DR = 0, 1, 2

f<sub>OSC</sub>—the frequency of the crystal oscillator or CMOS compatible input signal at the X<sub>IN</sub> input of the ADS1240 and ADS1241.

f<sub>MOD</sub>—the frequency or speed at which the modulator of the ADS1240 and ADS1241 is running. This depends on the SPEED bit as given by the following equation:

$$f_{\text{MOD}} = \frac{f_{\text{OSC}}}{\text{mfactor}} = \frac{f_{\text{OSC}}}{128 \cdot 2^{\text{SPEED}}}$$

f<sub>SAMP</sub>—the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

|         | SPEED = 0 | SPEED = 1 |
|---------|-----------|-----------|
| mfactor | 128       | 256       |

f<sub>DATA</sub>—the frequency of the digital output data produced by the ADS1240 and ADS1241, f<sub>DATA</sub> is also referred to as the Data Rate.

| PGA SETTING | SAMPLING FREQUENCY                                                |
|-------------|-------------------------------------------------------------------|
| 1, 2, 4, 8  | $f_{\text{SAMP}} = \frac{f_{\text{OSC}}}{\text{mfactor}}$         |
| 16          | $f_{\text{SAMP}} = \frac{f_{\text{OSC}} \cdot 2}{\text{mfactor}}$ |
| 32          | $f_{\text{SAMP}} = \frac{f_{\text{OSC}} \cdot 4}{\text{mfactor}}$ |
| 64, 128     | $f_{\text{SAMP}} = \frac{f_{\text{OSC}} \cdot 8}{\text{mfactor}}$ |

**Full-Scale Range (FSR)**—as with most A/D converters, the full-scale range of the ADS1240 and ADS1241 is defined as the input, that produces the positive full-scale digital output minus the input, that produces the negative full-scale digital output.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: [1.25V (positive full-scale) minus –1.25V (negative full-scale)] = 2.5V.

**Least Significant Bit (LSB) Weight**—this is the theoretical amount of voltage that the differential voltage at the analog input has to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full-Scale Range}}{2^N - 1}$$

where N is the number of bits in the digital output.

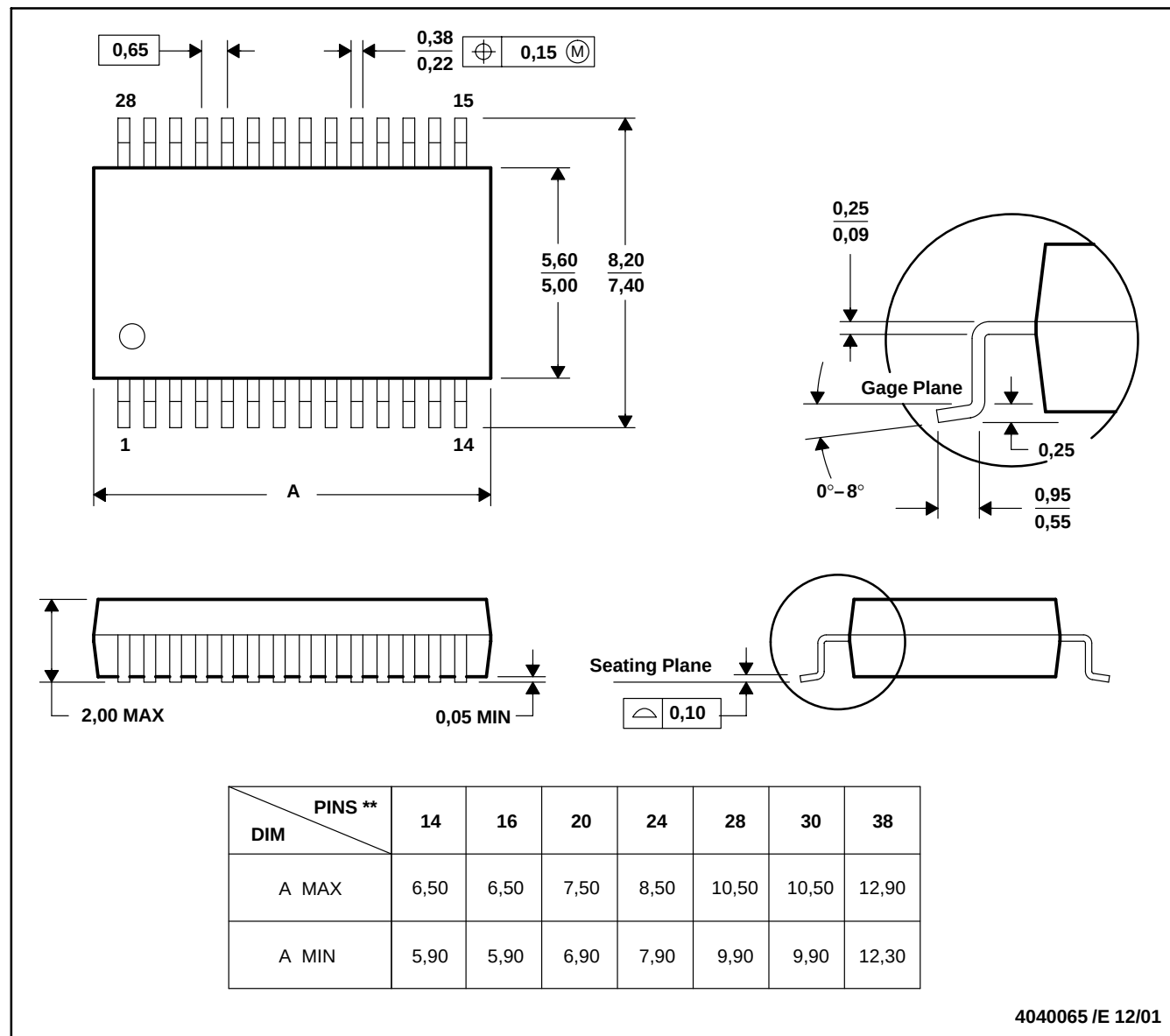
t<sub>DATA</sub>—the inverse of f<sub>DATA</sub>, or the period between each data output.

| 5V SUPPLY ANALOG INPUT <sup>(1)</sup> |                  |                                            |                  | GENERAL EQUATIONS                           |                                                 |                                                 |
|---------------------------------------|------------------|--------------------------------------------|------------------|---------------------------------------------|-------------------------------------------------|-------------------------------------------------|
| GAIN SETTING                          | FULL-SCALE RANGE | DIFFERENTIAL INPUT VOLTAGES <sup>(2)</sup> | PGA OFFSET RANGE | FULL-SCALE RANGE                            | DIFFERENTIAL INPUT VOLTAGES <sup>(2)</sup>      | PGA SHIFT RANGE                                 |
| 1                                     | 5V               | ±2.5V                                      | ±1.25V           | $\frac{2 \cdot V_{\text{REF}}}{\text{PGA}}$ | $\frac{\pm V_{\text{REF}}}{\text{PGA}}$         | $\frac{\pm V_{\text{REF}}}{2 \cdot \text{PGA}}$ |
| 2                                     | 2.5V             | ±1.25V                                     | ±0.625V          |                                             |                                                 |                                                 |
| 4                                     | 1.25V            | ±0.625V                                    | ±312.5mV         |                                             |                                                 |                                                 |
| 8                                     | 0.625V           | ±312.5mV                                   | ±156.25mV        |                                             |                                                 |                                                 |
| 16                                    | 312.5mV          | ±156.25mV                                  | ±78.125mV        |                                             |                                                 |                                                 |
| 32                                    | 156.25mV         | ±78.125mV                                  | ±39.0625mV       | $\frac{V_{\text{REF}}}{\text{PGA}}$         | $\frac{\pm V_{\text{REF}}}{2 \cdot \text{PGA}}$ | $\frac{\pm V_{\text{REF}}}{4 \cdot \text{PGA}}$ |
| 64                                    | 78.125mV         | ±39.0625mV                                 | ±19.531mV        |                                             |                                                 |                                                 |
| 128                                   | 39.0625mV        | ±19.531mV                                  | ±9.766mV         |                                             |                                                 |                                                 |
|                                       |                  |                                            |                  |                                             |                                                 |                                                 |

NOTES: (1) With a 2.5V reference. (2) Refer to electrical specification for analog input voltage range.

TABLE VI. Full-Scale Range versus PGA Setting.

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-150

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| <b>Products</b>  |                                                                    | <b>Applications</b> |                                                                          |
|------------------|--------------------------------------------------------------------|---------------------|--------------------------------------------------------------------------|
| Amplifiers       | <a href="http://amplifier.ti.com">amplifier.ti.com</a>             | Audio               | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                   |
| Data Converters  | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     | Automotive          | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| DSP              | <a href="http://dsp.ti.com">dsp.ti.com</a>                         | Broadband           | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
| Interface        | <a href="http://interface.ti.com">interface.ti.com</a>             | Digital Control     | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Logic            | <a href="http://logic.ti.com">logic.ti.com</a>                     | Military            | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Power Mgmt       | <a href="http://power.ti.com">power.ti.com</a>                     | Optical Networking  | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Microcontrollers | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> | Security            | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
|                  |                                                                    | Telephony           | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
|                  |                                                                    | Video & Imaging     | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
|                  |                                                                    | Wireless            | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated