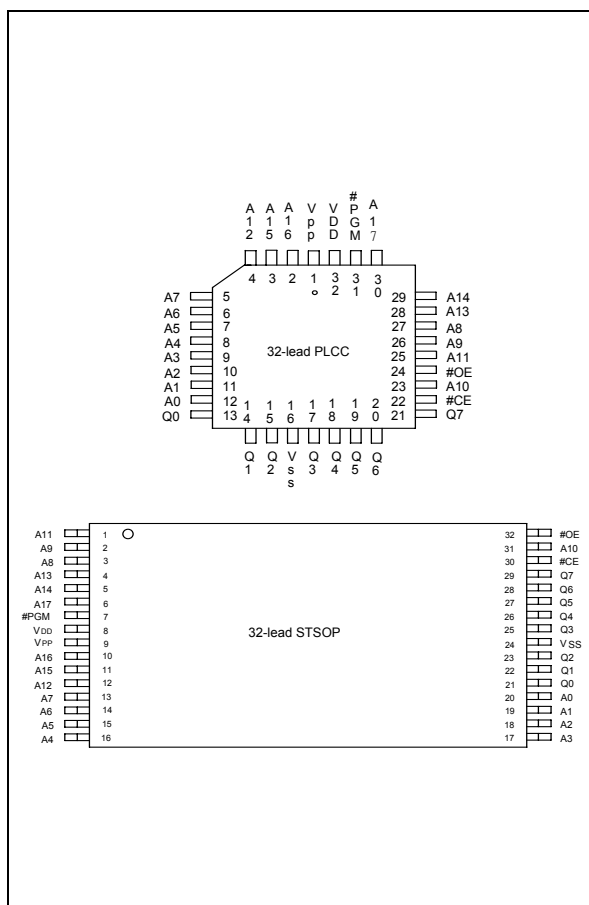


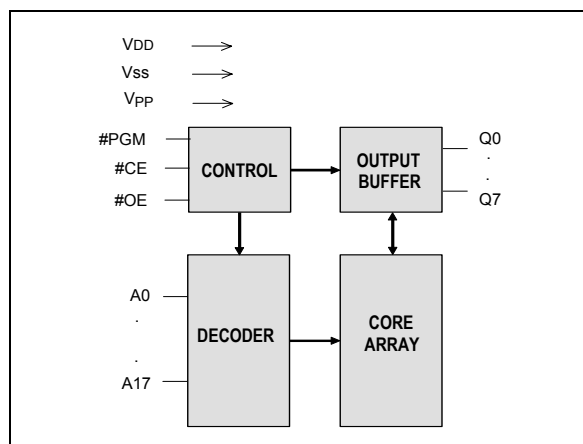
1. GENERAL DESCRIPTION

2. FEATURES

- ### 3. PIN CONFIGURATIONS



4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYMBOL	DESCRIPTION
A1 – A17	Address Inputs
Q0 – Q7	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#PGM	Program Enable
VPP	Program/Erase Supply Voltage
VDD	Power Supply
Vss	Ground
NC	No Connection



6. FUNCTIONAL DESCRIPTION

Read Mode

Like conventional UVEPROMs, the W27L02 has two control functions and both of these produce data at the outputs.

#CE is for power control and chip select. #OE controls the output buffer to gate data to the output pins. When addresses are stable, the address access time (TACC) is equal to the delay from #CE to output (TCE), and data are available at the outputs TOE after the falling edge of #OE, if TACC and TCE timings are met.

Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27L02 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

There are two ways to enter Erase mode. One is to raise VPP to VPE (12V), VDD = VCE (5V), #CE low, #OE high, A9 = VHH (12V), and all other address pins are kept at fixed low or high. Pulsing #PGM low starts the erase operation. The other way is somewhat like flash, by programming two consecutive commands into the device and then enter Erase mode. The two commands are loading Data = AA(hex) to Addr. = 5555(hex) and Data = 10(hex) to Addr. = 2AAA(hex). Be careful to note that the #PGM pulse widths of these two commands are different: One is 100 μ S, while the other is 100 mS. Please refer to the Smart Erase Algorithm 1 & 2.

Erase Verify Mode

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to "1" or not. The erase verify mode automatically ensures a substantial erase margin. This mode will be entered after the erase operation if VDD = VPE (5V), #CE low, and #OE low, #PGM high.

Program Mode

Programming is performed exactly as it is in conventional UVEPROMs, and programming is the only way to change cell data from "1" to "0." The program mode is entered when VPP is raised to VPP (12V), VDD = VCP (5V), #CE low, #OE high, the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing #PGM low starts the programming operation.

Program Verify Mode

All of the bytes in the chip must be verified to check whether they have been successfully programmed with the desired data or not. Hence, after each byte is programmed, a program verify operation should be performed. The program verify mode automatically ensures a substantial program margin. This mode will be entered after the program operation if VPP = VPP (12V), #CE low, #OE low, and #PGM high.

Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When #CE high, erasing or programming of non-target chips is inhibited, so that except for the #CE, the W27L02 may have common inputs.



Standby Mode

The standby mode significantly reduces V_{DD} current. This mode is entered when $\#CE$ high. In standby mode, all outputs are in a high impedance state, independent of $\#OE$ and $\#PGM$.

Two-line Output Control

Since EPROMs are often used in large memory arrays, the W27L02 provides two control inputs for multiple memory connections. Two-line control provides for lowest possible memory power dissipation and ensures that data bus contention will not occur.

System Considerations

EPROM power switching characteristics require careful device decoupling. System designers are concerned with three supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by the falling and rising edges of $\#CE$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a $0.1\ \mu\text{F}$ ceramic capacitor connected between its V_{DD} and V_{SS} . This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a $4.7\ \mu\text{F}$ electrolytic capacitor should be placed at the array's power supply connection between V_{DD} and V_{SS} . The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

Table of Operating Modes

$V_{DD} = 3.3\text{V} \pm 10\%$, $V_{pp} = V_{pe} = V_{HH} = 12\text{V}$, $V_{CP} = V_{PE} = V_{CE} = 5\text{V}$, $X = V_{IH}$ or V_{IL}

MODE	PINS								
	#CE	#OE	#PGM	A0	A9	OTER ADDR	VDD	VPP	OUTPUTS
Read	VIL	VIL	X	X	X	X	VDD	VDD	DOUT
Output Disable	VIL	VIH	X	X	X	X	VDD	VDD	High Z
Standby (TTL)	VIH	X	X	X	X	X	VDD	VDD	High Z
Standby (CMOS)	VDD ±0.3V	X	X	X	X	X	VDD	VDD	High Z
Program	VIL	VIH	VIL	X	X	X	VCP	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	X	VCP	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	X	VCP	VPP	High Z
Erase1	VIL	VIH	VIL	VIL	VPE		VCE	VPE	FF (Hex)
Erase2	VIL	VIH	VIL	First command: Addr. = 5555 (hex)			VCE	VCP	AA (Hex)
				Second command: Addr. = 2AAA (hex)			VCE	VCP	10 (Hex)
Erase Verify	VIL	VIL	VIH	X	X	X	VPE	VPP	DOUT
Erase Inhibit	VIH	X	X	X	X	X	VCE	VPE	High Z
Product Identifier - Manufacturer	VIL	VIL	X	VIL	VHH	X	VDD	VDD	DA (Hex)
Product Identifier - Device	VIL	VIL	X	VIH	VHH	X	VDD	VDD	85 (Hex)



8. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Operation Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
Voltage on all Pins with Respect to Ground Except VDD, VPP and A9 Pins	-0.5 to VDD +0.5	V
Voltage on VDD Pin with Respect to Ground	-0.5 to +7.0	V
Voltage on VPP Pin with Respect to Ground	-0.5 to +14.5	V
Voltage on A9 Pin with Respect to Ground	-0.5 to +14.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Capacitance

(VDD = 3.3V ±10%, TA = 25° C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	VIN = 0V	6	pF
Output Capacitance	COUT	VOUT = 0V	12	pF

Read Operation DC Characteristics

(VDD = 3.3V ±10%, TA = 0 to 70° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	ILI	VIN = 0V to VDD	-5	-	5	μA
Output Leakage Current	ILO	VOUT = 0V to VDD	-10	-	10	μA
Standby VDD Current (TTL input)	ISB	#CE = VIH	-	-	200	μA
Standby VDD Current (CMOS input)	ISB1	#CE = VDD ±0.2V	-	-	20	μA
VDD Operating Current	ICC	#CE = VIL, IOUT = 0 mA, f = 5 MHz	-	-	15	mA
VPP Operating Current	I PP	VPP = VDD	-	-	10	μA
Input Low Voltage	VIL	-	-0.3	-	0.6	V
Input High Voltage	VIH	-	2.0	-	VDD +0.5	V
Output Low Voltage	VOL	IOL = 1.6 mA	-	-	0.4	V
Output High Voltage	VOH	IOH = -0.1 mA	2.4	-	-	V
VPP Operating Voltage	VPP	-	VDD -0.7	-	VDD	V



Electrical Characteristics, continued

Program/Erase DC Characteristics

(TA = 25° C , VDD = 3.3V ±10%, VHH = 12V)

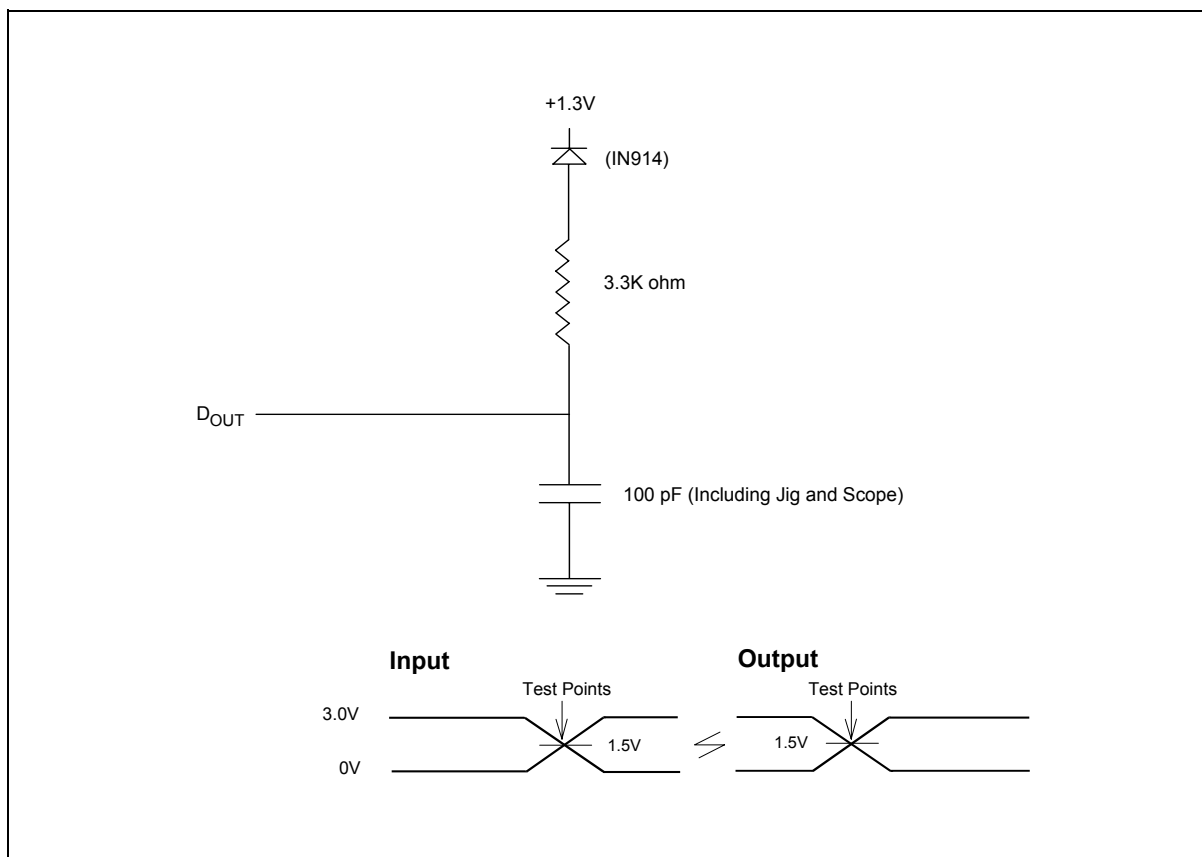
PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	ILI	VIN = VIL or VIH	-10	-	10	μA
VDD Program Current	ICP	#CE = VIL, #OE = VIH, #PGM = VIL	-	-	30	mA
VDD Erase Current	ICE	#CE = VIL, #OE = VIH, #PGM = VIL, A9 = VHH	-	-	30	mA
VPP Program Current	IPP	#CE = VIL, #OE = VIH, #PGM = VIL	-	-	30	mA
VPP Erase Current	IPE	#CE = VIL, #OE = VIH, #PGM = VIL, A9 = VHH	-	-	30	mA
Input Low Voltage	VIL	-	-0.3	-	0.8	V
Input High Voltage	VIH	-	2.4	-	5.5	V
Output Low Voltage (Verify)	VOL	IOL = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	VOH	IOH = -0.4 mA	2.4	-	-	V
A9 Silicon I.D. Voltage	VID	-	11.5	12.0	12.5	V
A9 Erase Voltage	VID	-	11.75	12.0	14.25	V
VPP Program Voltage	VPP	-	11.75	12.0	12.25	V
VPP Erase Voltage	VPE	-	11.75	12.0	14.25	V
VDD Supply Voltage (Program)	VCP	-	4.5	5.0	5.5	V
VDD Supply Voltage (Erase)	VCE	-	4.5	5.0	5.5	V
VDD Supply Voltage (Erase Verify)	VPE	-	-	5.0	-	V

Note: VDD must be applied simultaneously or before VPP and removed simultaneously or after VPP.

Electrical Characteristics, continued

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V/1.5V
Output Load	CL = 100 pF, IOH/IOL = -0.1 mA/1.6 mA for Read IOH/IOL = -0.4 mA/2.1 mA for Program/Erase

AC Test Load and Waveforms



Electrical Characteristics, continued

Read Operation AC Characteristics

(V_{DD} = 3.3V ±10%, T_A = 0 to 70° C)

PARAMETER	SYM.	W27L02-70		W27L02-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	70	-	90	-	nS
Chip Enable Access Time	TCE	-	70	-	90	nS
Address Access Time	TACC	-	70	-	90	nS
Output Enable Access Time	TOE	-	30	-	40	nS
#OE High to High-Z Output	TDF	-	25	-	25	nS
Output Hold from Address Change	TOH	0	-	0	-	nS

Note: V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC Programming/Erase Characteristics

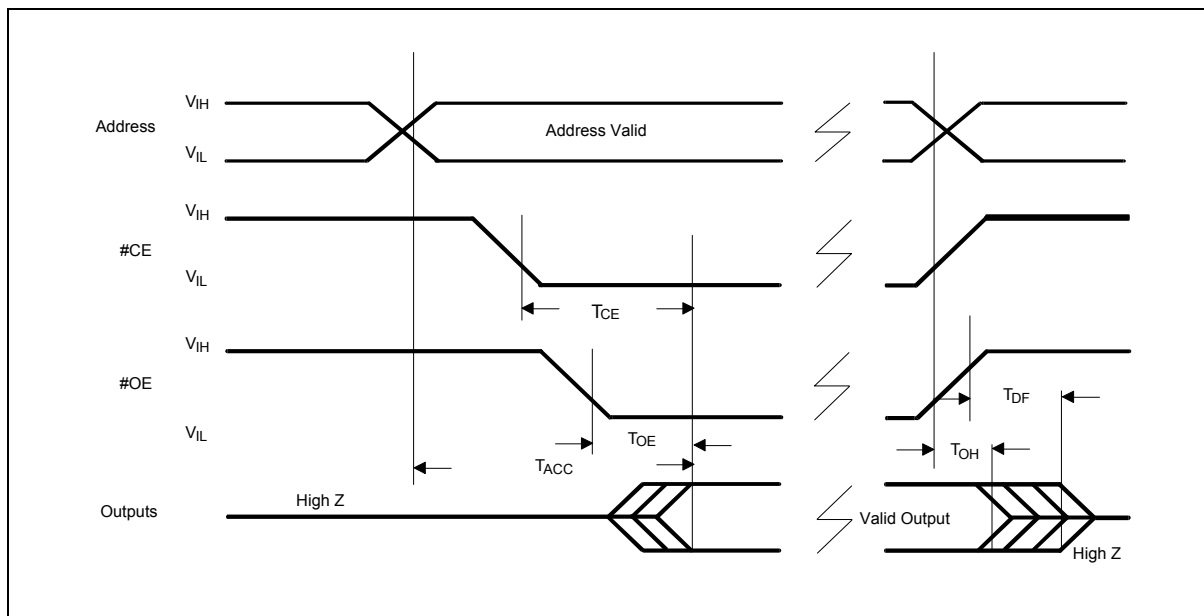
(V_{DD} = 3.3V ±10%, T_A = 25° C)

PARAMETER	SYM.	LIMITS			UNIT
		MIN.	TYP.	MAX.	
V _{PP} Setup Time	T _{VPS}	2.0	-	-	μS
Address Setup Time	T _{AS}	2.0	-	-	μS
Data Setup Time	T _{DS}	2.0	-	-	μS
#PGM Program Pulse Width	T _{PWP}	95	100	105	μS
#PGM Erase Pulse Width	T _{PWE}	95	100	105	mS
Data Hold Time	T _{DH}	2.0	-	-	μS
#OE Setup Time	T _{OES}	2.0	-	-	μS
Data Valid from #OE	T _{OEV}	-	-	150	nS
#OE High to Output High Z	T _{DFP}	0	-	130	nS
Address Hold Time after #PGM High	T _{AH}	0	-	-	μS
Address Hold Time (Erase)	T _{AHE}	2.0	-	-	μS
#CE Setup Time	T _{CES}	2.0	-	-	μS

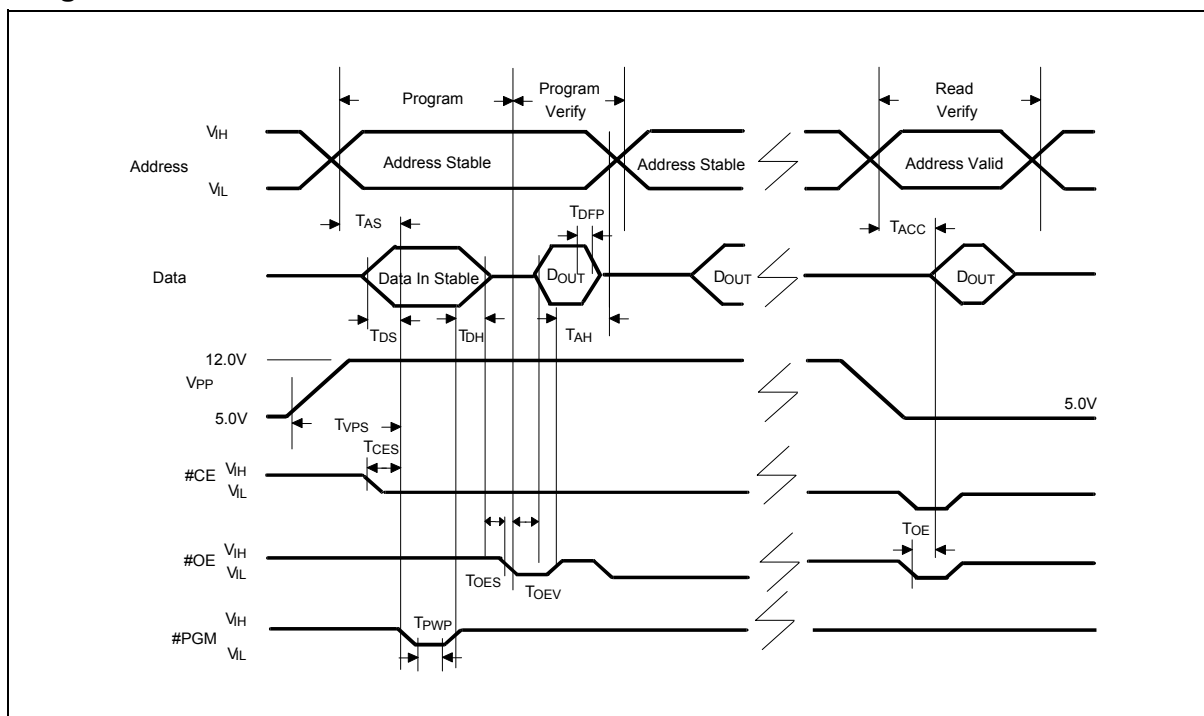
Note: V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

9. TIMING WAVEFORMS

AC Read Waveform

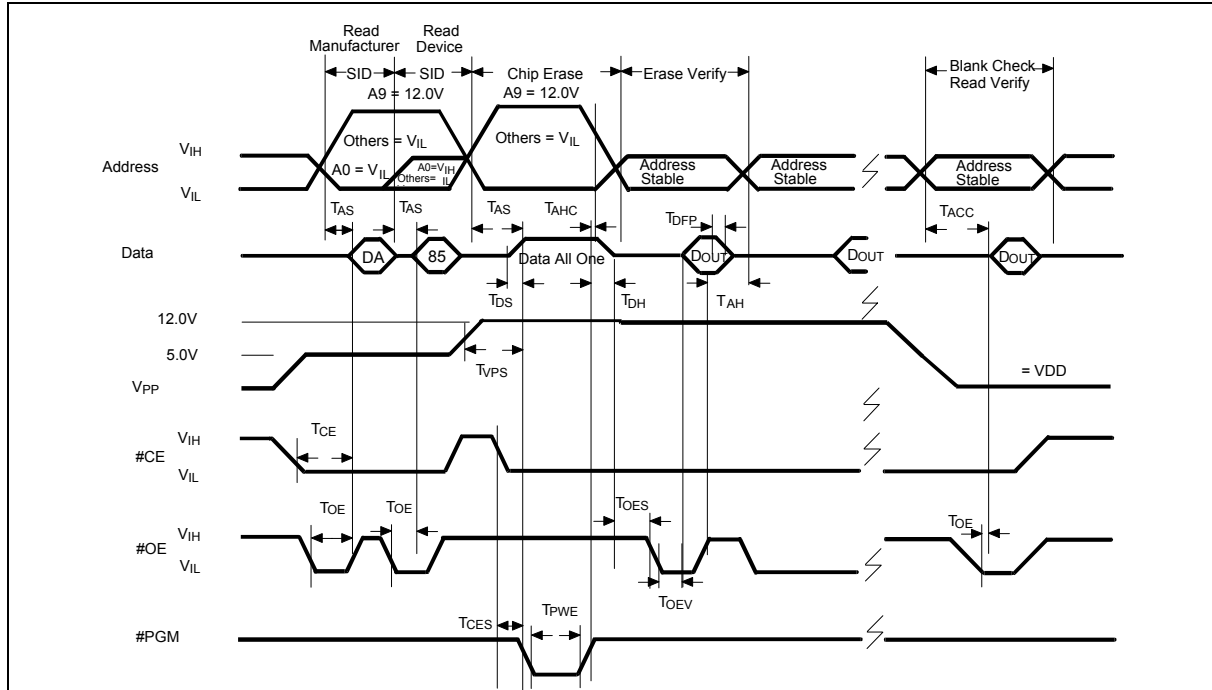


Program Waveform

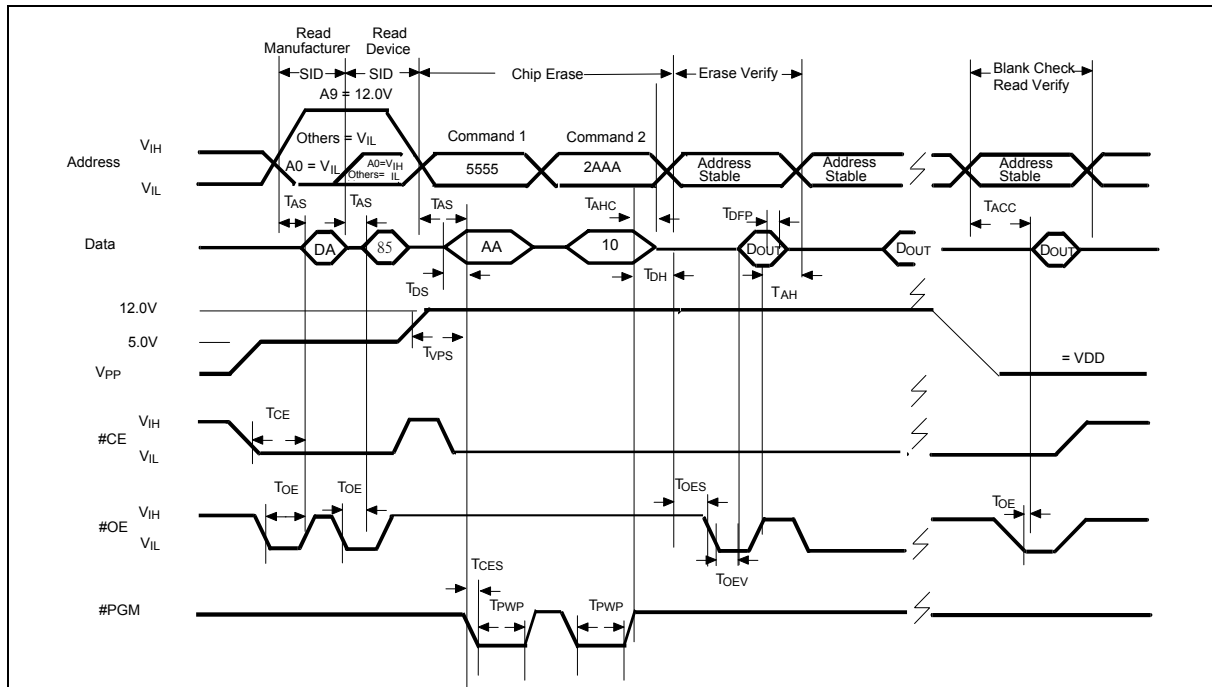


Timing Waveforms, Continued

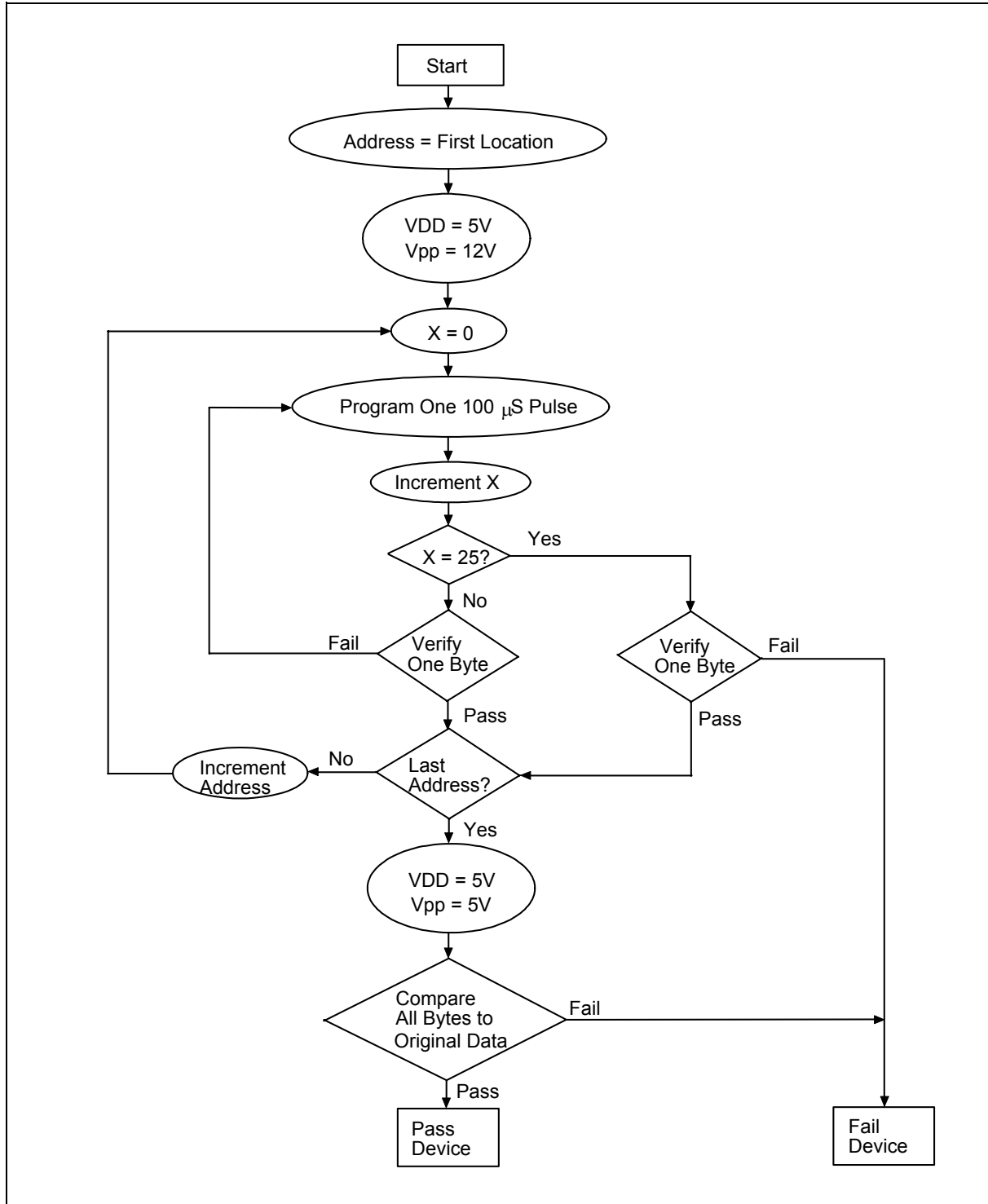
Erase Waveform 1

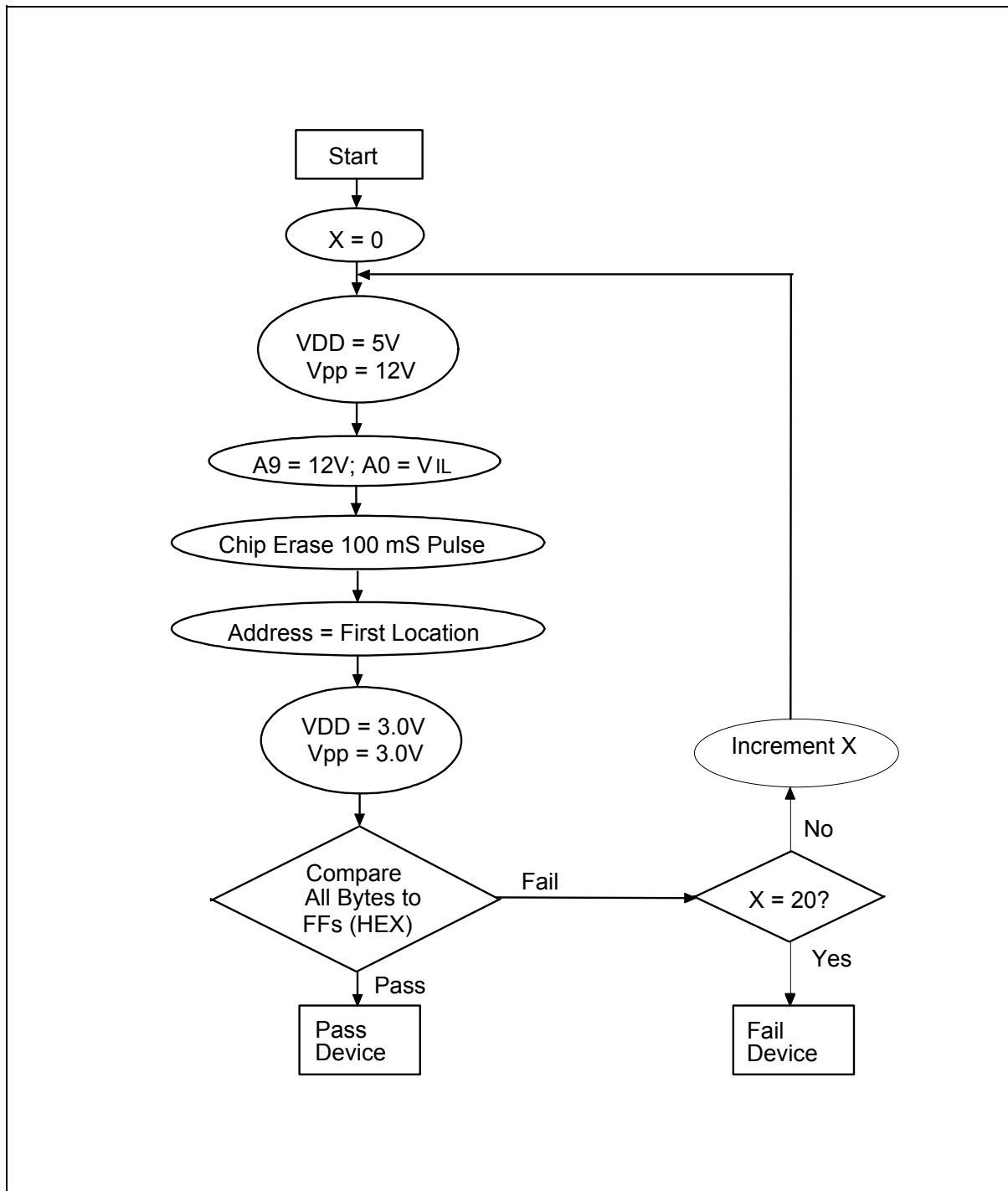


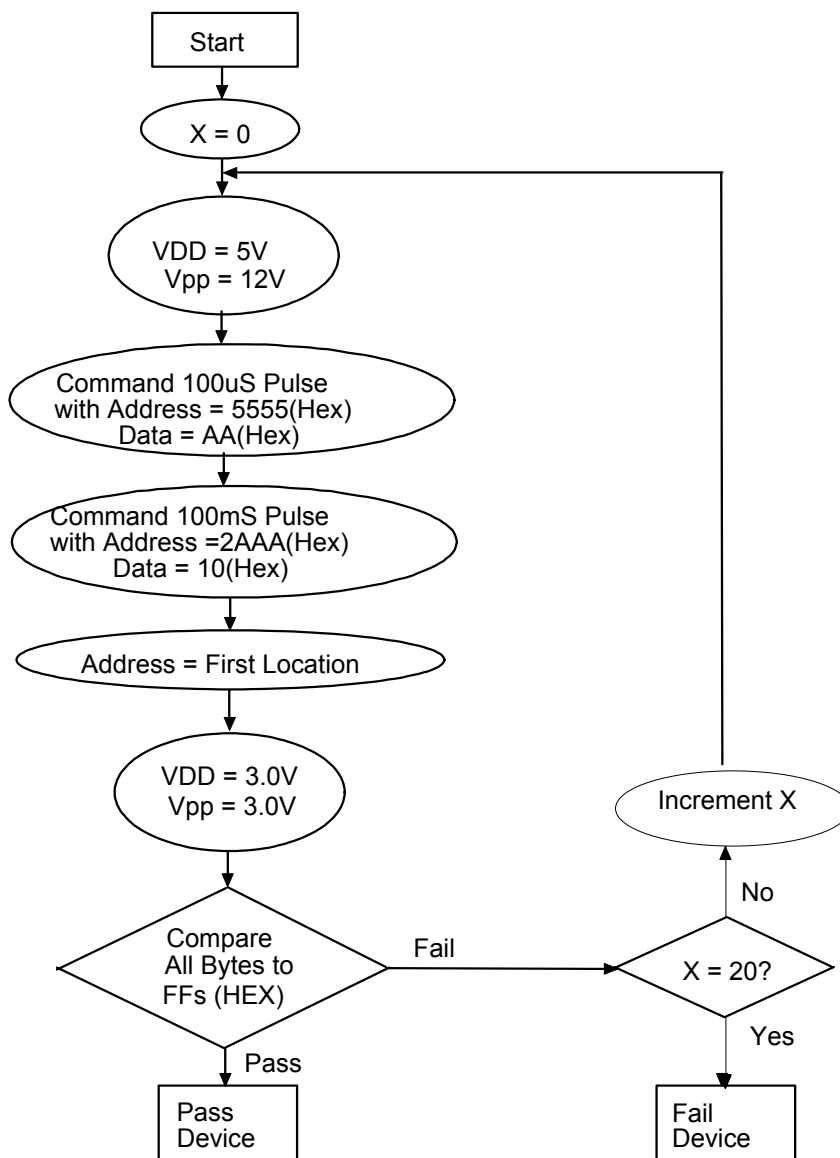
Erase Waveform 2



10. SMART PROGRAMMING ALGORITHM



11. SMART ERASE ALGORITHM 1

12. SMART ERASE ALGORITHM 2

**13. ORDERING INFORMATION**

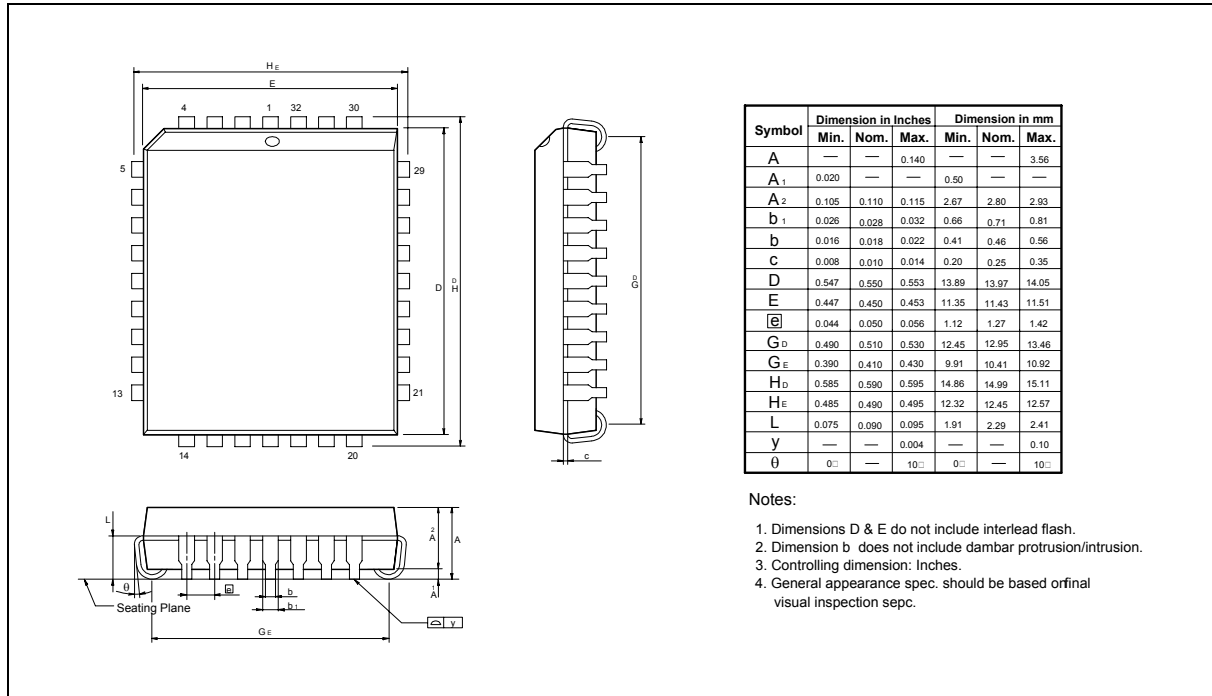
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (μA)	PACKAGE
W27L02P-70	70	15	20	32-Lead PLCC
W27L02P-90	90	15	20	32-Lead PLCC
W27L02Q-70	70	15	20	32-Lead STSOP
W27L02Q-90	90	15	20	32-Lead STSOP

Notes:

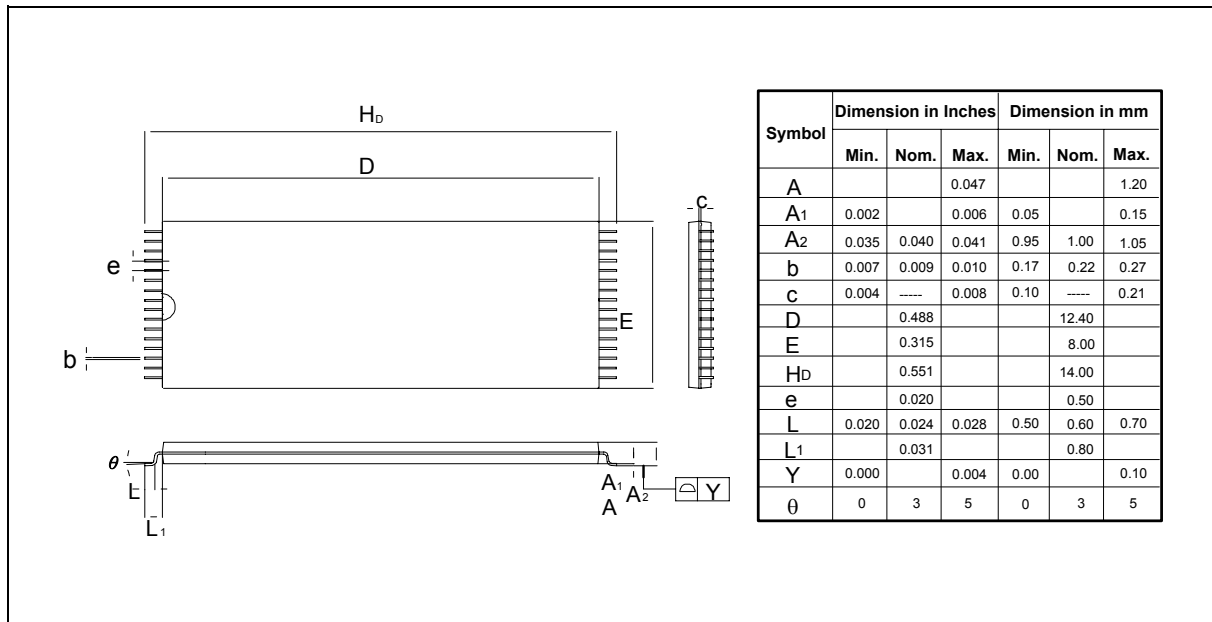
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14. PACKAGE DIMENSIONS

32-Lead PLCC



32-Lead STSOP (8 x 14 mm)





15. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 19, 2001	-	Initial Issue
A2	May 30, 2002	10	Modify Erase Waveform
		2, 3, 4, 6	Correct the V _{CV} (V _{PP}) as V _{PE} (V _{PP}) under Erase Inhibit Mode
		3	Modify the Pin of V _{PP} from V _{PE} to V _{PP} In the Erase Verify Mode
		All	Delete V _{DD} = 5.0V \pm 10%
A3	Feb. 20, 2003	1, 13, 14	Delete DIP package



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