

DM74LS174 • DM74LS175 Hex/Quad D-Type Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect at the output.

Features

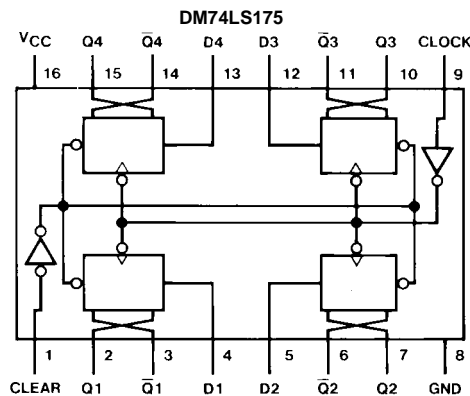
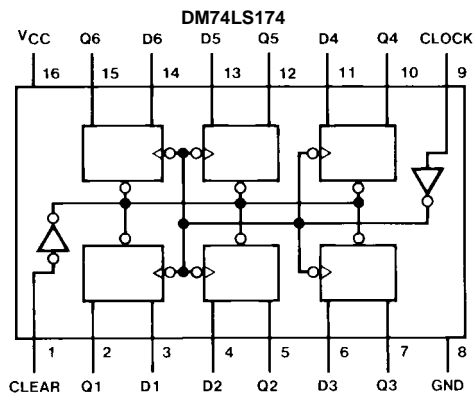
- DM74LS174 contains six flip-flops with single-rail outputs
- DM74LS175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
 - Buffer/storage registers
 - Shift registers
 - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 14 mW

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|-----------------------------------------------------------------------------|
| DM74LS174M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74LS174SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74LS174N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |
| DM74LS175M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74LS175SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74LS175N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



Function Table

(Each Flip-Flop)

| Inputs | | | Outputs | |
|--------|-------|---|---------|-------------|
| Clear | Clock | D | Q | \bar{Q} † |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | Q_0 | \bar{Q}_0 |

H = HIGH Level (steady state)

L = LOW Level (steady state)

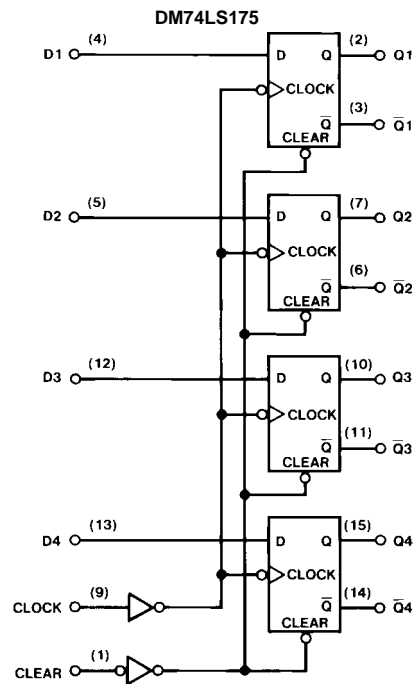
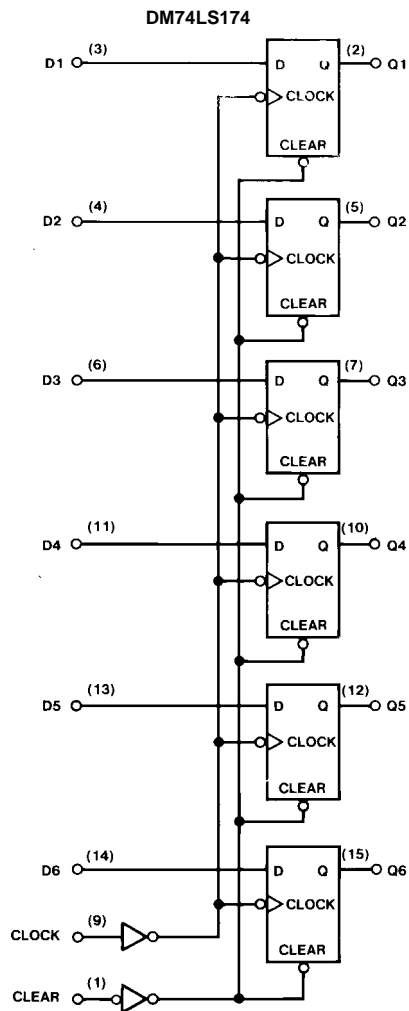
X = Don't Care

↑ = Transition from LOW-to-HIGH level

Q_0 = The level of Q before the indicated steady-state input conditions were established.

† = DM74LS175 only

Logic Diagrams



Absolute Maximum Ratings(Note 1)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | –65°C to +150°C |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS174 Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|-----------|--------------------------------|-------|-----|------|-------|
| V_{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} | HIGH Level Input Voltage | 2 | | | V |
| V_{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I_{OH} | HIGH Level Output Current | | | –0.4 | mA |
| I_{OL} | LOW Level Output Current | | | 8 | mA |
| f_{CLK} | Clock Frequency (Note 2) | 0 | | 30 | MHz |
| f_{CLK} | Clock Frequency (Note 3) | 0 | | 25 | MHz |
| t_W | Pulse Width (Note 4) | Clock | 20 | | ns |
| | | Clear | 20 | | |
| t_{SU} | Data Setup Time (Note 4) | 20 | | | ns |
| t_H | Data Hold Time (Note 4) | 0 | | | ns |
| t_{REL} | Clear Release Time (Note 4) | 25 | | | ns |
| T_A | Free Air Operating Temperature | 0 | | 70 | °C |

Note 2: $C_L = 15$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

Note 3: $C_L = 50$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

Note 4: $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

DM74LS174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 5) | Max | Units |
|----------|-----------------------------------|------------------------------------------------------------------------------------------------|-------|-----------------|-------|---------------|
| V_I | Input Clamp Voltage | $V_{CC} = \text{Min}$, $I_I = -18$ mA | | | –1.5 | V |
| V_{OH} | HIGH Level Output Voltage | $V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ | 2.7 | 3.4 | | V |
| V_{OL} | LOW Level Output Voltage | $V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ | | 0.35 | 0.5 | V |
| | | $I_{OL} = 4$ mA, $V_{CC} = \text{Min}$ | | 0.25 | 0.4 | |
| I_I | Input Current @ Max Input Voltage | $V_{CC} = \text{Max}$, $V_I = 7\text{V}$ | | | 0.1 | mA |
| I_{IH} | HIGH Level Input Current | $V_{CC} = \text{Max}$, $V_I = 2.7\text{V}$ | | | 20 | μA |
| I_{IL} | LOW Level Input Current | $V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$ | Clock | | –0.4 | mA |
| | | | Clear | | –0.4 | |
| | | | Data | | –0.36 | |
| I_{OS} | Short Circuit Output Current | $V_{CC} = \text{Max}$ (Note 6) | –20 | | –100 | mA |
| I_{CC} | Supply Current | $V_{CC} = \text{Max}$ (Note 7) | | 16 | 26 | mA |

Note 5: All typicals are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: With all outputs OPEN and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock.

DM74LS174 Switching Characteristicsat $V_{CC} = 5V$ and $T_A = 25^\circ C$

| Symbol | Parameter | From (Input) To (Output) | R _L = 2 kΩ | | | | Units |
|------------------|----------------------------------------------------|-----------------------------|------------------------|-----|------------------------|-----|-------|
| | | | C _L = 15 pF | | C _L = 50 pF | | |
| | | | Min | Max | Min | Max | |
| f _{MAX} | Maximum Clock Frequency | | 30 | | 25 | | MHz |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Clock to Output | | 30 | | 32 | ns |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clock to Output | | 30 | | 36 | ns |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Output | | 35 | | 42 | ns |

DM74LS175 Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|-----------|--------------------------------|-------|-----|------|-------|
| V_{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} | HIGH Level Input Voltage | 2 | | | V |
| V_{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I_{OH} | HIGH Level Output Current | | | -0.4 | mA |
| I_{OL} | LOW Level Output Current | | | 8 | mA |
| f_{CLK} | Clock Frequency (Note 8) | 0 | | 30 | MHz |
| f_{CLK} | Clock Frequency (Note 9) | 0 | | 25 | MHz |
| t_W | Pulse Width (Note 10) | Clock | 20 | | ns |
| | | Clear | 20 | | |
| t_{SU} | Data Setup Time (Note 10) | 20 | | | ns |
| t_H | Data Hold Time (Note 10) | 0 | | | ns |
| t_{REL} | Clear Release Time (Note 10) | 25 | | | ns |
| T_A | Free Air Operating Temperature | 0 | | 70 | °C |

Note 8: $C_L = 15$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5$ V.

Note 9: $C_L = 50$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5$ V.

Note 10: $T_A = 25^\circ\text{C}$ and $V_{CC} = 5$ V.

DM74LS175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 11) | Max | Units |
|----------|-----------------------------------|------------------------------------------------------------------------------------------------|-------|------------------|-------|---------------|
| V_I | Input Clamp Voltage | $V_{CC} = \text{Min}$, $I_I = -18$ mA | | | -1.5 | V |
| V_{OH} | HIGH Level Output Voltage | $V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ | 2.7 | 3.4 | | V |
| V_{OL} | LOW Level Output Voltage | $V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ | | 0.35 | 0.5 | V |
| | | $I_{OL} = 4$ mA, $V_{CC} = \text{Min}$ | | 0.25 | 0.4 | |
| I_I | Input Current @ Max Input Voltage | $V_{CC} = \text{Max}$, $V_I = 7$ V | | | 0.1 | mA |
| I_{IH} | HIGH Level Input Current | $V_{CC} = \text{Max}$, $V_I = 2.7$ V | | | 20 | μA |
| I_{IL} | LOW Level Input Current | $V_{CC} = \text{Max}$ $V_I = 0.4$ V | Clock | | -0.4 | mA |
| | | | Clear | | -0.4 | |
| | | | Data | | -0.36 | |
| I_{OS} | Short Circuit Output Current | $V_{CC} = \text{Max}$ (Note 12) | -20 | | -100 | mA |
| I_{CC} | Supply Current | $V_{CC} = \text{Max}$ (Note 13) | | 11 | 18 | mA |

Note 11: All typicals are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

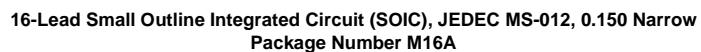
Note 12: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 13: With all outputs OPEN and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock input.

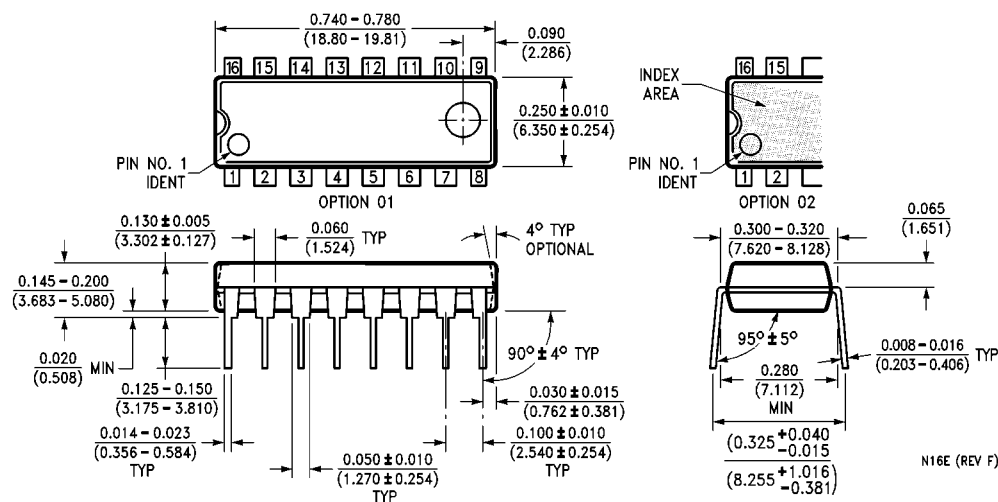
DM74LS175 Switching Characteristics

at $V_{CC} = 5$ V and $T_A = 25^\circ\text{C}$ (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | R _L = 2 kΩ | | | | Units |
|------------------|----------------------------------------------------|------------------------------|------------------------|-----|------------------------|-----|-------|
| | | | C _L = 15 pF | | C _L = 50 pF | | |
| | | | Min | Max | Min | Max | |
| f _{MAX} | Maximum Clock Frequency | | 30 | | 25 | | MHz |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Clock to Q or \overline{Q} | | 30 | | 32 | ns |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clock to Q or \overline{Q} | | 30 | | 36 | ns |
| t _{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | Clear to \overline{Q} | | 25 | | 29 | ns |
| t _{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Q | | 35 | | 42 | ns |



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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