

74VCX245

Low Voltage Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs

General Description

The VCX245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The T/R input determines the direction of data flow. The \overline{OE} input disables both the A and B ports by placing them in a high impedance state.

The 74VCX245 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74VCX245 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- Power-off high impedance inputs and outputs
- Supports Live Insertion and Withdrawal (Note 1)
- t_{PD}
3.5 ns max for 3.0V to 3.6V V_{CC}
- Static Drive (I_{OH}/I_{OL})
 ± 24 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
Human body model > 2000V
Machine model > 200V

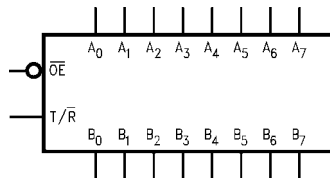
Note 1: To ensure the high impedance state during power up and power down, \overline{OE}_n should be tied to V_{CC} through a pull up resistor. The minimum value of the resistor is determined by the current sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCX245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VCX245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

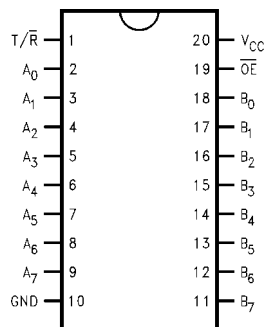
Logic Symbol



Pin Descriptions

Pin Names	Description
\overline{OE}	Output Enable Input (Active LOW)
T/R	Transmit/Receive Input
A ₀ –A ₇	Side A Inputs or 3-STATE Outputs
B ₀ –B ₇	Side B Inputs or 3-STATE Outputs

Connection Diagram



Truth Table

Inputs		Outputs
OE	T/R	
L	L	Bus B ₀ –B ₇ Data to Bus A ₀ –A ₇
L	H	Bus A ₀ –A ₇ Data to Bus B ₀ –B ₇
H	X	HIGH Z State on A ₀ –A ₇ , B ₀ –B ₇ (Note 2)

H = HIGH Voltage Level

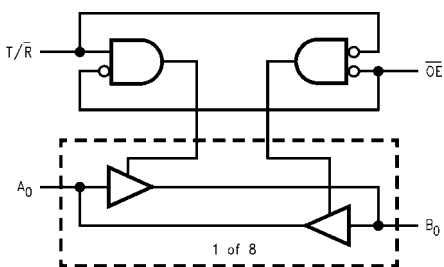
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Note 2: Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
DC Output Voltage (V_O)	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 4)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current	± 100 mA
Storage Temperature (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 5)

Power Supply	
Operating	1.4V to 3.6V
Input Voltage	-0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.3V$ to 2.7V	± 18 mA
$V_{CC} = 1.65V$ to 2.3V	± 6 mA
$V_{CC} = 1.4V$ to 1.6V	± 2 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6	2.0 1.6 $0.65 \times V_{CC}$ $0.65 \times V_{CC}$		V
V_{IL}	LOW Level Input Voltage		2.7-3.6 2.3-2.7 1.65-2.3 1.4 - 1.6		0.8 0.7 $0.35 \times V_{CC}$ $0.35 \times V_{CC}$	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12$ mA $I_{OH} = -18$ mA $I_{OH} = -24$ mA	2.7-3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA $I_{OH} = -12$ mA $I_{OH} = -18$ mA	2.3-2.7 2.3 2.3 2.3	$V_{CC} - 0.2$ 2.0 1.8 1.7		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA	1.65-2.3 1.65	$V_{CC} - 0.2$ 1.25		
		$I_{OH} = -100 \mu A$ $I_{OH} = -2$ mA	1.4 - 1.6 1.4	$V_{CC} - 0.2$ 1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{OL}	LOW Level Output Voltage	$I_{OL} = 100\ \mu\text{A}$ $I_{OL} = 12\ \text{mA}$ $I_{OL} = 18\ \text{mA}$ $I_{OL} = 24\ \text{mA}$	2.7–3.6 2.7 3.0 3.0		0.2 0.4 0.4 0.55	V
		$I_{OL} = 100\ \mu\text{A}$ $I_{OL} = 12\ \text{mA}$ $I_{OL} = 18\ \text{mA}$	2.3–2.7 2.3 2.3		0.2 0.4 0.6	
		$I_{OL} = 100\ \mu\text{A}$ $I_{OL} = 6\ \text{mA}$	1.65–2.3 1.65		0.2 0.3	
		$I_{OL} = 100\ \mu\text{A}$ $I_{OL} = 2\ \text{mA}$	1.4–1.6 1.4		0.2 0.35	
I _I	Input Leakage Current	$0 \leq V_I \leq 3.6\text{V}$	1.4–3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6\text{V}$ $V_I = V_{IH}$ or V_{IL}	1.4–3.6		±10	μA
I _{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6\text{V}$	0		10	μA
I _{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND $V_{CC} \leq (V_I, V_O) \leq 3.6\text{V}$ (Note 6)	1.4–3.6 1.4–3.6		20 ±20	μA
ΔI _{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6\text{V}$	2.7–3.6		750	μA

Note 6: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = –40°C to +85°C		Units	Figure Number
				Min	Max		
t _{PHL} , t _{PLH}	Propagation Delay A _n to B _n or B _n to A _n	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.5	ns	Figures 1, 2
			2.5 ± 0.2	0.8	4.2		
			1.8 ± 0.15	1.5	8.4		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	16.8		Figures 5, 6
t _{PZL} , t _{PZH}	Output Enable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	4.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	5.6		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 5, 7, 8
t _{PLZ} , t _{PHZ}	Output Disable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.6	3.6	ns	Figures 1, 3, 4
			2.5 ± 0.2	0.8	4.0		
			1.8 ± 0.15	1.5	7.2		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	14.4		Figures 5, 7, 8
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 8)	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1		1.5		

Note 7: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	0.3 0.7 1.0	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	-0.3 -0.7 -1.0	V
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8 2.5 3.3	1.3 1.7 2.0	V

Capacitance

Symbol	Parameter	Conditions	T _A = +25°C	Units
			Typical	
C _{IN}	Input Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	6	pF
C _{I/O}	Input/Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V	20	pF

AC Loading and Waveforms (V_{CC} 3.3V \pm 0.3V to 1.8V \pm 0.15V)

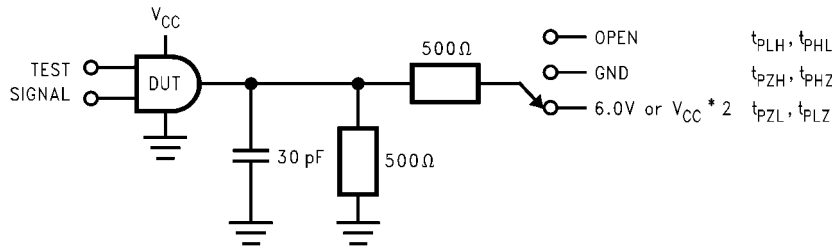


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5V \pm 0.2V$; $1.8V \pm 0.15V$
t_{PZH} , t_{PHZ}	GND

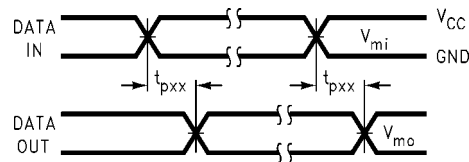


FIGURE 2. Waveform for Inverting and Non-inverting Functions

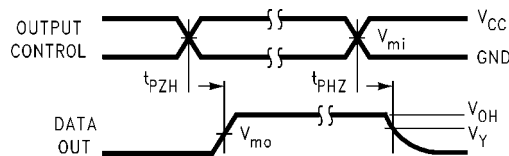


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

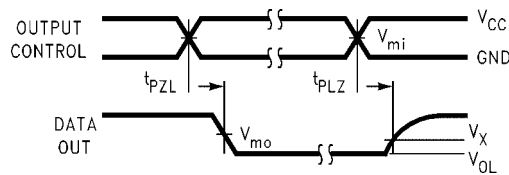
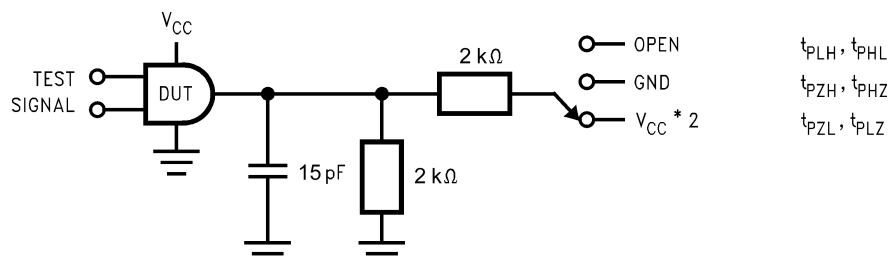


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	3.3V \pm 0.3V	2.5V \pm 0.2V	1.8V \pm 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ($V_{CC} 1.5 \pm 0.1V$)



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$V_{CC} \times 2$ at $V_{CC} = 1.5 \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

FIGURE 5. AC Test Circuit

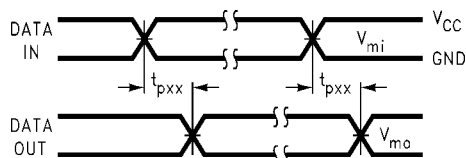


FIGURE 6. Waveform for Inverting and Non-Inverting Functions

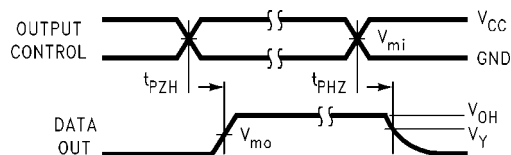


FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

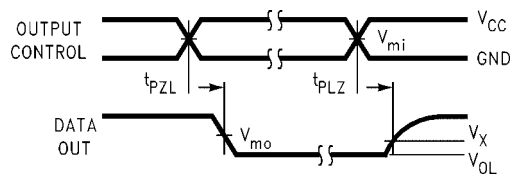
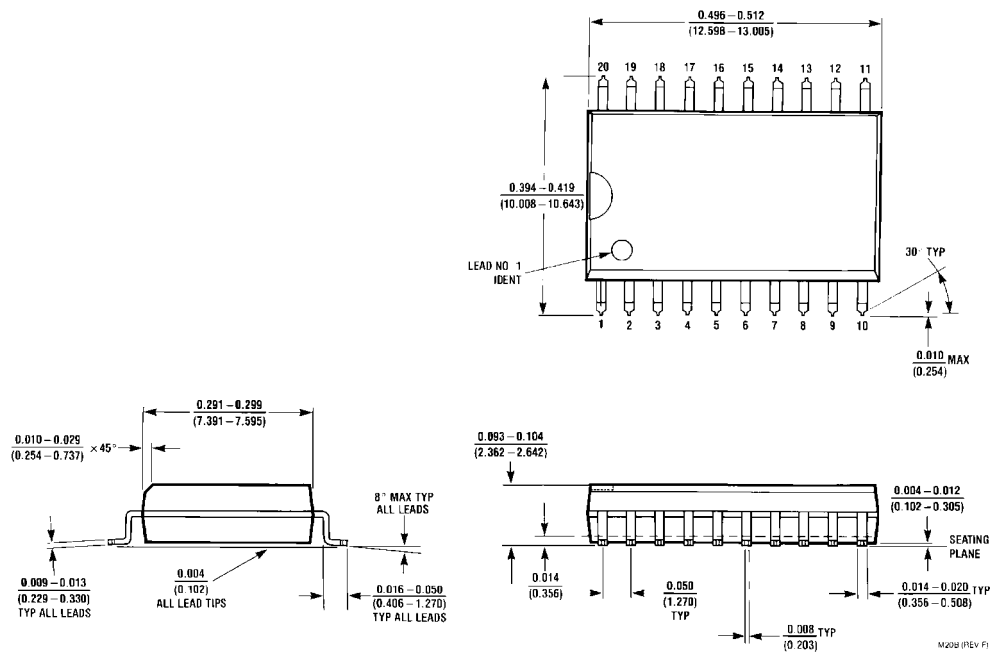


FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

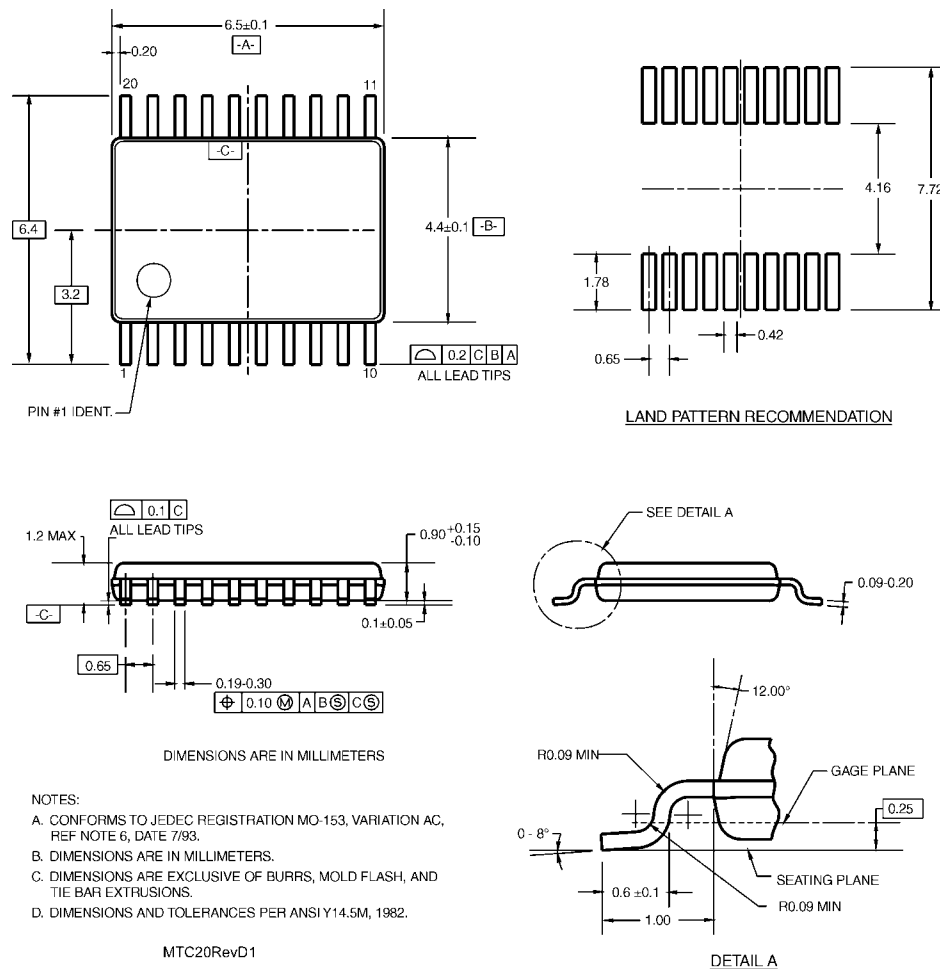
Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	$V_{OL} + 0.1V$
V_Y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com