



13-BIT TO 26-BIT REGISTERED *IDT74SSTVM16859* BUFFER WITH SSTL I/O ADVANCE INFORMATION

FEATURES:

- 1:2 register buffer
- Meets or exceeds JEDEC standard SSTVM16859
- 2.3V to 2.7V Operation
- SSTL_2 Class II style data inputs/outputs
- Differential CLK input
- $\overline{\text{RESET}}$ control compatible with LVC MOS levels
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in 56 pin MLF and 64 pin TSSOP packages

APPLICATIONS:

- Along with CSPT857C, Zero Delay PLL Clock buffer, provides complete solution for DDR1 registered DIMMs

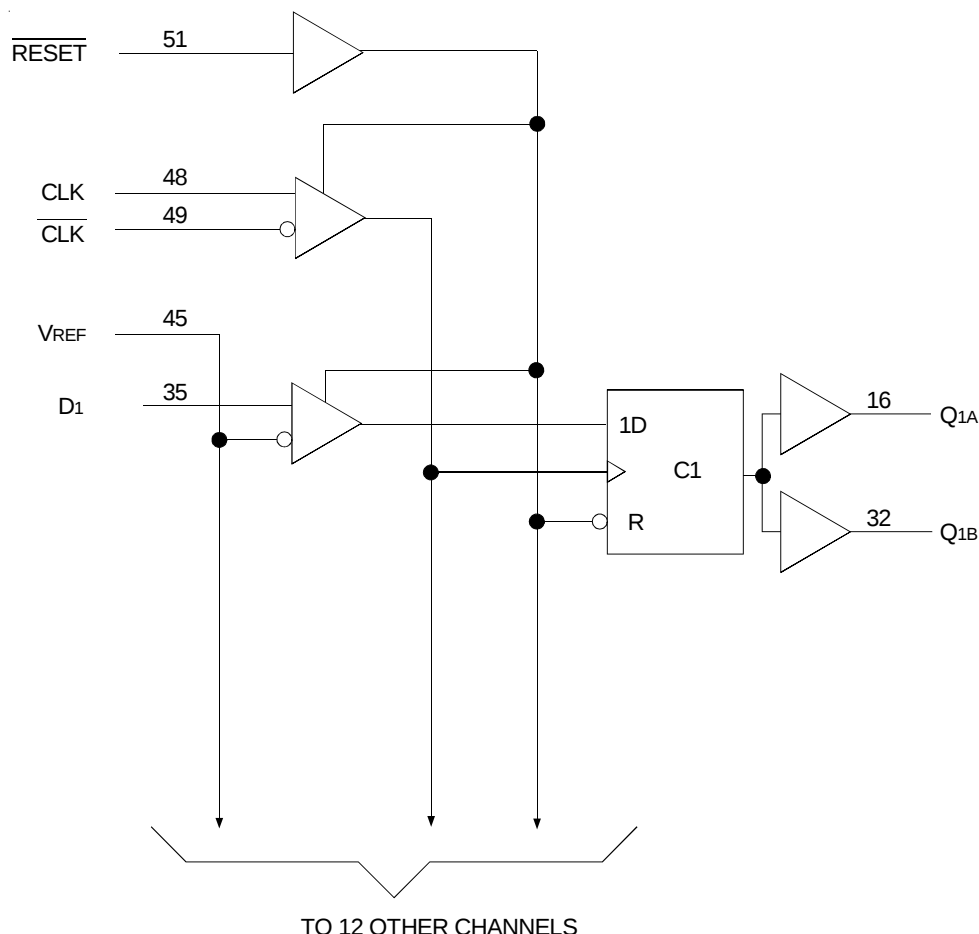
DESCRIPTION:

The SSTVM16859 is a 13-bit to 26-bit registered buffer designed for 2.3V-2.7V V_{DD} and supports low standby operation. All data inputs and outputs are SSTL_2 level compatible with JEDEC standard for SSTL_2.

$\overline{\text{RESET}}$ is an LVC MOS input since it must operate predictably during the power-up phase. $\overline{\text{RESET}}$, which can be operated independent of CLK and $\overline{\text{CLK}}$, must be held in the low state during power-up in order to ensure predictable outputs (low state) before a stable clock has been applied.

$\overline{\text{RESET}}$, when in the low state, will disable all input receivers, reset all registers, and force all outputs to a low state, before a stable clock has been applied. With inputs held low and a stable clock applied, outputs will remain low during the Low-to-High transition of $\overline{\text{RESET}}$.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Names	Description
Q1 - Q13	Data Output
GND	Ground
V _{DDQ}	Output-stage drain power voltage
V _{DD}	Logic power voltage
$\overline{\text{RESET}}$	Asynchronous reset input - resets registers and disables data and clock differential input receivers
V _{REF}	Input reference voltage
CLK	Positive master clock input
$\overline{\text{CLK}}$	Negative master clock input
D1 - D13	Data Input - clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$
Center PAD	Ground (MLF package only)

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = 0°C to +70°C, V_{DD} = 2.5V ±0.2V, V_{DDQ} = 2.5V ±0.2V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{IK}	Control Inputs	V _{DD} = 2.3V, I _I = -18mA	—	—	-1.2	V
V _{OH}		V _{DD} = 2.3V to 2.7V, I _{OH} = -100μA	V _{DD} - 0.2	—	—	V
		V _{DD} = 2.3V, I _{OH} = -16mA	1.95	—	—	
V _{OL}		V _{DD} = 2.3V to 2.7V, I _{OL} = 100μA	—	—	0.2	V
		V _{DD} = 2.3V, I _{OL} = 16mA	—	—	0.35	
I _I	All Inputs	V _{DD} = 2.7V, V _I = V _{DD} or GND	—	—	±5	μA
I _{DD}	Static Standby	I _O = 0, V _{DD} = 2.7V, $\overline{\text{RESET}}$ = GND	—	—	0.01	mA
	Static Operating	I _O = 0, V _{DD} = 2.7V, $\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH} (AC) or V _{IL} (AC)	—	—	20	
I _{DDQ}	Dynamic Operating (Clock Only)	I _O = 0, V _{DD} = 2.7V, $\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle.	—	6	—	μA/Clock MHz
	Dynamic Operating (Per Each Data Input) ⁽¹⁾	I _O = 0, V _{DD} = 2.7V, $\overline{\text{RESET}}$ = V _{DD} , V _I = V _{IH} (AC) or V _{IL} (AC), CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle.	—	43	—	μA/Clock MHz/Data Input
r _{OH}	Output HIGH	V _{DD} = 2.3V to 2.7V, I _{OH} = -20mA	7	—	20	Ω
r _{OL}	Output LOW	V _{DD} = 2.3V to 2.7V, I _{OH} = 20mA	7	—	20	Ω
r _{O(A)}	r _{OH} - r _{OL} each separate bit	V _{DD} = 2.5V, T _A = 25°C, I _{OH} = -20mA	—	—	4	Ω
C _I	Data Inputs	V _{DD} = 2.5V, V _I = V _{REF} ± 310mV	2	—	3	pF
	CLK and $\overline{\text{CLK}}$	V _{ICR} = 1.25V, V _I (PP) = 360mV	2	—	3	
	$\overline{\text{RESET}}$	V _I = V _{DD} or GND	2	—	3	

NOTE:

- Power dissipation levels will allow operation at DDR333 speeds without excessive die temperature.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$ (1)

Symbol	Parameter	Min.	Typ. ⁽⁴⁾	Max.	Unit
V _{DD}	Supply Voltage	V _{DDQ}	—	2.7	V
V _{DDQ}	Output Supply Voltage	2.3	2.5	2.7	V
V _{REF}	Reference Voltage (V _{REF} = V _{DDQ} /2)	1.15	1.25	1.35	V
V _{TT}	Termination Voltage	V _{REF} – 40mV	V _{REF}	V _{REF} + 40mV	V
V _I	Input Voltage	0	—	V _{DD}	V
V _{IH}	AC High-Level Input Voltage	Data Inputs	V _{REF} + 310mV	—	V
V _{IL}	AC Low-Level Input Voltage	Data Inputs	—	V _{REF} – 310mV	V
V _{IH}	DC High-Level Input Voltage	Data Inputs	V _{REF} + 150mV	—	V
V _{IL}	DC Low-Level Input Voltage	Data Inputs	—	V _{REF} – 150mV	V
V _{IH}	High-Level Input Voltage	$\overline{\text{RESET}}$	1.7	—	V
V _{IL}	Low-Level Input Voltage	$\overline{\text{RESET}}$	—	0.7	V
V _{ICR}	Common-Mode Input Range	CLK, $\overline{\text{CLK}}$	0.97	1.53	V
V _{I(PP)}	Peak-to-Peak Input Voltage	CLK, $\overline{\text{CLK}}$	360	—	mV
I _{OH}	High-Level Output Current	—	—	–20	mA
I _{OL}	Low-Level Output Current	—	—	20	mA
T _A	Operating Free-Air Temperature	0	—	+70	°C

NOTE:

1. The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation.

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

Symbol	Parameter	V _{DD} = 2.5V ± 0.2V		Unit
		Min.	Max.	
CLOCK	Clock Frequency	—	200	MHz
t _W	Pulse Duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW	2.5	—	ns
t _{ACT}	Differential Inputs Active Time ⁽¹⁾	—	22	ns
t _{INACT}	Differential Inputs Inactive Time ⁽²⁾	—	22	ns
t _{SU}	Setup Time, Fast Slew Rate ^(3,5)	Data Before CLK↑, CLK↓	0.65	ns
	Setup Time, Slow Slew Rate ^(4,5)		0.75	ns
t _H	Hold Time, Fast Slew Rate ^(3,5)	Data Before CLK↑, CLK↓	0.75	ns
	Hold Time, Slow Slew Rate ^(2,5)		0.9	ns

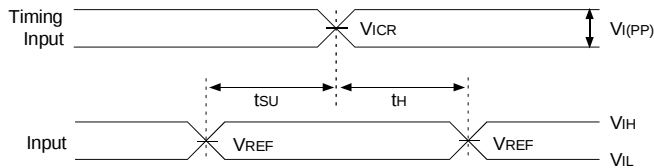
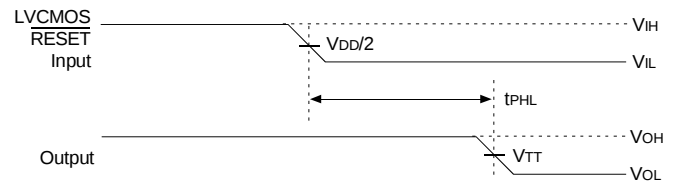
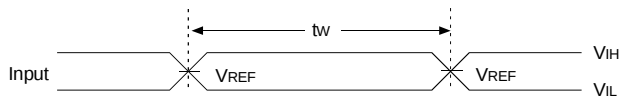
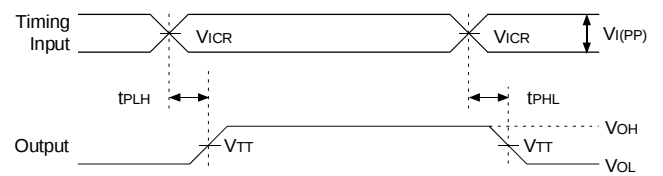
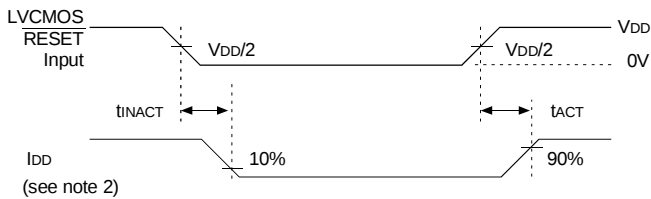
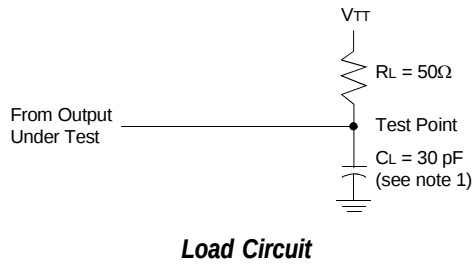
NOTES:

1. Data inputs must be low a minimum time of t_{ACT} max., after $\overline{\text{RESET}}$ is taken HIGH.
2. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{INACT} max., after $\overline{\text{RESET}}$ is taken LOW.
3. For data signal input slew rate is ≥1V/ns.
4. For data signal input slew rate is ≥0.5V/ns and <1V/ns.
5. CLK, $\overline{\text{CLK}}$ signal input slew rates are ≥1V/ns.

SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED)

Symbol	Parameter	V _{DD} = 2.5V ± 0.2V		Unit
		Min.	Max.	
f _{MAX}		200	—	MHz
t _{PDM}	CLK and $\overline{\text{CLK}}$ to Q	1.1	2.6	ns
t _{PDMS}	CLK and $\overline{\text{CLK}}$ to Q (simultaneous switching)	—	2.9	ns
t _{PHL}	$\overline{\text{RESET}}$ to Q	—	5	ns

TEST CIRCUITS AND WAVEFORMS ($V_{DD} = 2.5V \pm 0.2V$)



NOTES:

1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_O = 0mA$.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10MHz$, $Z_o = 50\Omega$, input slew rate = $1 V/ns \pm 20\%$ (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DDQ}/2$
6. $V_{IH} = V_{REF} + 310mV$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS input.
7. $V_{IL} = V_{REF} - 310mV$ (AC voltage levels) for differential inputs. $V_{IL} = GND$ for LVC MOS input.
8. t_{PDM} is t_{PD} with one output switching. t_{PDMSS} is t_{PD} with all outputs switching.

ORDERING INFORMATION

IDT74SSTVM	XX	XXX	XX	XX	
	Family	Device Type	Package	Process	
				Blank	0°C to +70°C (Commercial)
			PA NL		Thin Shrink Small Outline Package Thermally Enhanced Plastic Very Fine Pitch Quad Flat No Lead Package
				859	13-Bit to 26-Bit Registered Buffer with SSTL I/O
				16	Double-Density



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