

74LCXR162245

Low Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs/Outputs and 26Ω Series Resistors in the Outputs

General Description

The LCXR162245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The $T/\bar{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

In addition, all A and B outputs include equivalent 26Ω (nominal) series resistors to reduce overshoot and undershoot and are designed to sink/source up to 12 mA at $V_{CC} = 3.0V$.

The LCXR162245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- A and B side outputs have equivalent 26Ω series resistors
- 5.3 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Flow through pinout
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

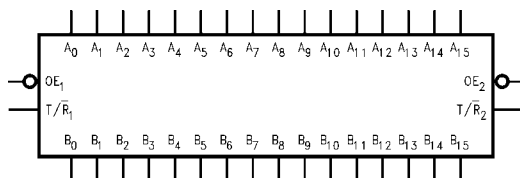
Note 1: To ensure the high-impedance state during power up or down $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCXR162245MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [RAIL]
74LCXR162245MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LCXR162245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [RAIL]
74LCXR162245MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

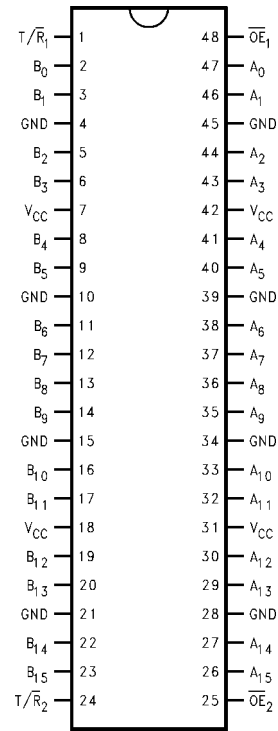


Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input
$T/\bar{R}_n$	Transmit/Receive Input
A_0 – A_{15}	Side A Inputs or 3-STATE Outputs
B_0 – B_{15}	Side B Inputs or 3-STATE Outputs

74LCXR162245 Low Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs/Outputs and 26Ω Series Resistors in the Outputs

Connection Diagram



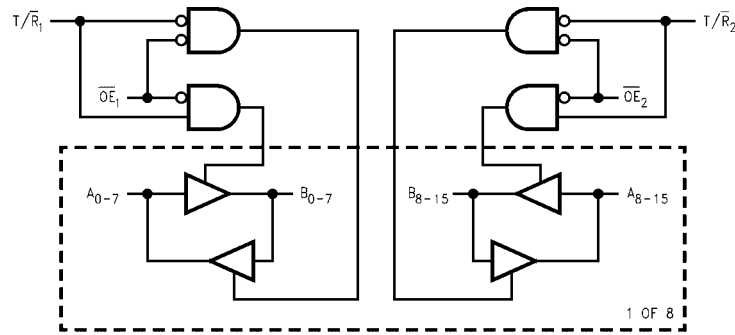
Truth Tables

Inputs		Outputs
$\overline{OE_1}$	$\overline{T/R_1}$	
L	L	Bus B_0 – B_7 Data to Bus A_0 – A_7
L	H	Bus A_0 – A_7 Data to Bus B_0 – B_7
H	X	HIGH Z State on A_0 – A_7 , B_0 – B_7 (Note 2)

Inputs		Outputs
$\overline{OE_2}$	$\overline{T/R_2}$	
L	L	Bus B_8 – B_{15} Data to Bus A_8 – A_{15}
L	H	Bus A_8 – A_{15} Data to Bus B_8 – B_{15}
H	X	HIGH Z State on A_8 – A_{15} , B_8 – B_{15} (Note 2)

Note 2: A and B port inputs are still active

Logic Diagram



Absolute Maximum Ratings ^(Note 3)				
Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	−0.5 to +7.0		V
V _I	DC Input Voltage	−0.5 to +7.0		V
V _O	DC Output Voltage	−0.5 to +7.0 −0.5 to V _{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 4)	V
I _{IK}	DC Input Diode Current	−50	V _I < GND	mA
I _{OK}	DC Output Diode Current	−50 +50	V _O < GND V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions ^(Note 5)

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage	Operating	2.0	3.6
		Data Retention	1.5	3.6
V _I	Input Voltage	0	5.5	V
V _O	Output Voltage	HIGH or LOW State	0	V _{CC}
		3-STATE	0	5.5
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V – 3.6V V _{CC} = 2.7V – 3.0V V _{CC} = 2.3V – 2.7V	±12 ±8 ±4	mA
T _A	Free-Air Operating Temperature	−40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Unused pins (Inputs or I/O's) must be held HIGH or LOW. They may not Float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = −40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7 2.7 – 3.6	1.7 2.0		V
V _{IL}	LOW Level Input Voltage		2.3 – 2.7 2.7 – 3.6		0.7 0.8	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = −100 μA	2.3 – 3.6	V _{CC} − 0.2		V
		I _{OH} = −4 mA	2.3	1.8		
		I _{OH} = −4 mA	2.7	2.2		
		I _{OH} = −6 mA	3.0	2.4		
		I _{OH} = −8 mA	2.7	2.0		
		I _{OH} = −12 mA	3.0	2.0		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 – 3.6		0.2	V
		I _{OL} = 4 mA	2.3		0.6	
		I _{OL} = 4 mA	2.7		0.4	
		I _{OL} = 6 mA	3.0		0.55	
		I _{OL} = 8 mA	2.7		0.6	
		I _{OL} = 12 mA	3.0		0.8	
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I _{OZ}	3-STATE I/O Leakage	0 ≤ V _O ≤ 5.5V	2.3 – 3.6		±5.0	μA
		V _I = V _{IH} or V _{IL}				

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		20	μA
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 6)	2.3 – 3.6		±20	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 – 3.6		500	μA

Note 6: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	5.3	1.5	6.0	1.5	6.4	ns
t _{PLH}	A _n to B _n or B _n to A _n	1.5	5.3	1.5	6.0	1.5	6.4	
t _{PZL}	Output Enable Time	1.5	7.3	1.5	8.0	1.5	9.5	ns
t _{PZH}		1.5	7.3	1.5	8.0	1.5	9.5	
t _{PLZ}	Output Disable Time	1.5	6.4	1.5	6.9	1.5	7.7	ns
t _{PHZ}		1.5	6.4	1.5	6.9	1.5	7.7	
t _{OSHL}	Output to Output Skew (Note 7)		1.0					ns
t _{OSLH}			1.0					

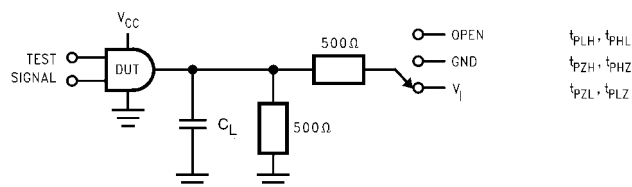
Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

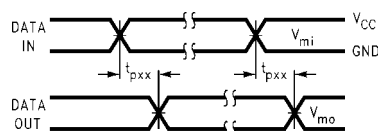
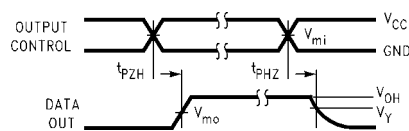
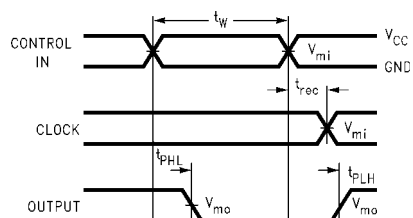
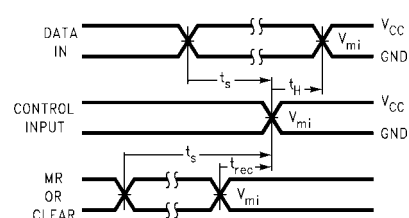
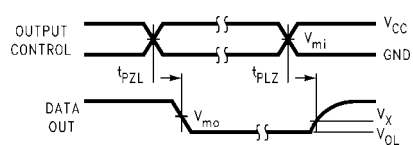
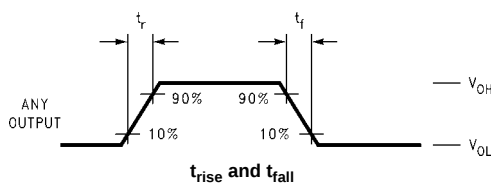
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	3.3 2.5	0.35 0.25	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	3.3 2.5	-0.35 -0.25	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	20	pF

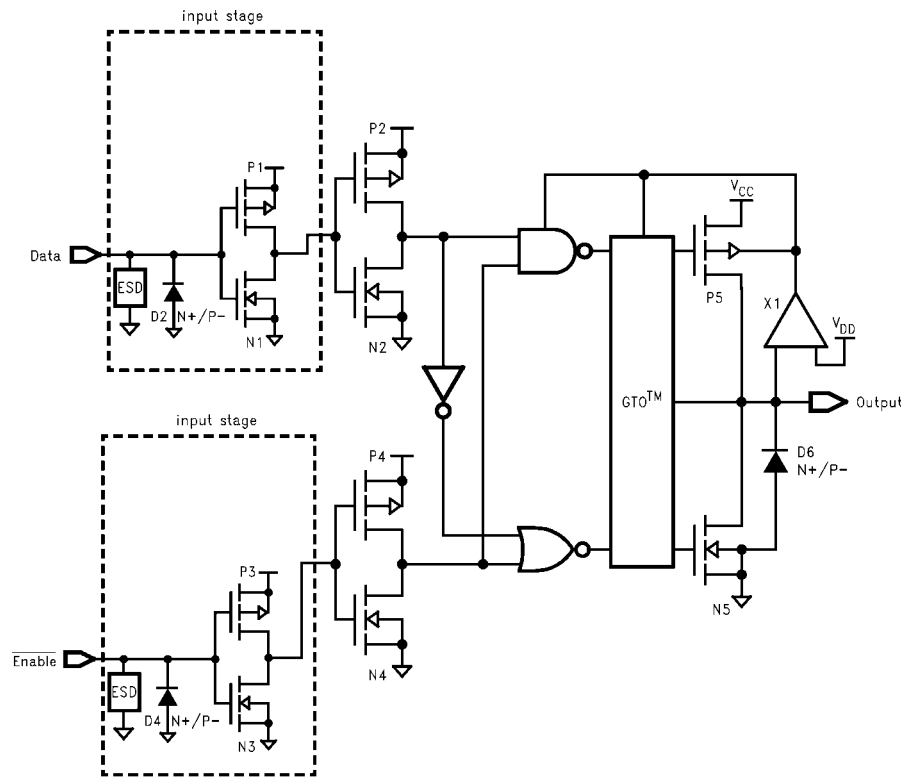
AC LOADING and WAVEFORMS Generic for LCX Family**FIGURE 1. AC Test Circuit** (C_L includes probe and jig capacitance)

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND

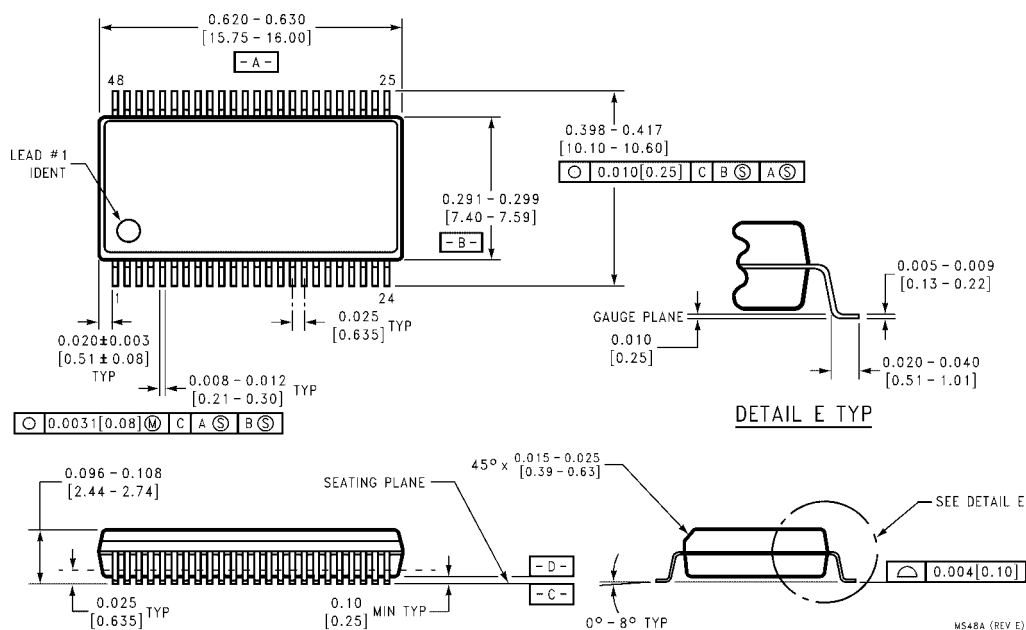
**Waveform for Inverting and Non-Inverting Functions****3-STATE Output High Enable and Disable Times for Logic****Propagation Delay, Pulse Width and t_{rec} Waveforms****Setup Time, Hold Time and Recovery Time for Logic****3-STATE Output Low Enable and Disable Times for Logic****FIGURE 2. Waveforms**
(Input Characteristics; $f = 1MHz$, $t_R = t_F = 3ns$)

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

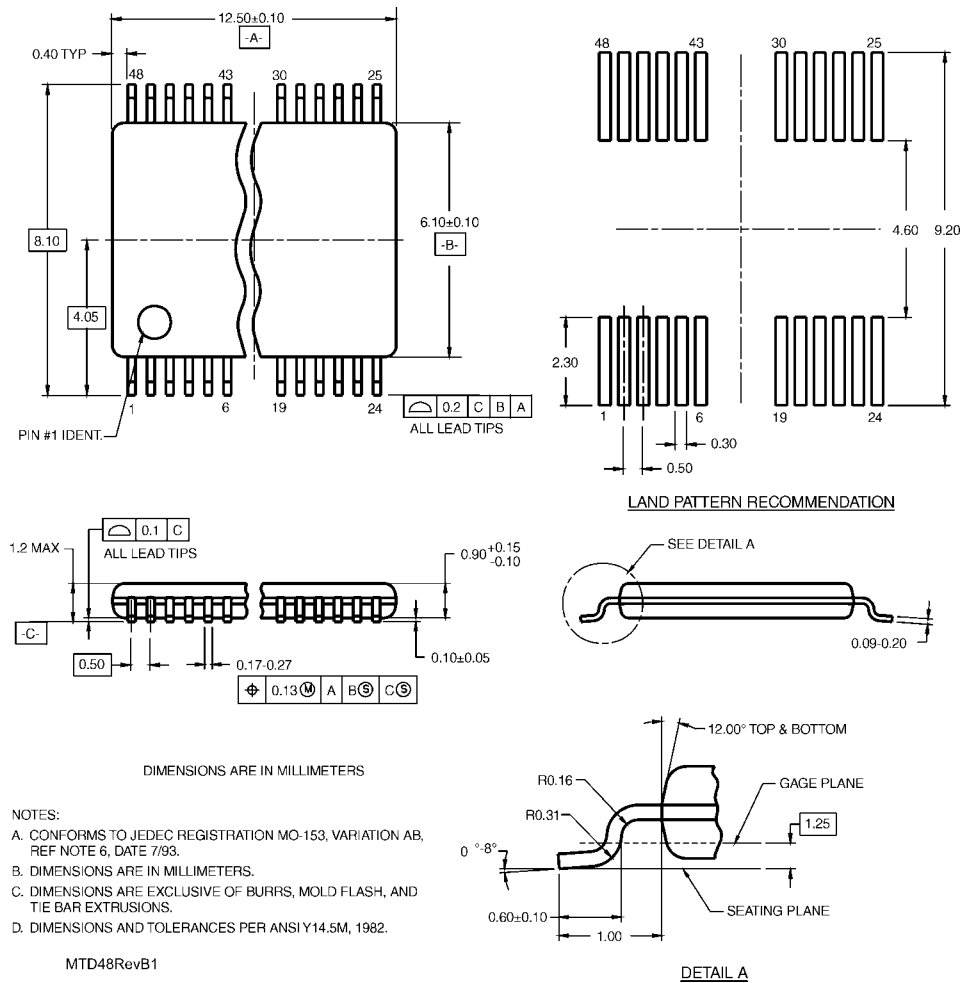


Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com