

74ACTQ74

Quiet Series Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The 74ACTQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q , $\bar{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

The ACTQ74 utilizes Fairchild Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Asynchronous Inputs:

- LOW input to $\bar{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\bar{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\bar{C}_D$ and $\bar{S}_D$ makes both Q and $\bar{Q}$ HIGH

Features

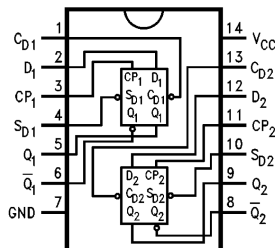
- I_{CC} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- 4 kV minimum ESD immunity
- TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74ACTQ74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74ACTQ74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACTQ74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering form.

Connection Diagram



Pin Descriptions

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

FACT™, FACT Quiet Series™ and GTO™ are trademarks of Fairchild Semiconductor Corporation.

Truth Table

(Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level

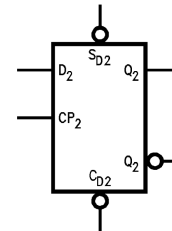
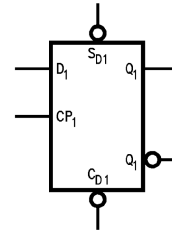
L = LOW Voltage Level

X = Immaterial

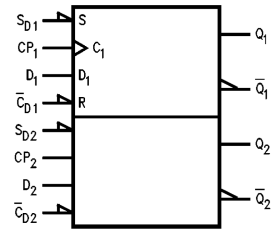
↗ = LOW-to-HIGH Clock Transition

 $Q_0(\overline{Q}_0)$ = Previous $Q(\overline{Q})$ before LOW-to-HIGH Transition of Clock

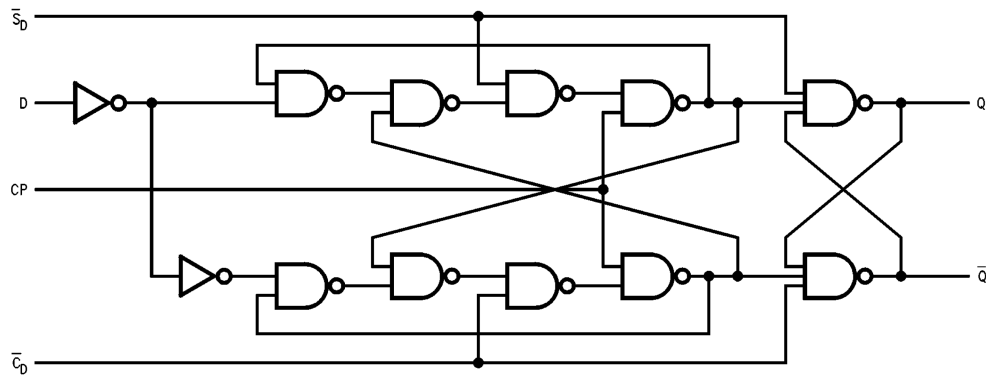
Logic Symbols



IEEE/IEC



Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	–0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	–0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	–65°C to +150°C
DC Latch-Up Source or Sink Current	± 300 mA
Junction Temperature (T_J) PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	–40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = −24 mA I _{OH} = −24 mA (Note 2)
		5.5		4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 2)
		5.5		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum 3-STATE Leakage Current	5.5		± 0.5	± 5.0	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1V
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 2)	5.5			−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	V _{IN} = V _{CC} or GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.1	1.5		V	Figure 1, Figure 2 (Note 4)(Note 5)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	−0.6	−1.2		V	Figure 1, Figure 2 (Note 4)(Note 5)
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 4)(Note 6)
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 4)(Note 6)

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: PDIP package.

Note 5: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 6: Max number of data inputs (n) switching. (n – 1) inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), $f = 1$ MHz.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	5.0	145	200		125		MHz
t _{PLH}	Propagation Delay	5.0	3.0	7.0	8.5	3.0	9.0	ns
t _{PHL}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$							
t _{PLH}	Propagation Delay	5.0	3.0	6.5	8.0	3.0	8.6	ns
t _{PHL}	CP _n to Q _n or $\overline{Q}_n$							
t _{OSLH}	Output to Output	5.0		0.5	1.0		1.0	ns
t _{OSHL}	Skew (Note 8)							

Note 7: Voltage Range 5.0 is 5.0V ± 0.5V.

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V _{CC} (V) (Note 9)	T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW D _n to CP _n	5.0	1.0	3.0	3.0	ns
t _H	Hold Time, HIGH or LOW D _n to CP _n	5.0	−0.5	1.5	1.5	ns
t _W	CP _n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	4.0	4.0	ns
t _{REC}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	1.5	1.5	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	60.0	pF	V _{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

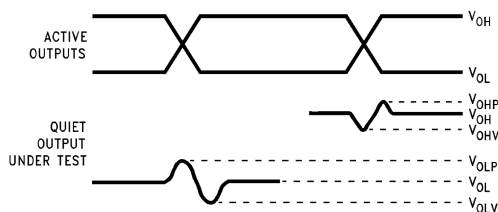
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskw the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.



V_{OHV} and V_{OLP} are measured with respect to ground reference.

Input pulses have the following characteristics: $f = 1 \text{ MHz}$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$, skew $< 150 \text{ ps}$.

FIGURE 1. Quiet Output Noise Voltage Waveforms

5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV} :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case transition for active and enable.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD} :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL} , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD} .
- Next decrease the input HIGH voltage level, V_{IH} , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD} .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

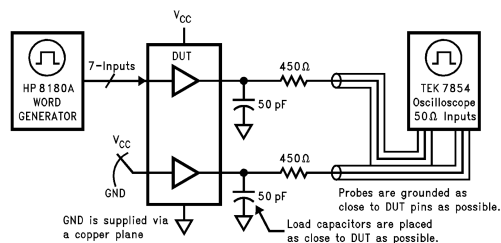
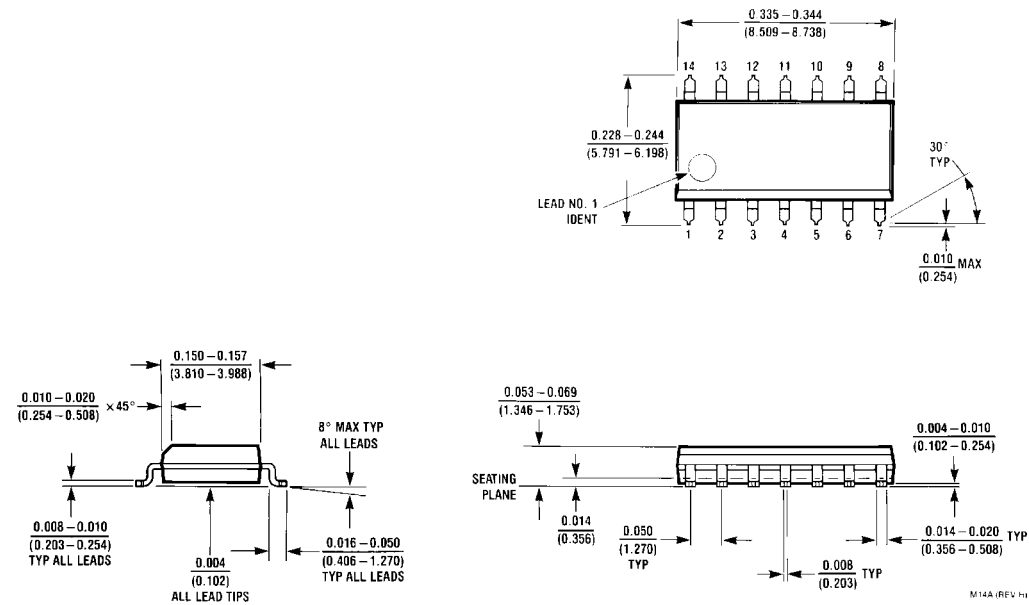
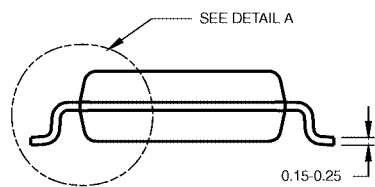
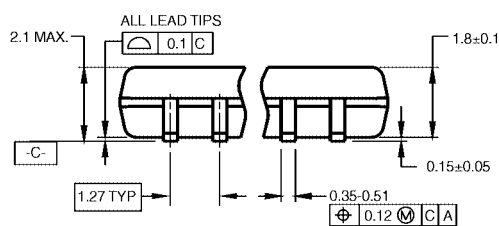
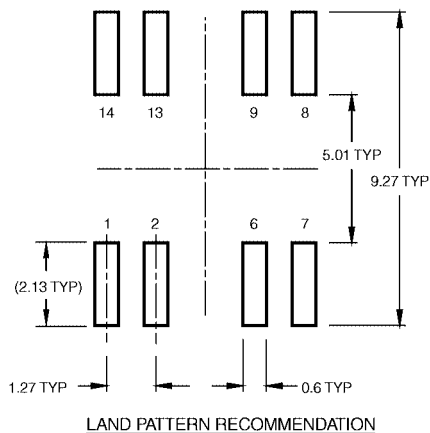
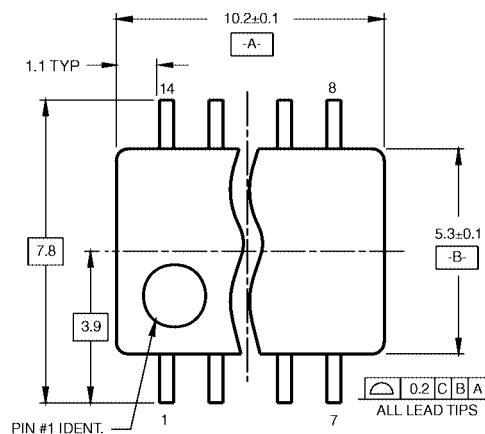


FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

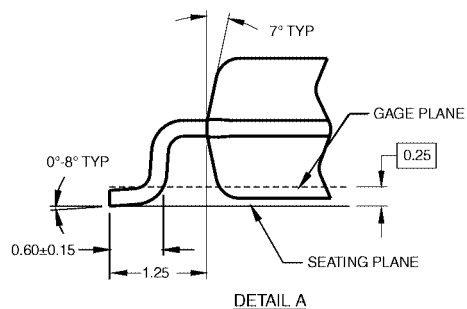
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

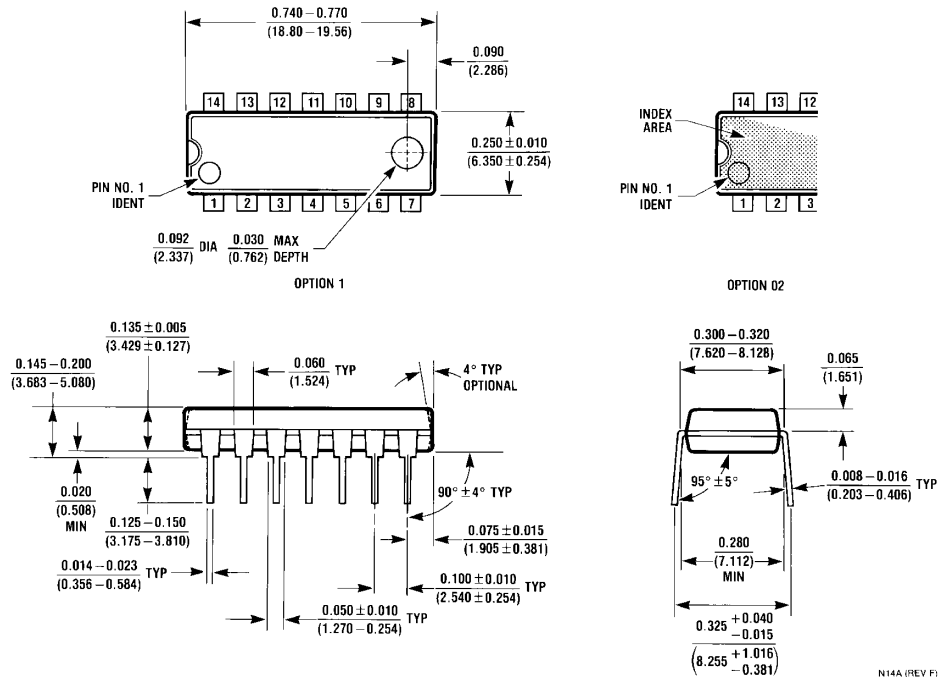
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
 2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
- www.fairchildsemi.com**