FAIRCHILD SEMICONDUCTOR™

August 1986
Revised July 2001

DM9602
Dual Retriggerable, Resettable One Shots

General Description

These dual resettable, retriggerable one shots have two inputs per function; one which is active HIGH, and one which is active LOW. This allows the designer to employ either leading-edge or trailing-edge triggering, which is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is allowed to rapidly discharge and then charge again. The retriggerable feature permits output pulse widths to be extended. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. The output pulse may then be terminated at any time by applying a LOW logic level to the RESET pin. Retriggering may be inhibited by either connecting the Q output to an active HIGH input, or the $\overline{Q}$ output to an active LOW input.

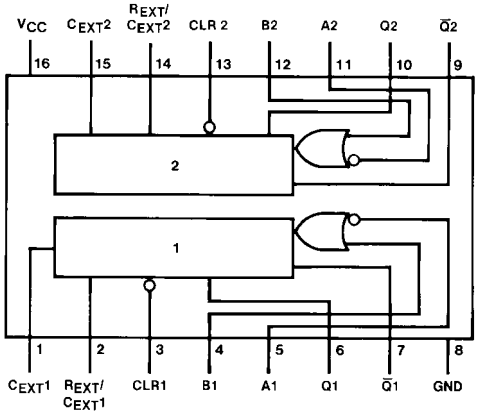
Features

- 70 ns to ∞ output width range
- Resettable and retriggerable—0% to 100% duty cycle
- TTL input gating—leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for V_{CC} and temperature variations

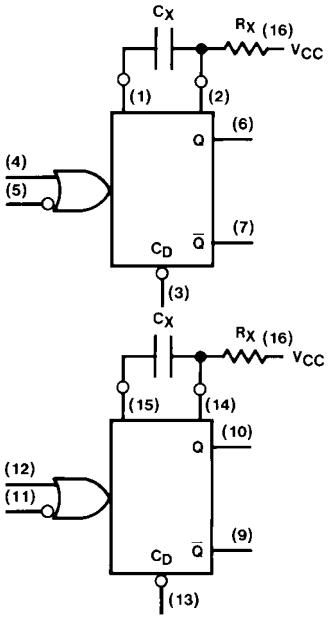
Ordering Code:

Order Number	Package Number	Package Description
DM9602N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Logic Diagrams



Function Table

Pin Numbers			Operation
A	B	CLR	
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
3. The output pulse with (t) is defined as follows:

$$t = K R_X C_X \left[1 + \frac{1}{R_X}\right] \quad \begin{array}{l}\text{for } C_X > 10^3 \text{ pF} \\ K \approx 0.34\end{array}$$

where: R_X is in kΩ, C_X is in pF

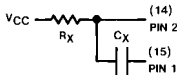
t is in ns

for $C_X < 10^3$ pF, see Figure 1.

for K vs. C_X see Figure 6.

4. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   1. Use with low leakage capacitors:

      The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0V is less than 3 μA, and the inverse capacitor leakage at 1.0V is less than 5 μA over the operational temperature range.

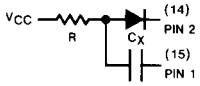


      $R < 0.6\ R_X$ (Max)

   2. Use with high inverse leakage current electrolytic capacitors:

      The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

      $t \approx 0.3\ RC_X$



   3. Use to obtain extended pulse widths:

      This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

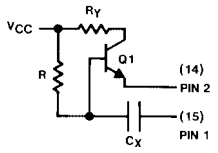
      $R < R_X\ (0.7)\ (h_{FE}\ Q1)$ or $< 2.5\ M\Omega$, whichever is the lesser

      $R_X\ (min) < R_Y < R_X\ (max)$

      ($5\ k\Omega \le R_Y \le 10\ k\Omega$ is recommended)

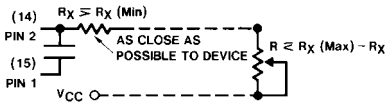
      Q1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962.

      $t \approx 0.3\ RC_X$

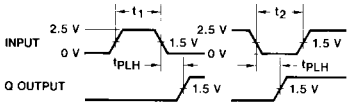


      This configuration is not recommended with retriggerable operation.

5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules (See Triggering Truth Table)

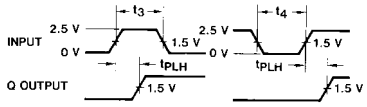


Input to Pin 5(11), (Pin 3(13) = HIGH)

Pin 4(12) = LOW

t_1, t_3 = Min. Positive Input Pulse Width > 40 ns

t_2, t_4 = Min. Negative Input Pulse Width > 40 ns

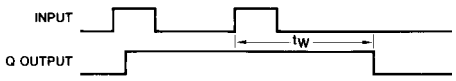


Input to Pin 4(12) (Pin 3(13) = HIGH)

Pin 5(11) = HIGH

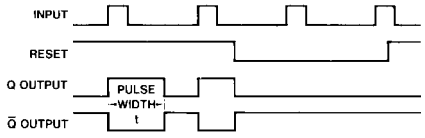
8. The retriggerable pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = K R_X C_X \left(1 + \frac{1}{R_X}\right) + t_{PLH}$$



The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X (ns) after the initial trigger pulse (i.e., during the discharge cycle).

9. Reset Operation—An overriding clear (active LOW level) is provided on each one shot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



10. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the DM9602 is recommended.

Note 1: For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

Typical Performance Characteristics

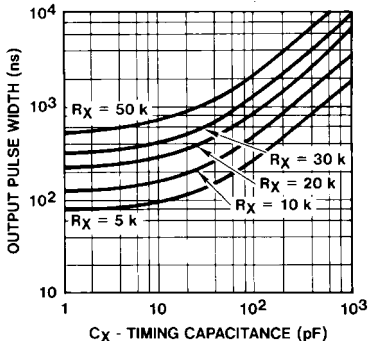


FIGURE 1. Output Pulse Width vs. Timing Resistance and Capacitance for $C_X < 10^3$ pF

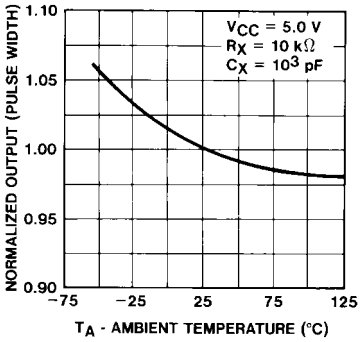


FIGURE 2. Normalized Output Pulse Width vs. Ambient Temperature

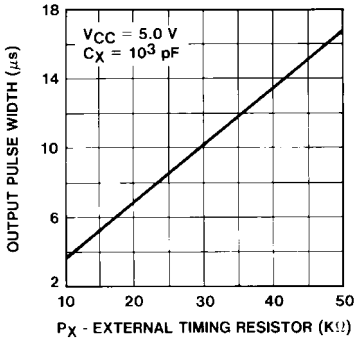


FIGURE 3. Pulse Width vs. Timing Resistor

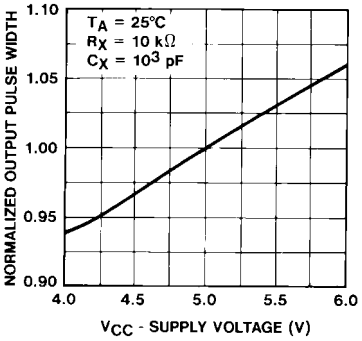


FIGURE 4. Normalized Output Pulse Width vs. Supply Voltage

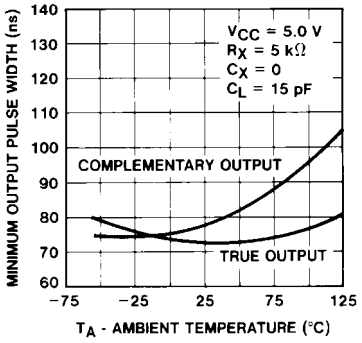


FIGURE 5. Minimum Output Pulse Width vs. Ambient Temperature

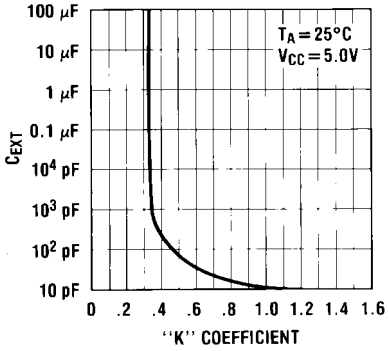


FIGURE 6. Typical "K" Coefficient Variation vs. Timing Capacitance

Absolute Maximum Ratings(Note 2)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	$T_A = -55°C$				V
		$T_A = 0°C$	1.9			
		$T_A = 25°C$	1.8			
		$T_A = 75°C$	1.65			
		$T_A = 125°C$				
V_{IL}	LOW Level Input Voltage	$T_A = -55°C$				V
		$T_A = 0°C$			0.85	
		$T_A = 25°C$			0.85	
		$T_A = 75°C$			0.85	
		$T_A = 125°C$				
I_{OH}	HIGH Level Output Current				−0.8	mA
I_{OL}	LOW Level Output Current				16	mA
T_A	Free Air Operating Temperature		0		75	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min (Note 5)		2.4			V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 5)				0.45	V
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 4.5V				60	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max	V_I = 0.45V			−1.6	mA
		V_{CC} = Min	V_I = 0.45V			−1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max, V_{OUT} = 1V (Note 5)(Note 6)				−35	mA
I_{CC}	Supply Current	V_{CC} = Max			39	50	mA

Note 3: Unless otherwise noted, R_X = 10k for all tests.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Ground PIN 1(15) for V_{OL} on PIN 7(9) or V_{OH} and I_{OS} on PIN 6(10) and apply momentary ground to PIN 4(12). Open PIN 1(15) for V_{OL} on PIN 6(10) or V_{OH} and I_{OS} on PIN 7(9).

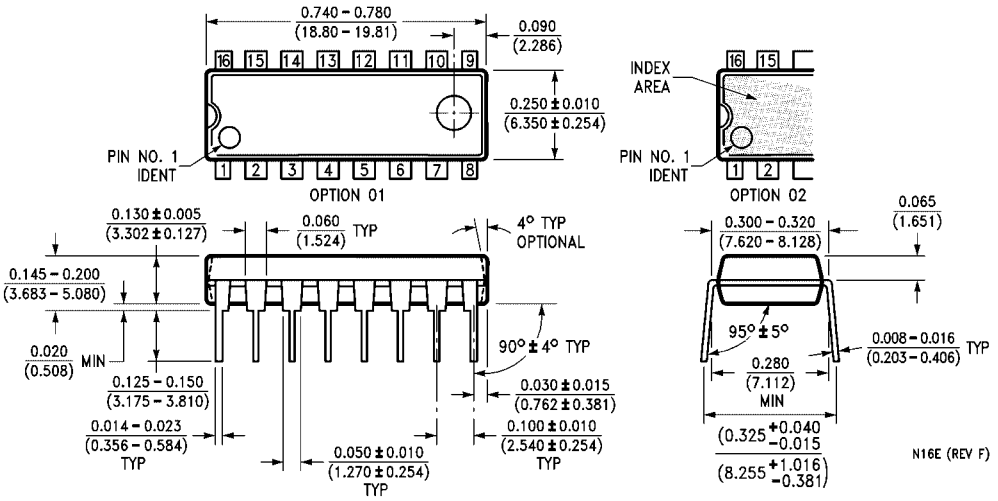
Note 6: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = 5V, T_A = 25°C

Symbol	Parameter		Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	Negative Trigger Input to True Output	C_L = 15 pF C_X = 0 R_X = 5 kΩ		40	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output	Negative Trigger Input To Complement Output			48	ns
t_{PW}(MIN)	Minimum True Output Pulse Width				100	ns
	Minimum Complement Pulse Width				110	
t_{PW}	Pulse Width		R_X = 10 kΩ C_X = 1000 pF	3.08	3.76	µs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pins 2, 14 to GND		50	pF
R_X	External Timing Resistor			5	50	kΩ

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E