

## DM93L38 8-Bit Multiple Port Register

### General Description

The DM93L38 is an 8-bit multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all TTL families.

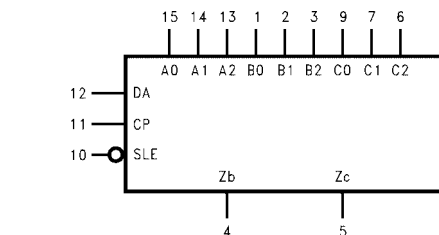
### Features

- Master/slave operation permitting simultaneous write/read without race problems
- Simultaneously read two bits and write one bit in any one of eight bit positions
- Readily expandable to allow for larger word sizes

### Ordering Code:

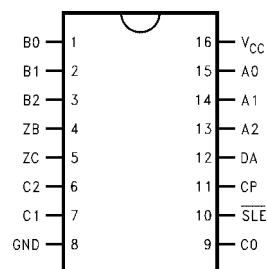
Order Number	Package Number	Package Description
DM93L38N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

### Logic Symbol



V<sub>CC</sub> = Pin 16  
GND = Pin 8

### Connection Diagram



### Pin Descriptions

Pin Names	Description
A0–A2	Write Address Inputs
DA	Data Input
B0–B2	B Read Address Inputs
C0–C2	C Read Address Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{\text{SLE}}$	Slave Enable Input (Active LOW)
ZB	B Output
ZC	C Output

## Functional Description

The DM93L38 8-bit multiple port register can be considered a 1-bit slice of eight high speed working registers. Data can be written into any one and read from any two of the eight locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous read/write activity from the same location. When the clock input (CP) is LOW data applied to the data input line ( $D_A$ ) enters the selected master. This selection is accomplished by coding the three write input select lines ( $A_0$ – $A_2$ ) appropriately. Data is stored synchronously with the rising edge of the clock pulse.

The information for each of the two slaved (output) latches is selected by two sets of read address inputs ( $B_0$ – $B_2$  and  $C_0$ – $C_2$ ). The information enters the slave while the clock is HIGH and is stored while the clock is LOW. If Slave Enable is LOW ( $\overline{SLE}$ ), the slave latches are continuously enabled.

The signals are available on the output pins ( $Z_B$  and  $Z_C$ ). The input bit selection and the two output bit selections can be accomplished independently or simultaneously. The data flows into the device, is demultiplexed according to the state of the write address lines and is clocked into the selected latch. The eight latches function as masters and store the input data. The two output latches are slaves and hold the data during the read operation. The state of each slave is determined by the state of the master selected by its associated set of read address inputs.

The method of parallel expansion is shown in Figure 1. One DM93L38 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time, where n devices are connected in parallel.

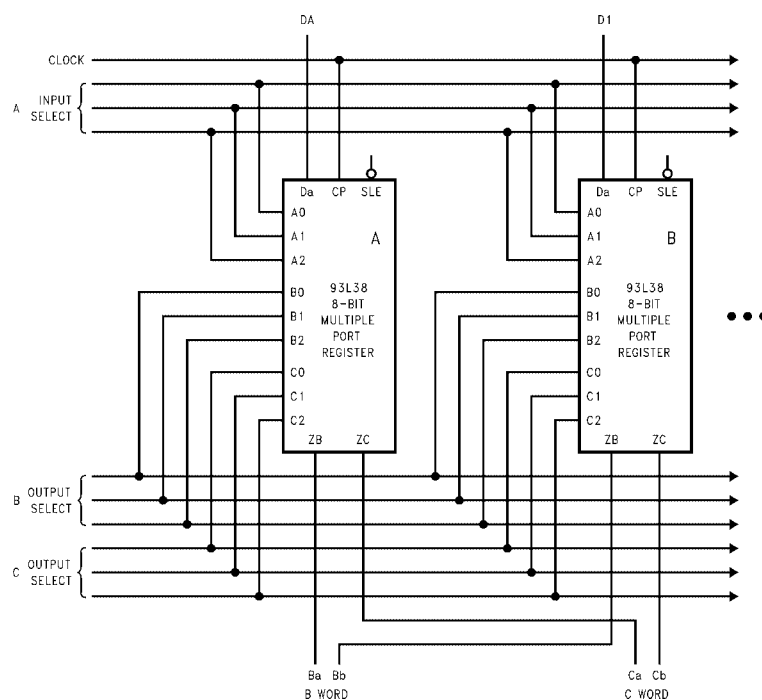
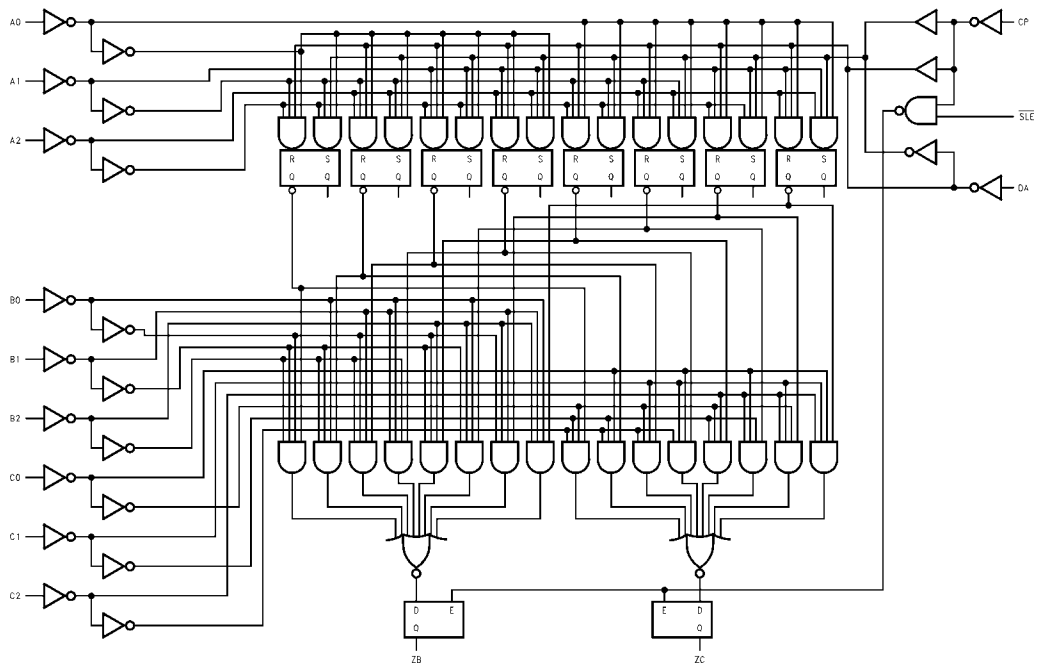


FIGURE 1. Parallel Expansion

# Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Norm	Max	Units
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.7	V
I <sub>OH</sub>	HIGH Level Output Current			–400	μA
I <sub>OL</sub>	LOW Level Output Current			4.8	mA
T <sub>A</sub>	Free Air Operating Temperature	–55		125	°C
t <sub>S</sub> (H)	Setup Time HIGH or LOW	30			ns
t <sub>S</sub> (L)	D <sub>A</sub> to CP	22			
t <sub>H</sub> (H)	Hold Time HIGH or LOW	0			ns
t <sub>H</sub> (L)	D <sub>A</sub> to CP	–4.0			
t <sub>S</sub> (H)	Setup Time HIGH or LOW	0			ns
t <sub>S</sub> (L)	A <sub>n</sub> to CP	0			
t <sub>H</sub> (H)	Hold Time HIGH or LOW	0			ns
t <sub>H</sub> (L)	A <sub>n</sub> to CP	0			
t <sub>W</sub> (H)	CP Pulse Width HIGH or LOW	40			ns
t <sub>W</sub> (L)		30			

**Electrical Characteristics**

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –10 mA			–1.5	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.4			V
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>CC</sub> = Min I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.3	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	HIGH Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V			50	μA
I <sub>IL</sub>	LOW Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.3V			–2	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	–2.5		–25	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 4)			70	mA

**Note 2:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

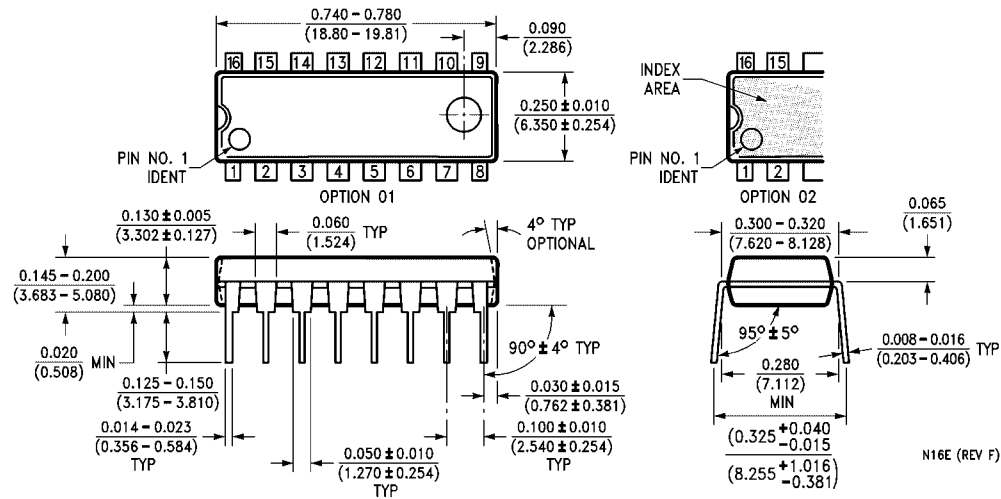
**Note 3:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 4:** I<sub>CC</sub> is measured with all outputs OPEN and all input grounded.

Switching Characteristics				
$V_{CC} = +5.0V, T_A = +25^{\circ}C$				
Symbol	Parameter	$C_L = 15\text{ pF}$		Units
		Min	Max	
$t_{PLH}$	Propagation Delay		68	ns
$t_{PHL}$	$B_n$ or $C_n$ or $Z_n$		95	
$t_{PLH}$	Propagation Delay		70	ns
$t_{PHL}$	$D_A$ to $Z_n$		92	
$t_{PLH}$	Propagation Delay		65	ns
$t_{PHL}$	CP to $Z_n$		57	

## Physical Dimensions

inches (millimeters) unless otherwise noted



N16E (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)