NAND FLASH
528 Byte, 264 Word Page Family

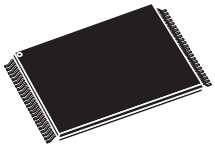
128 Mbit, 256 Mbit, 512 Mbit, 1 Gbit (x8/x16) 1.8V, 3V Supply Flash Memories

DATA BRIEFING

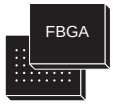
FEATURES SUMMARY

- HIGH DENSITY NAND FLASH MEMORIES
  - Up to 1 Gbit memory array
  - Up to 32Mbit spare area
  - Cost effective solutions for mass storage applications
- NAND INTERFACE
  - x8 or x16 bus width
  - Multiplexed Address/ Data
  - Pinout compatibility for all densities
- SUPPLY VOLTAGE
  - 1.8V device: V_{CC} = 1.65 to 1.95V
  - 3.0V device: V_{CC} = 2.7 to 3.6V
- PAGE SIZE
  - x8 device: (512 + 16 spare) Bytes
  - x16 device: (256 + 8 spare) Words
- BLOCK SIZE
  - x8 device: (16K + 512 spare) Bytes
  - x16 device: (8K + 256 spare) Words
- PAGE READ / PROGRAM
  - Random access: 12µs (max)
  - Sequential access: 50ns (min)
  - Page program time: 200µs (typ)
- COPY BACK PROGRAM MODE
  - Fast page copy without external buffering
- CACHE PROGRAM MODE
  - Internal Cache Register to improve the program throughput
- FAST BLOCK ERASE
  - Block erase time: 2ms (Typ)
- STATUS REGISTER
- ELECTRONIC SIGNATURE
- CHIP ENABLE 'DON'T CARE' OPTION
  - Simple interface with microcontroller

Figure 1. Packages



TSOP48
12 x 20 mm



VFBGA63 8.5x15x1 mm
TFBGA63 8.5x15x1.2 mm
VFBGA63 9x11x1 mm

- AUTOMATIC PAGE 0 READ AT POWER-UP OPTION
  - Boot from NAND support
  - Automatic Memory Download
- SERIAL NUMBER OPTION
- HARDWARE DATA PROTECTION
  - Program/Erase locked during Power transitions
- DATA INTEGRITY
  - 100,000 Program/Erase cycles
  - 10 years Data Retention
- DEVELOPMENT TOOLS
  - Error Correction Code software and hardware models
  - Bad Blocks Management and Wear Leveling algorithms
  - PC Demo board with simulation software
  - File System OS Native reference software
  - Hardware simulation models

For further information please contact the STMicroelectronics distributor nearest to you.

SUMMARY DESCRIPTION

The NAND Flash 528 Byte/ 264 Word Page is a family of non-volatile Flash memories that uses NAND cell technology. The devices range from 128Mbits to 1Gbit and operate with either a 1.8V or 3V voltage supply. The size of a Page is either 528 Bytes (512 + 16 spare) or 264 Words (256 + 8 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 or x16 Input/Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100,000 cycles. To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC). A Write Protect pin is available to give a hardware protection against program and erase operations.

The devices feature an open-drain Ready/Busy output that can be used to identify if the Program/ Erase/Read (P/E/R) Controller is currently active. The use of an open-drain output allows the Ready/ Busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back command is available to optimize the management of defective blocks. When a Page Program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

Each device has a Cache Program feature which improves the program throughput for large files. It loads the data in a Cache Register while the previous data is transferred to the Page Buffer and programmed into the memory array.

The devices are available in the following packages:

- TSOP48 12 x 20mm for all products
- VFBGA63 (8.5x15x1 mm, 6 x 8 ball array, 0.8mm pitch) for the 512Mb product
- TFBGA63 (8.5x15x1.2 mm, 6 x 8 ball array, 0.8mm pitch) for the 1Gb product
- VFBGA63 (9x15x1 mm, 6 x 8 ball array, 0.8mm pitch) for 128Mb and 256Mb products.

Three options are available for the NAND Flash family:

- Automatic Page 0 Read after Power-up, which allows the microcontroller to directly download the boot code from page 0.
- Chip Enable Don't Care, which allows code to be directly downloaded by a microcontroller, as Chip Enable transitions during the latency time do not stop the read operation.
- A Serial Number, which allows each device to be uniquely identified. The Serial Number options is subject to an NDA (Non Disclosure Agreement) and so not described in the datasheet. For more details of this option contact your nearest ST Sales office.

For information on how to order these options refer to Table 3, Ordering Information Scheme. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

See Table 1, Product List, for all the devices available in the family.

Table 1. Product List

Part Number	Density	Bus Width	Page Size	Block Size	Memory Array	Operating Voltage	Timings				Package
							Random Access Max	Sequential Access Min	Page Program Typical	Block Erase Typical	
NAND128R3A	128Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 1024 Blocks	1.65 to 1.95V	15µs	60ns	300µs	2ms	TSOP48 VFBGA63 (9x11x1 mm)
NAND128W3A						2.7 to 3.6V	12µs	50ns	200µs		
NAND128R4A		x16	256+8 Words	8K+256 Words		1.65 to 1.95V	15µs	60ns	300µs		
NAND128W4A						2.7 to 3.6V	12µs	50ns	200µs		
NAND256R3A	256Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 2048 Blocks	1.65 to 1.95V	15µs	60ns	300µs	2ms	TSOP48 VFBGA63 (9x11x1 mm)
NAND256W3A						2.7 to 3.6V	12µs	50ns	200µs		
NAND256R4A		x16	256+8 Words	8K+256 Words		1.65 to 1.95V	15µs	60ns	300µs		
NAND256W4A						2.7 to 3.6V	12µs	50ns	200µs		
NAND512R3A	512Mbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 4096 Blocks	1.65 to 1.95V	15µs	60ns	300µs	2ms	TSOP48 VFBGA63 (8.5x15x1 mm)
NAND512W3A						2.7 to 3.6V	12µs	50ns	200µs		
NAND512R4A		x16	256+8 Words	8K+256 Words		1.65 to 1.95V	15µs	60ns	300µs		
NAND512W4A						2.7 to 3.6V	12µs	50ns	200µs		
NAND01GR3A	1Gbit	x8	512+16 Bytes	16K+512 Bytes	32 Pages x 8192 Blocks	1.65 to 1.95V	15µs	60ns	300µs	2ms	TSOP48 TFBGA63 (8.5x15x1.2 mm)
NAND01GW3A						2.7 to 3.6V	12µs	50ns	200µs		
NAND01GR4A		x16	256+8 Words	8K+256 Words		1.65 to 1.95V	15µs	60ns	300µs		
NAND01GW4A						2.7 to 3.6V	12µs	50ns	200µs		

Figure 2. Logic Block Diagram

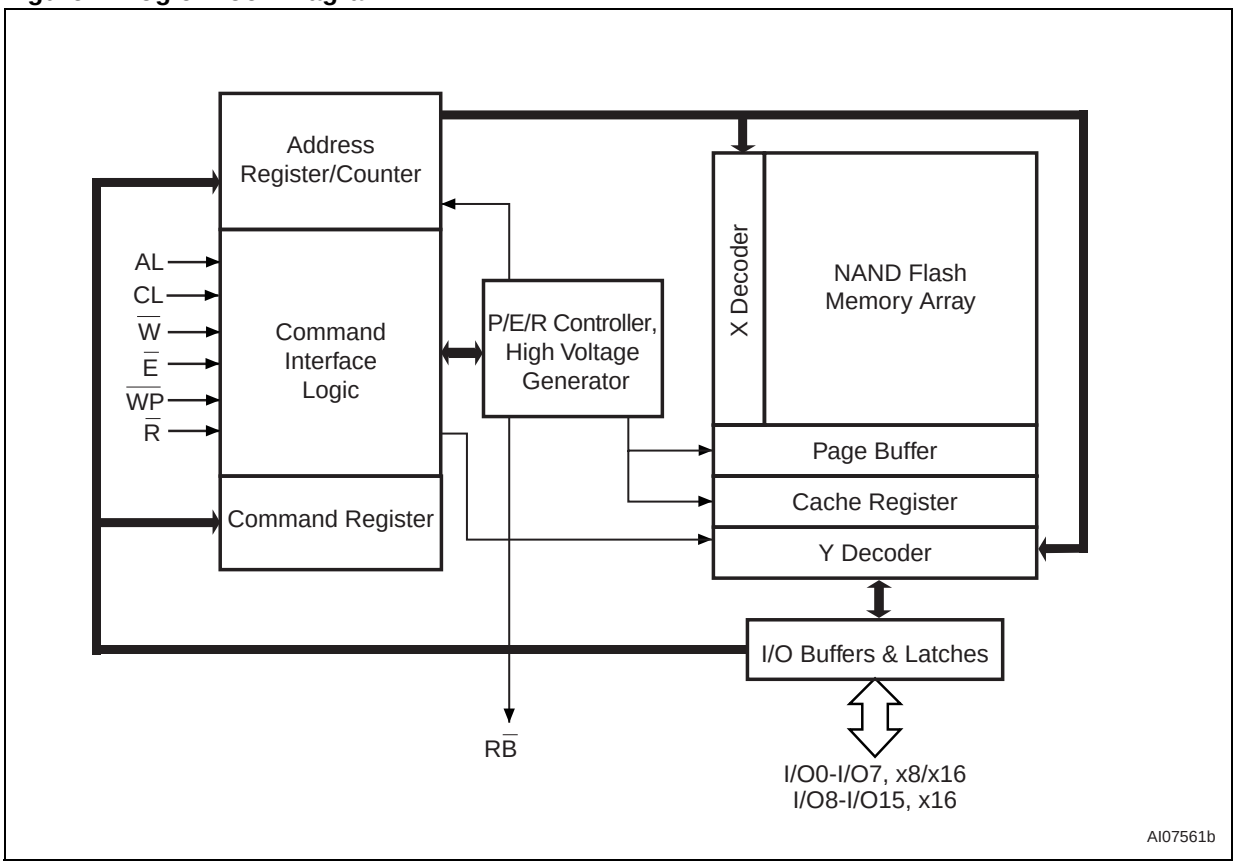


Figure 3. Logic Diagram

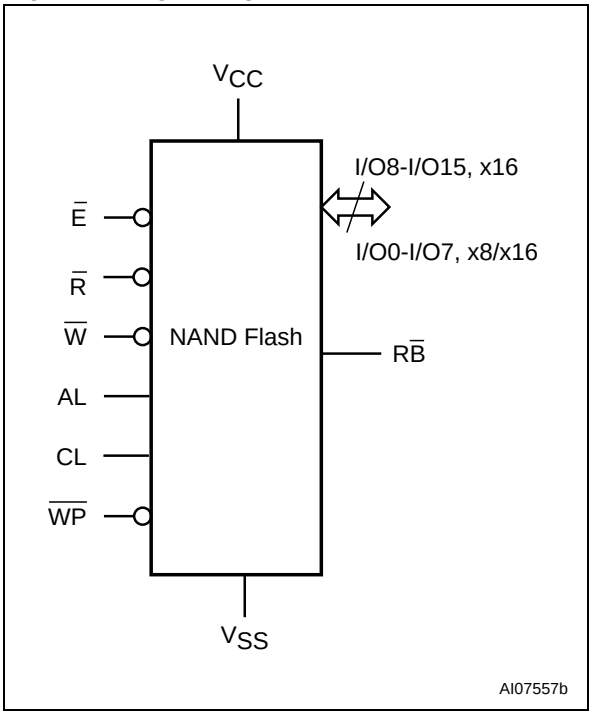


Table 2. Signal Names

I/O8-15	Data Input/Outputs for x16 devices
I/O0-7	Data Input/Outputs, Address Inputs, or Command Inputs for x8 and x16 devices
AL	Address Latch Enable
CL	Command Latch Enable
$\overline{E}$	Chip Enable
$\overline{R}$	Read Enable
$R\overline{B}$	Ready/Busy (open-drain output)
$\overline{W}$	Write Enable
$\overline{WP}$	Write Protect
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Do Not Use

PART NUMBERING

Table 3. Ordering Information Scheme

Example: NAND512R3A 0 A ZA 1 T

Device Type

NAND Flash Memory

Density

128 = 128Mb
256 = 256Mb
512 = 512Mb
01G = 1Gb

Operating Voltage

R = V_{CC} = 1.65 to 1.95V
W = V_{CC} = 2.7 to 3.6V

Bus Width

3 = x8
4 = x16

Family Identifier

A = 528 Bytes/ 264 Word Page

Options

0 = normal
1 = Read Page0 at Power-up
2 = Chip Enable Don't Care
3 = Chip Enable Don't Care Enabled and Read Page0 at Power-up

Silicon Version

A, B, C, D

Package

N = TSOP48 12 x 20mm
ZA = VFBGA63 9 x 11x1mm, 6x8 ball array, 0.8mm pitch (128Mbit and 256Mbit devices)
ZA = VFBGA63 8.5 x 15x1mm, 6x8 ball array, 0.8mm pitch (512Mbit devices)
ZA = TFBGA63 8.5 x 15x1.2mm, 6x8 ball array, 0.8mm pitch (1Gbit devices)

Temperature Range

1 = 0 to 70 °C
6 = –40 to 85 °C

Option

blank = Standard Packing
T = Tape & Reel Packing
E = Lead Free Package, Standard Packing
F = Lead Free Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits, in valid blocks, erased to '1'.
For further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 4. Document Revision History

Date	Version	Revision Details
16-Apr-2003	1.0	First Issue
18-Jun-2003	1.1	NAND Databrief updated to first issue of NAND Datasheet (text changes in FEATURES SUMMARY and SUMMARY DESCRIPTION sections).
18-Jul-2003	1.2	NAND Databrief updated to second issue of NAND Datasheet: VFBGA63 9 x 11mm package added and minor text changes.
07-Aug-2003	2.0	NAND Databrief updated to 07-Aug-2003 2.0 issue of NAND Datasheet: minor text changes to clarify packages.

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