



STS1C1S250

N-CHANNEL 250V - 0.9Ω - 0.75A SO-8

P-CHANNEL 250V - 2.1Ω - 0.6A SO-8

MESH OVERLAY POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS1C1S250(N-Channel)	250 V	<1.4Ω	0.80 A
STS1C1S250(P-Channel)	250 V	<2.8Ω	0.60 A

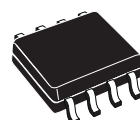
- TYPICAL R_{DS(on)} (N-Channel) = 0.9 Ω
- TYPICAL R_{DS(on)} (P-Channel) = 2.1 Ω
- GATE-SOURCE ZENER DIODE
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY

DESCRIPTION

This complementary pair uses the Company's proprietary high voltage MESH OVERLAY™ process based on advanced strip layout and efficient edge termination. Designed for high volume manufacturing capability, it is ideal in lighting converters such as CFL supplied from 120V mains.

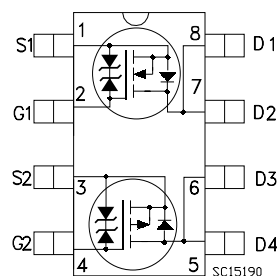
APPLICATIONS

- LIGHTING



SO-8

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		N-CHANNEL	P-CHANNEL	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	250	250	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	250	250	V
V _{GS}	Gate- source Voltage	±25		V
I _D	Drain Current (continuous) at T _C = 25°C	0.75	0.60	A
I _D	Drain Current (continuous) at T _C = 100°C	0.47	0.38	A
I _{DM} (1)	Drain Current (pulsed)	3	2.4	A
P _{TOT}	Total Dissipation at T _C = 25°C Single Operation Total Dissipation at T _C = 25°C Dual Operation	1.6 2		W
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(1)Pulse width limited by safe operating area

STS1C1S250

THERMAL DATA

Rthj-amb (2)	Thermal Resistance Junction-ambient Max (Single Operating) (Dual Operating)	62.5 78	°C/W
--------------	--	------------	------

(2) Mounted on 0.5 in² pad of 2oz. copper.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	N-CHANNEL I _D = 250 µA, V _{GS} = 0 P-CHANNEL I _D = 250 µA, V _{GS} = 0	n-ch p-ch	250 250			V V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C	n-ch p-ch n-ch p-ch			1 1 10 10	µA µA µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V	n-ch p-ch			±10 ±10	µA µA

ON (1)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	N-CHANNEL V _{DS} = V _{GS} , I _D = 250µA P-CHANNEL V _{DS} = V _{GS} , I _D = 250µA	n-ch p-ch	2 2	3 3	4 4	V V
R _{DS(on)}	Static Drain-source On Resistance	N-CHANNEL V _{GS} = 10V, I _D = 0.40A P-CHANNEL V _{GS} = 10V, I _D = 0.30A	n-ch p-ch		0.9 2.1	1.4 2.8	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
C _{iss}	Input Capacitance	N-CHANNEL V _{DS} = 25V, f = 1 MHz, V _{GS} = 0 P-CHANNEL V _{DS} = 25V, f = 1 MHz, V _{GS} = 0	n-ch p-ch		325 260		pF pF
C _{oss}	Output Capacitance		n-ch p-ch		51 52		pF pF
C _{rss}	Reverse Transfer Capacitance		n-ch p-ch		24 25.5		pF pF
R _g	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level=20mV Open Drain	n-ch p-ch		6 6		Ω Ω

(3) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	N-CHANNEL $V_{DD} = 125V, I_D = 1.5A$ $R_G = 4.7\Omega, V_{GS} = 10V$	n-ch p-ch		9 12		ns ns
t_r	Rise Time	P-CHANNEL $V_{DD} = 125V, I_D = 1.5A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (Resistive, see Figure 3)	n-ch p-ch		11 22		ns ns
Q_g	Total Gate Charge	N-CHANNEL $V_{DD} = 200V, I_D = 1.5A,$ $V_{GS} = 10V$	n-ch p-ch		15 16	20 21	nC nC
Q_{gs}	Gate-Source Charge	P-CHANNEL $V_{DD} = 200V, I_D = 1.5A,$ $V_{GS} = 10V$	n-ch p-ch		1.9 1.4		nC nC
Q_{gd}	Gate-Drain Charge	$V_{DD} = 200V, I_D = 1.5A,$ $V_{GS} = 10V$	n-ch p-ch		7 7.6		nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	N-CHANNEL $V_{DD} = 125V, I_D = 1.5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$	n-ch p-ch		31 29.5		ns ns
t_f	Fall Time	P-CHANNEL $V_{DD} = 200V, I_D = 1.5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)	n-ch p-ch		11 7		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current		n-ch p-ch			0.75 0.6	A A
I_{SDM} (4)	Source-drain Current (pulsed)		n-ch p-ch			3 2.4	A A
V_{SD} (5)	Forward On Voltage	$I_{SD} = 3A, V_{GS} = 0$ $I_{SD} = 3A, V_{GS} = 0$	n-ch p-ch			1.5 1.5	V V
t_{rr}	Reverse Recovery Time	N-CHANNEL $I_{SD} = 0.8A, di/dt = 100A/\mu s,$ $V_{DD} = 50V, T_j = 150^\circ C$	n-ch p-ch		127 143		ns ns
Q_{rr}	Reverse Recovery Charge	P-CHANNEL $I_{SD} = 0.60A, di/dt = 100A/\mu s,$ $V_{DD} = 40V, T_j = 150^\circ C$ (see test circuit, Figure 5)	n-ch p-ch		450 806		nC nC
I_{RRM}	Reverse Recovery Current		n-ch p-ch		7 11		A A

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 500 \mu A$ (Open Drain)	± 25			V

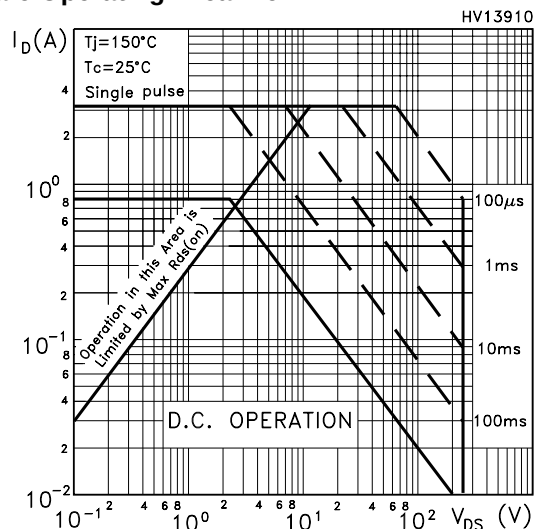
(4) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(5) Pulse width limited by safe operating area

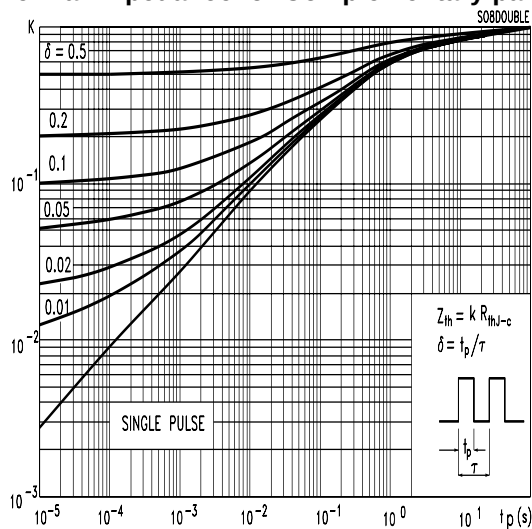
PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

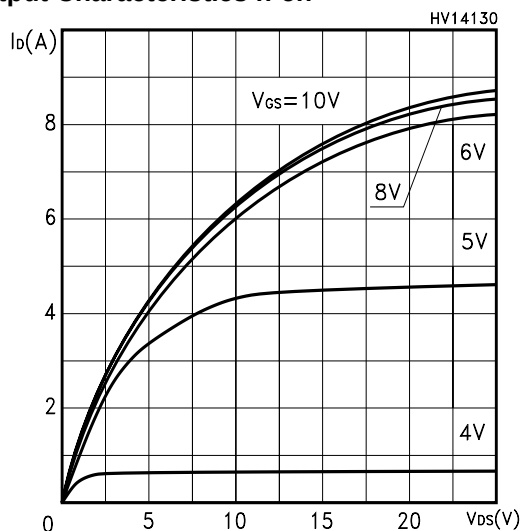
Safe Operating Area n-ch



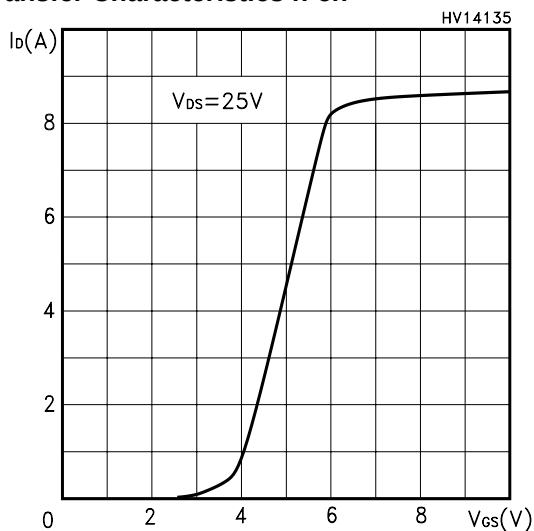
Thermal Impedance for Complementary pair



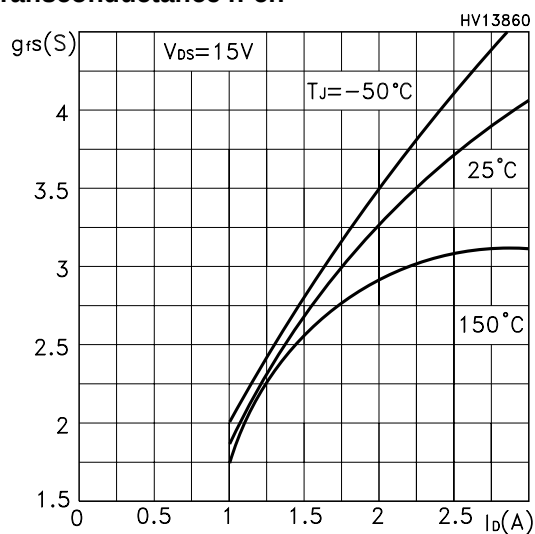
Output Characteristics n-ch



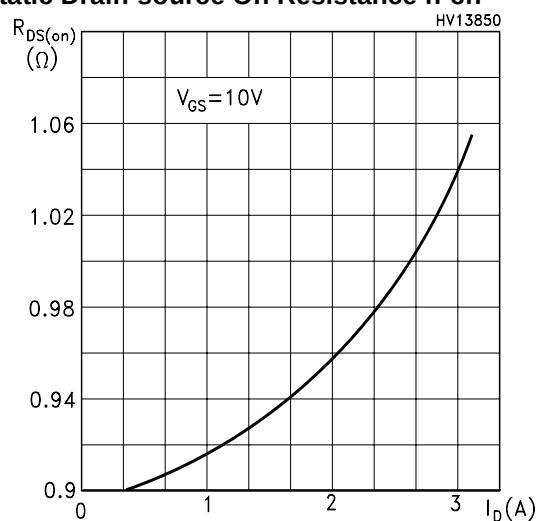
Transfer Characteristics n-ch



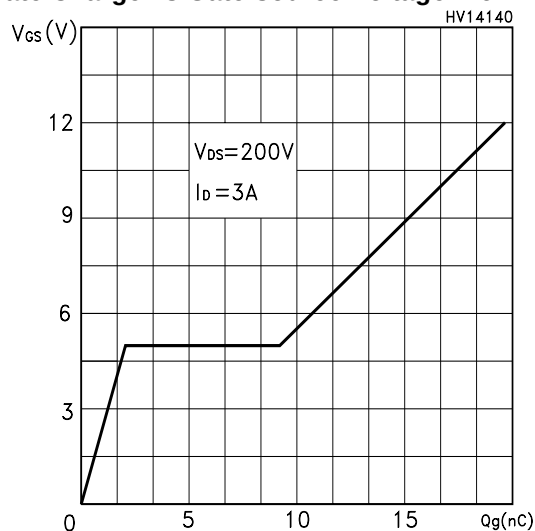
Transconductance n-ch



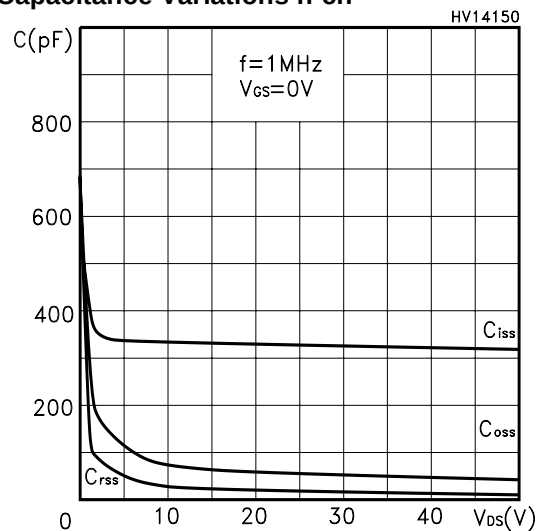
Static Drain-source On Resistance n-ch



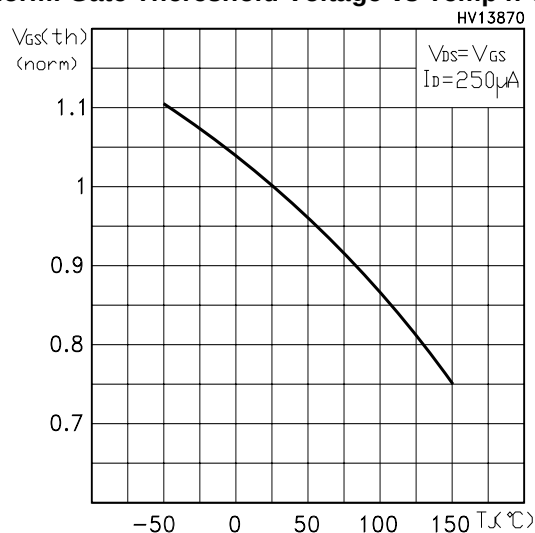
Gate Charge vs Gate-source Voltage n-ch



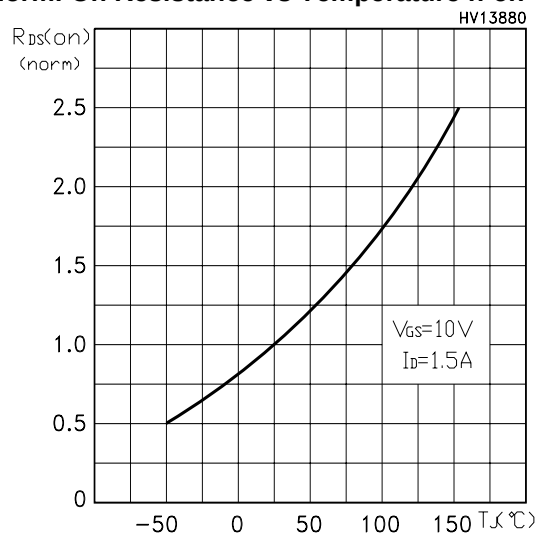
Capacitance Variations n-ch



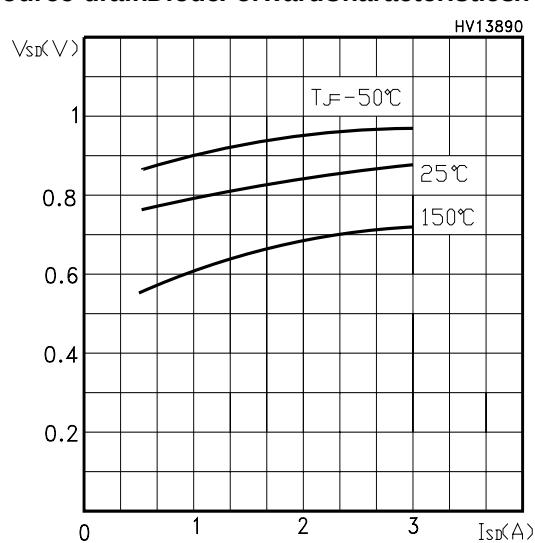
Norm. Gate Threshold Voltage vs Temp n-ch



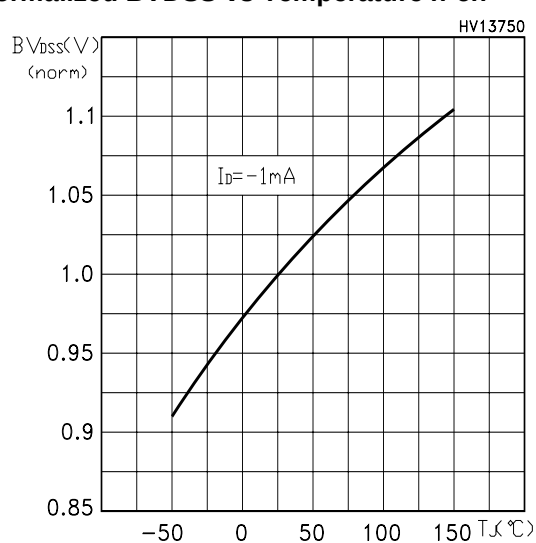
Norm. On Resistance vs Temperature n-ch



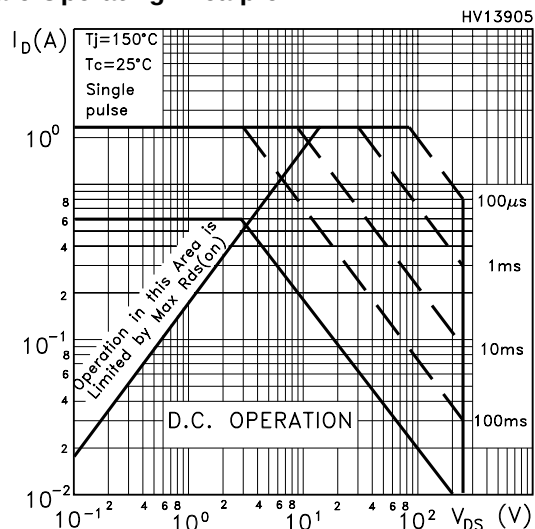
Source-drain Diode Forward Characteristics n-ch



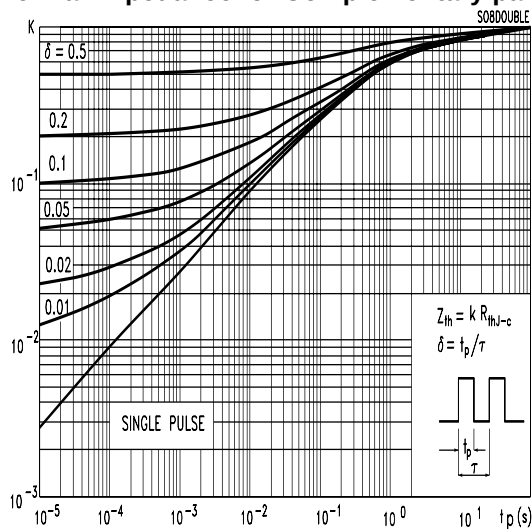
Normalized BVDSS vs Temperature n-ch



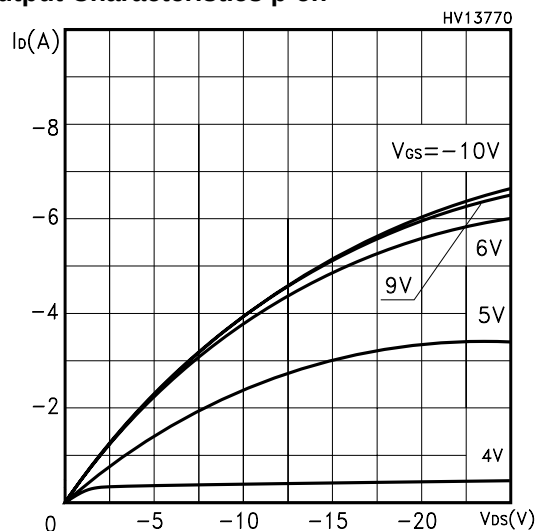
Safe Operating Area p-ch



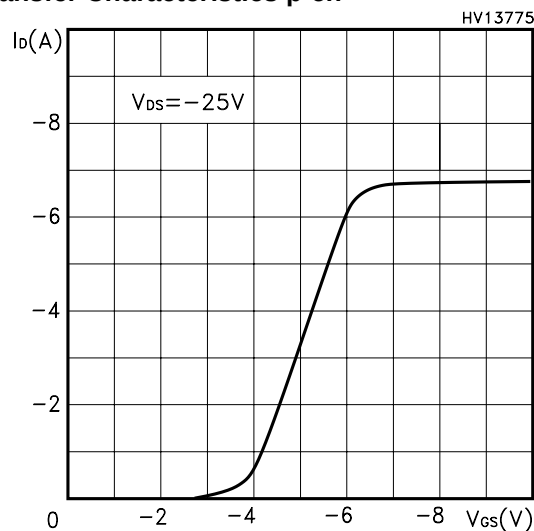
Thermal Impedance for Complementary pair



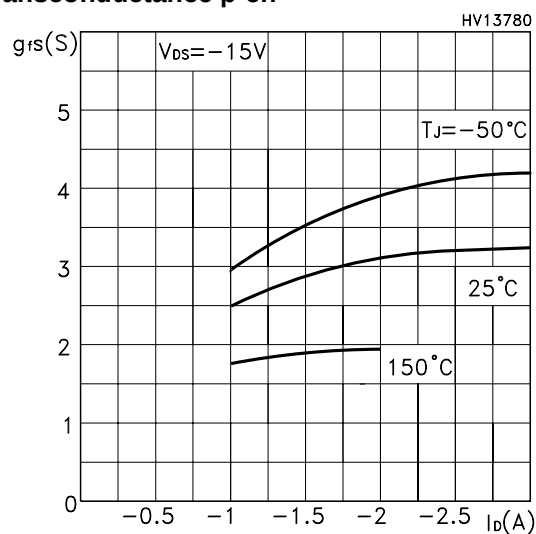
Output Characteristics p-ch



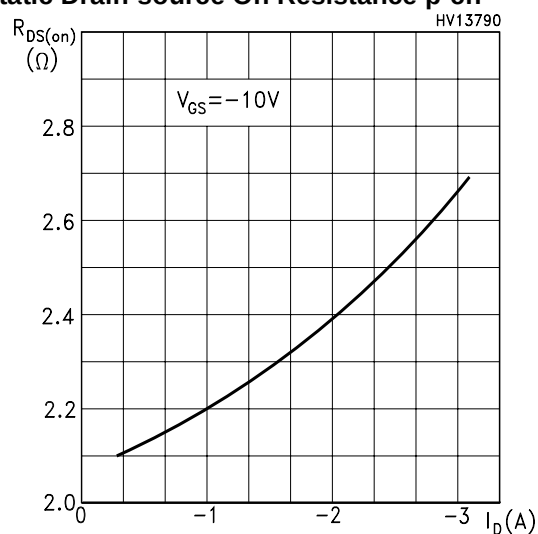
Transfer Characteristics p-ch



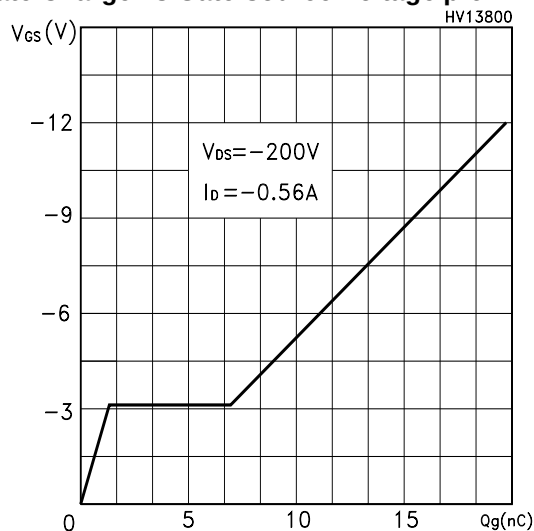
Transconductance p-ch



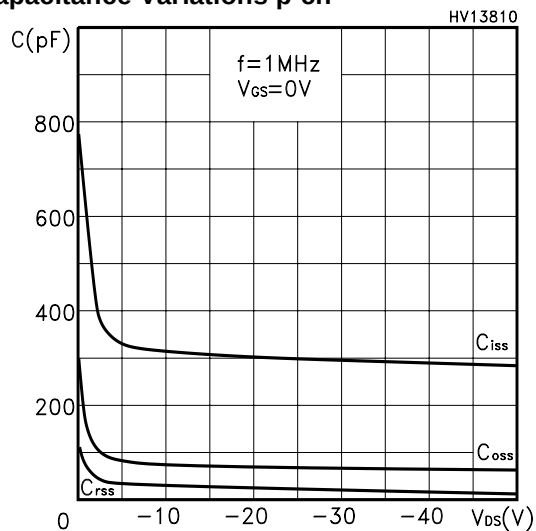
Static Drain-source On Resistance p-ch



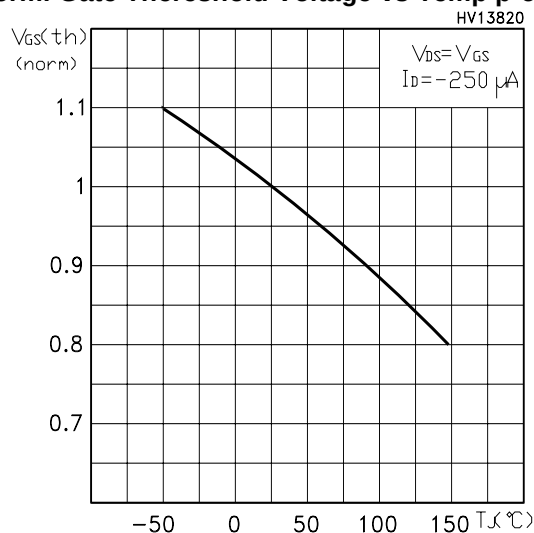
Gate Charge vs Gate-source Voltage p-ch



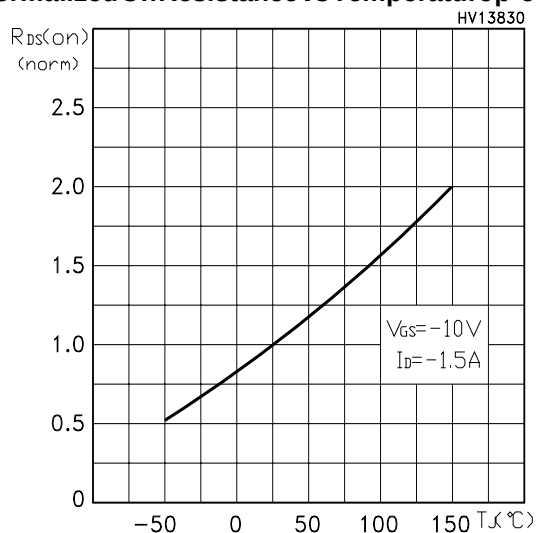
Capacitance Variations p-ch



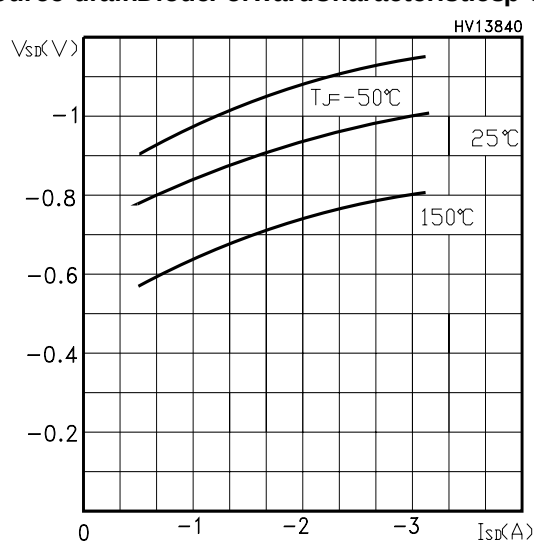
Norm. Gate Threshold Voltage vs Temp p-ch



Normalized OnResistance vs Temperature p-ch



Source-drain Diode Forward Characteristics p-ch



Normalized BVDSS vs Temperature p-ch

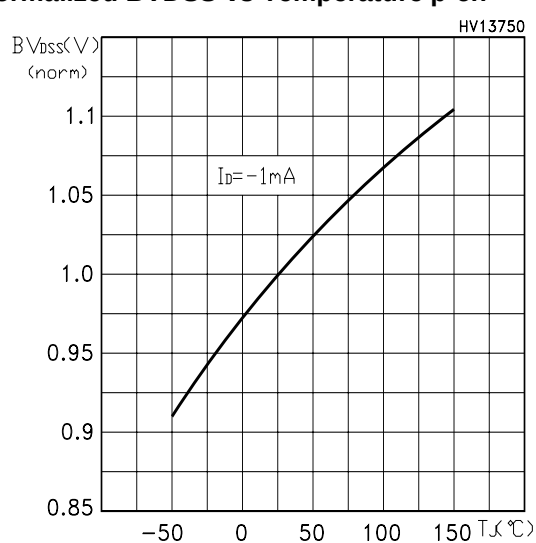


Fig. 1: Unclamped Inductive Load Test Circuit

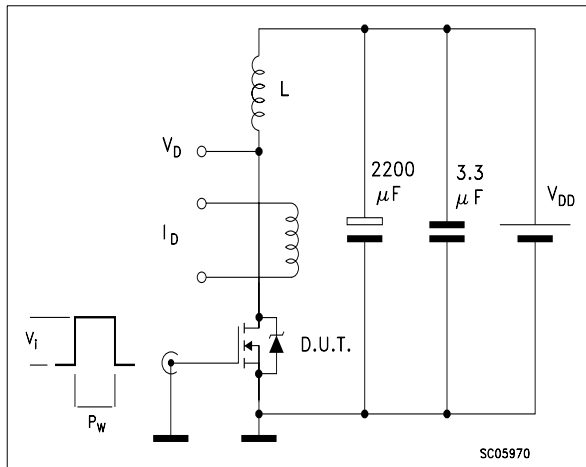


Fig. 2: Unclamped Inductive Waveform

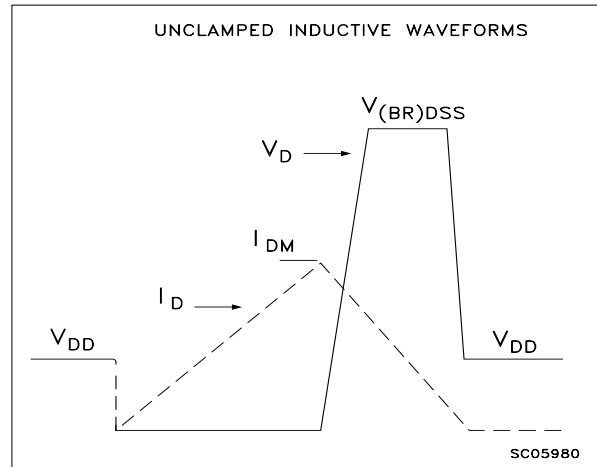


Fig. 3: Switching Times Test Circuit For Resistive Load

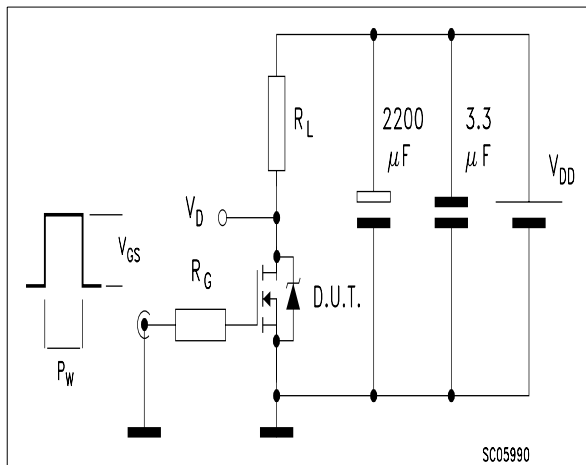


Fig. 4: Gate Charge test Circuit

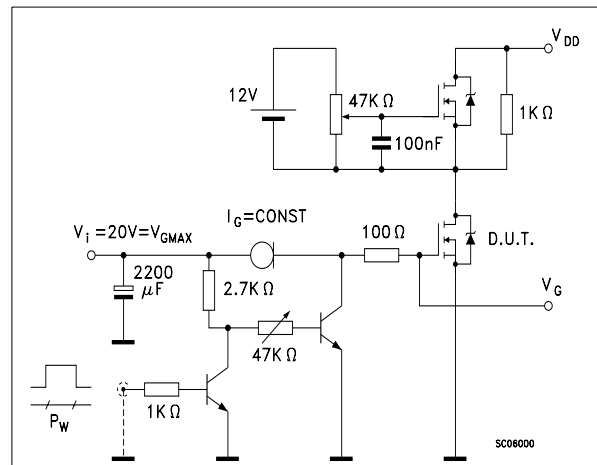
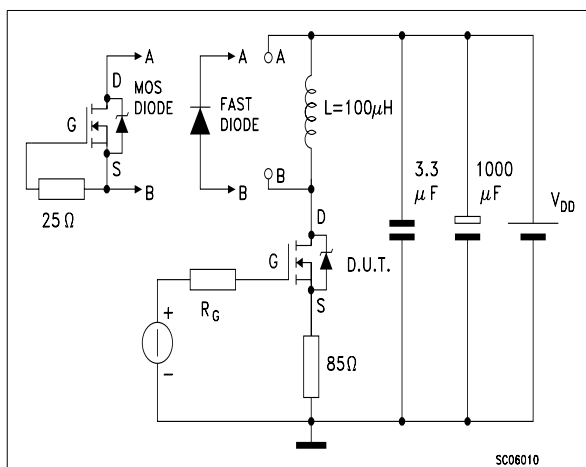
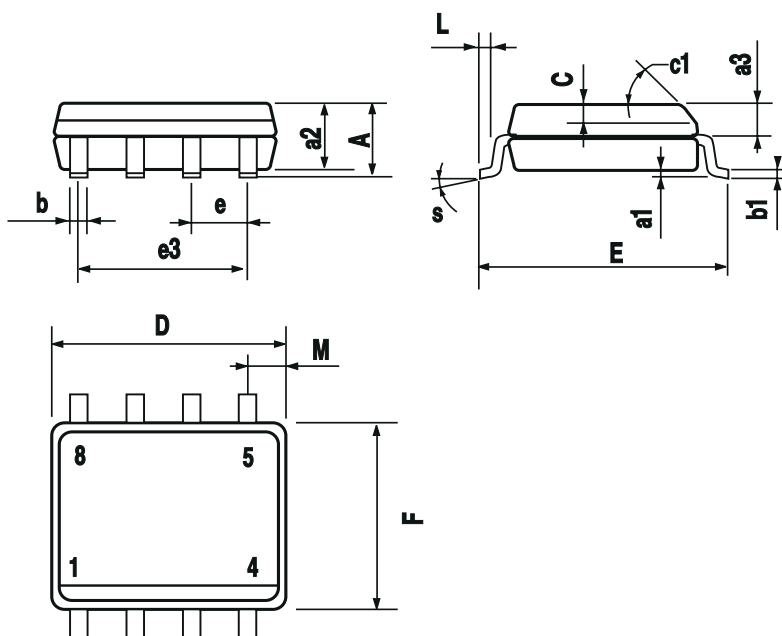


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>