

STD16NE10L

N-CHANNEL 100V - 0.07Ω - 16A DPAK STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD16NE10L	100 V	<0.10 Ω	16 A

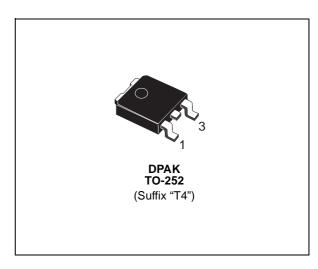
- TYPICAL $R_{DS}(on) = 0.07 \Omega$
- AVALANCHE RUGGED TECHNOLOGY
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175 °C OPERATING TEMPERATURE
- LOW THRESHOLD DRIVE
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

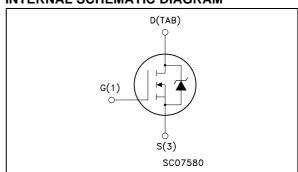
This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low onresistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RALAY DRIVERS
- DC-DC & DC-AC CONVERTERS
- AUTOMOTIVE ENVIRONMENT



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	100	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	16	А
I _D	Drain Current (continuous) at T _C = 100°C	11	А
I _{DM} (●)	Drain Current (pulsed)	64	А
P _{tot}	Total Dissipation at T _C = 25°C	90	W
	Derating Factor	0.6	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	75	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
Tj	Operating Junction Temperature	-55 to 175	

^(•) Pulse width limited by safe operating area

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⁽¹⁾ $I_{SD} \le 16A$, di/dt $\le 300A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_j \le T_{JMAX}$ (2) Starting $T_j = 25$ °C, $I_D = 8A$, $V_{DD} = 30V$

THERMAL DATA

Rthj-case Rthj-amb T _I	Thermal Resistance Junction-case Thermal Resistance Junction-ambient Maximum Lead Temperature For Soldering Purpose	Max Max	1.67 100 275	°C/W °C/W
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ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	$V_{DS} = Max Rating$ $V_{DS} = Max Rating T_C = 125^{\circ}C$			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I _D = 250 μA	1	1.7	2.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V V _{GS} = 5 V	I _D = 8 A I _D = 8 A		0.07 0.085	0.085 0.01	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (*)	Forward Transconductance	$V_{DS}>I_{D(on)}xR_{DS(on)max}$ $I_{D}=8A$	5	9		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1 MHz$, $V_{GS} = 0$		1750 165 45		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	$\begin{aligned} &V_{DD} = 50 \text{ V} & I_{D} = 8 \text{ A} \\ &R_{G} = 4.7 \Omega & V_{GS} = 4.5 \text{ V} \\ &(\text{Resistive Load, Figure 3}) \end{aligned}$		40 80		ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 80 V I _D = 16 A V _{GS} = 5V		24 5.5 11	32	nC nC nC

SWITCHING OFF

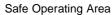
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(off)} t _f	Turn-off Delay Time Fall Time	$\begin{array}{ccc} V_{DD} = 50 \text{ V} & I_D = 8 \text{ A} \\ R_G = 4.7\Omega, & V_{GS} = 4.5 \text{ V} \\ \text{(Resistive Load, Figure 3)} \end{array}$		45 12		ns ns
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{clamp} = 80 \text{ V}$ $I_D = 16 \text{ A}$ $R_G = 4.7\Omega,$ $V_{GS} = 4.5 \text{ V}$ (Inductive Load, Figure 5)		12 17 35		ns ns ns

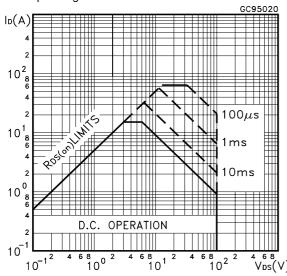
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				16 64	A A
V _{SD} (*)	Forward On Voltage	I _{SD} = 16 A V _{GS} = 0			1.5	V
t _{rr} Q _{rr} IRRM	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 16 A di/dt = 100A/µs V_{DD} = 40 V T_j = 150°C (see test circuit, Figure 5)		100 300 6		ns nC A

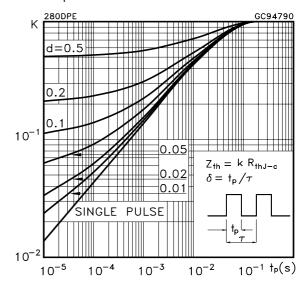
^(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

(•)Pulse width limited by safe operating area.



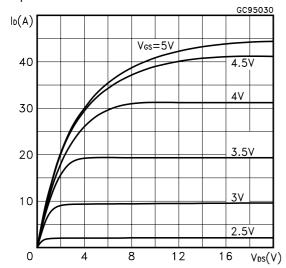


Thermal Impedance

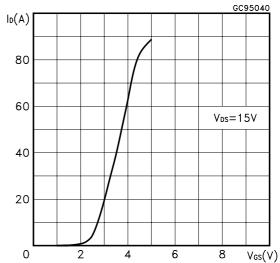


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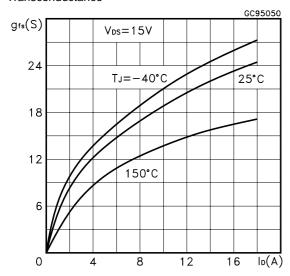
Output Characteristics



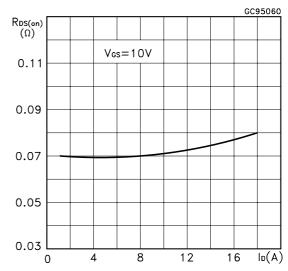
Transfer Characteristics



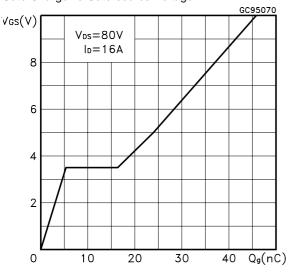
Transconductance



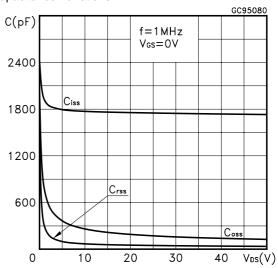
Static Drain-source On Resistance



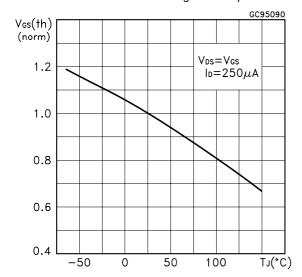
Gate Charge vs Gate-source Voltage



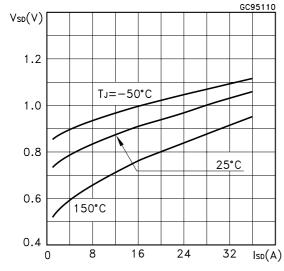
Capacitance Variations



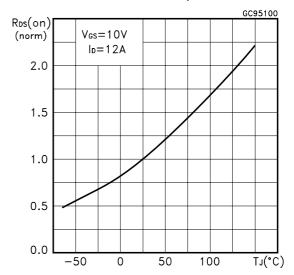
Normalized Gate Threshold Voltage vs Temperature



Source-drain Diode Forward Characteristics



Normalized on Resistance vs Temperature



Normalized Breakdown Voltage Temperature

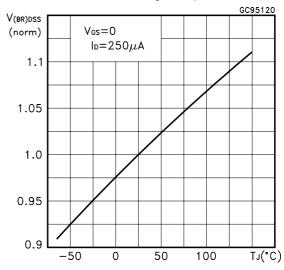


Fig. 1: Unclamped Inductive Load Test Circuit

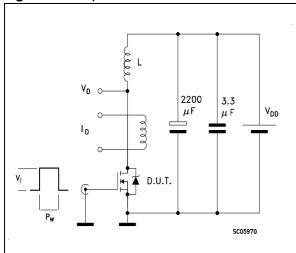


Fig. 3: Switching Times Test Circuits For Resistive Load

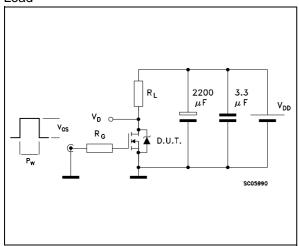


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

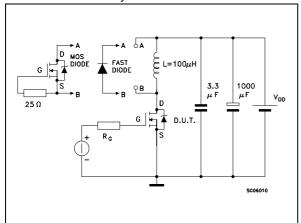


Fig. 2: Unclamped Inductive Waveform

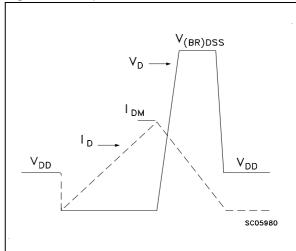
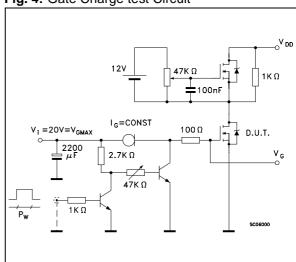
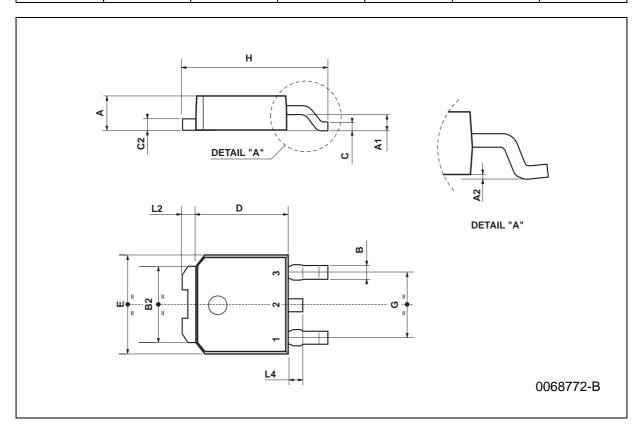


Fig. 4: Gate Charge test Circuit



TO-252 (DPAK) MECHANICAL DATA

DIM.		mm			inch	
Dilli.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
В	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
Н	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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