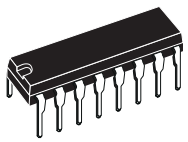
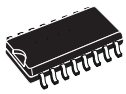
HCF4543B

BCD-TO-7-SEGMENT LATCH/DECODER/LCD DRIVER

- DISPLAY BLANKING OF ALL ILLEGAL INPUT COMBINATIONS
- LATCH STORAGE OF CODE
- INSTRUMENT DISPLAY DRIVER
- DASHBOARD DISPLAY DRIVER
- COMPUTER/CALCULATOR DISPLAY DRIVER
- TIMING DEVICE DRIVER (CLOCKS, WATCHES, TIMERS)
- PIN FOR PIN REPLACEMENT OF HCF4056B (PIN 7 CONNECTED TO V_{SS})
- DIRECT LED DRIVING CAPABILITY
- 5V, 10V AND 15V PARAMETRIC RATINGS
- MAXIMUM INPUT CURRENT OF 1A AT 18V OVER FULL PACKAGE TEMPERATURE RANGE; 100nA at 18V AND 25°C
- NOISE MARGIN (FULL PACKAGE TEMPERATURE RANGE):
  1V at V_{DD} = 5V ;
  2V at V_{DD} = 10V;
  2.5V at V_{DD} = 15V
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP



SOP

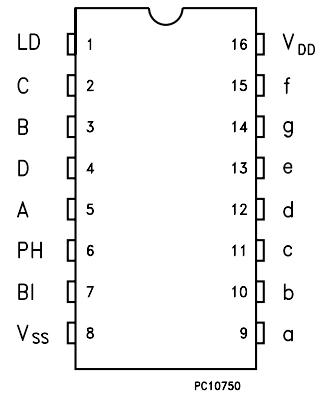
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4543BEY	
SOP	HCF4543BM1	HCF4543M013TR

DESCRIPTION

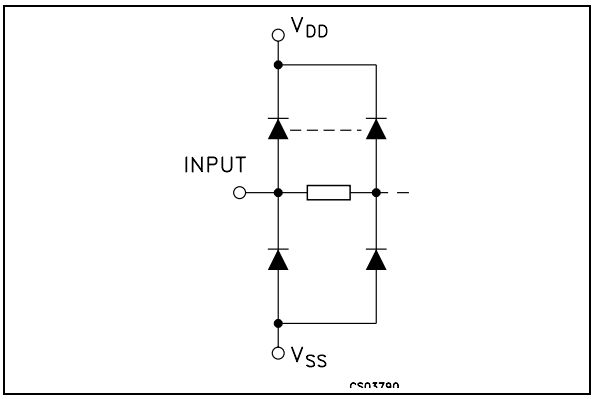
HCF4543B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
HCF4543B is a BCD-TO-7-SEGMENT LATCH/ DECODER/LCD DRIVER designed primarily for liquid crystal display (LCD) applications. It is also capable of driving light emitting diodes (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement of HCF4056B when pin 7 is connected to V_{SS}. It differs from HCF4056B in that it has a display blanking capability instead of a level shifting function and requires only one power supply. When HCF4056B is used in the level shifting mode, two power supplies are required. When the HCF4543B is used for LCD applications, a square wave must be applied to the phase input and the backplane of

PIN CONNECTION



the LCD device. For LED applications a logic 1 is required at the PHASE input for common cathode devices; a logic 0 is required for common-anode devices (see truth table).

IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

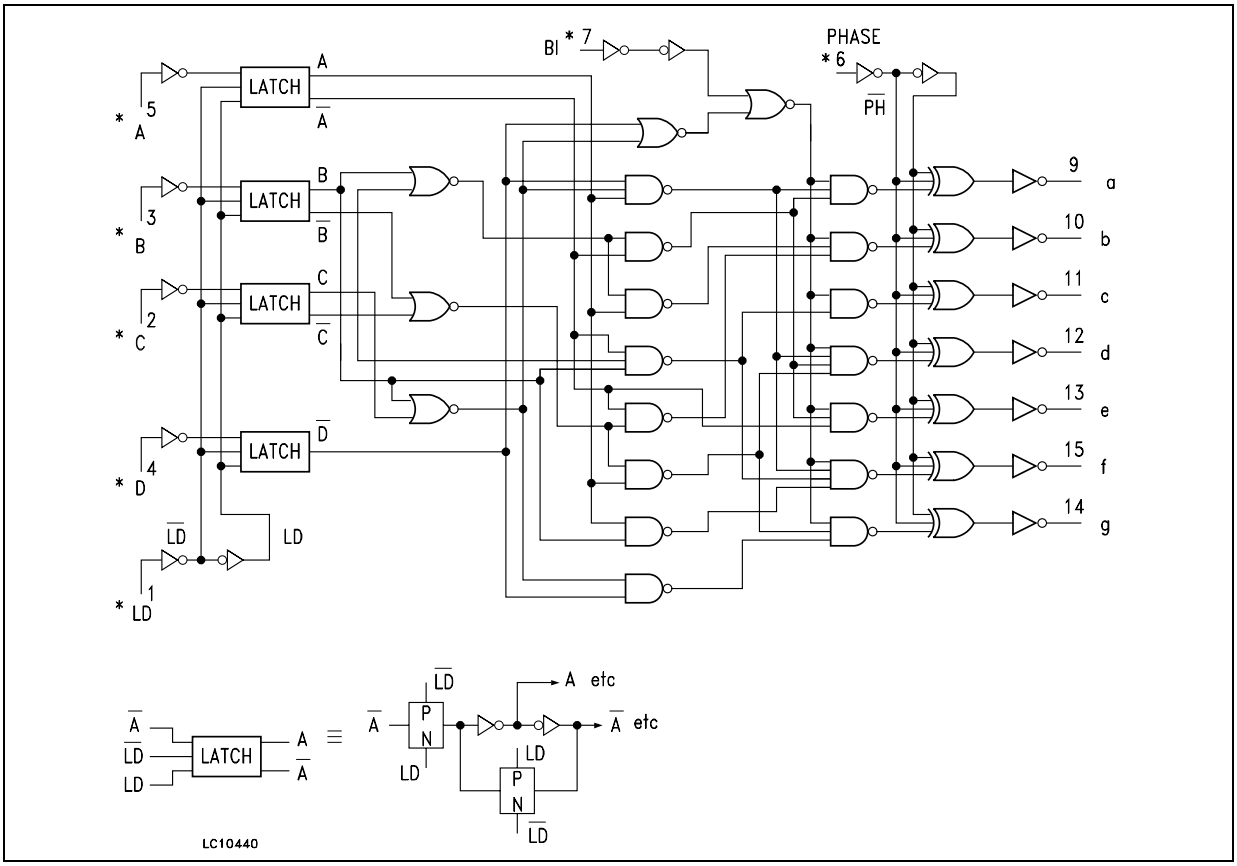
PIN No	SYMBOL	NAME AND FUNCTION
9, 10, 11, 12, 13, 15, 14	a to g	Decoded Outputs
5, 3, 2, 4	A, B, C, D	Data Inputs
1	LD	Latch Disable Inputs
6	PH	Phase Inputs
7	BI	Blanking Input
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

TRUTH TABLE

INPUT CODE							OUTPUT STATE							DISPLAY CHARACTER
LD	BI	PH*	D	C	B	A	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	BLANK
H	L	L	H	L	H	H	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	L	L	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	L	H	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	H	L	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	H	H	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X	**							**
•	•	•	•				INVERSE OF OUTPUT COMBINATIONS ABOVE							DISPLAY AS ABOVE

X : Don't Care
* : For Liquid-Crystal readouts apply a square to Ph.
For common cathode LED readouts, select Ph=0
For common anode LED readouts, select Ph=1
**: Depends upon the BCD code previously applied when LD=1
• : Above Combination

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.1	-2.6		-0.9		-0.9		mA
		0/5	4.6	<1	5	-0.31	-0.75		-0.25		-0.25		
		0/10	9.5	<1	10	-0.68	-1.6		-0.54		-0.54		
		0/15	13.5	<1	15	-2.3	-5.4		-1.84		-1.84		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

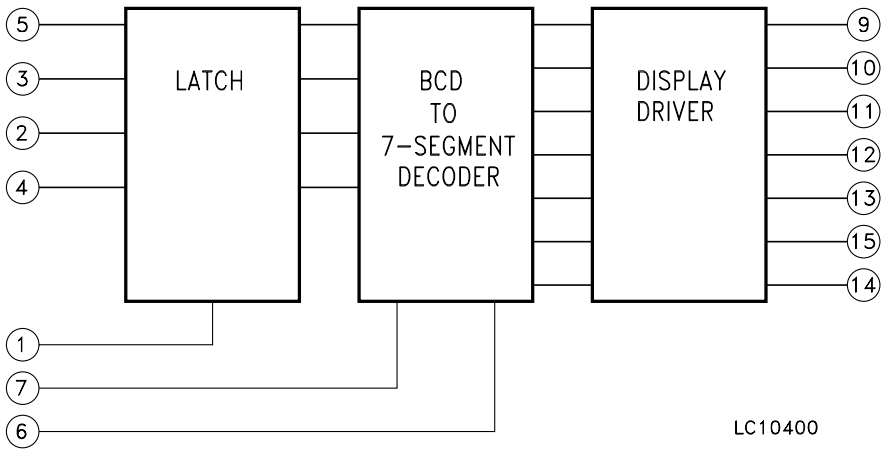
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

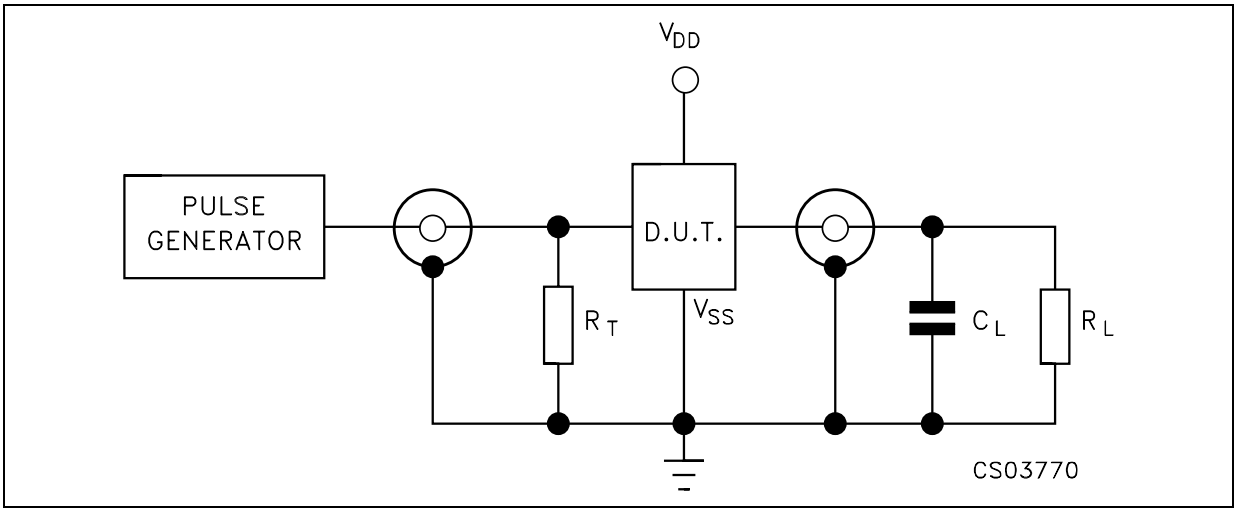
Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL}	Propagation Delay Time	5			600	1200	ns
		10			200	400	
		15			150	300	
t_{PLH}	Propagation Delay Time	5			500	1000	ns
		10			200	400	
		15			150	300	
t_{THL}	Transition Time	5			180	360	ns
		10			90	180	
		15			65	130	
t_{TLH}	Transition Time	5			180	360	ns
		10			90	180	
		15			65	130	
t_{WH}	Latch Disable Pulse Width	5		250	125		ns
		10		100	50		
		15		80	40		
t_{SU}	Address Setup Time	5		60	15		ns
		10		20	-5		
		15		10	-5		
t_H	Address Hold Time	5		25	-5		ns
		10		20	10		
		15		20	0		

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

BCD TO 7 SEGMENT LATCH/DECODER/DRIVER FUNCTIONAL DIAGRAM

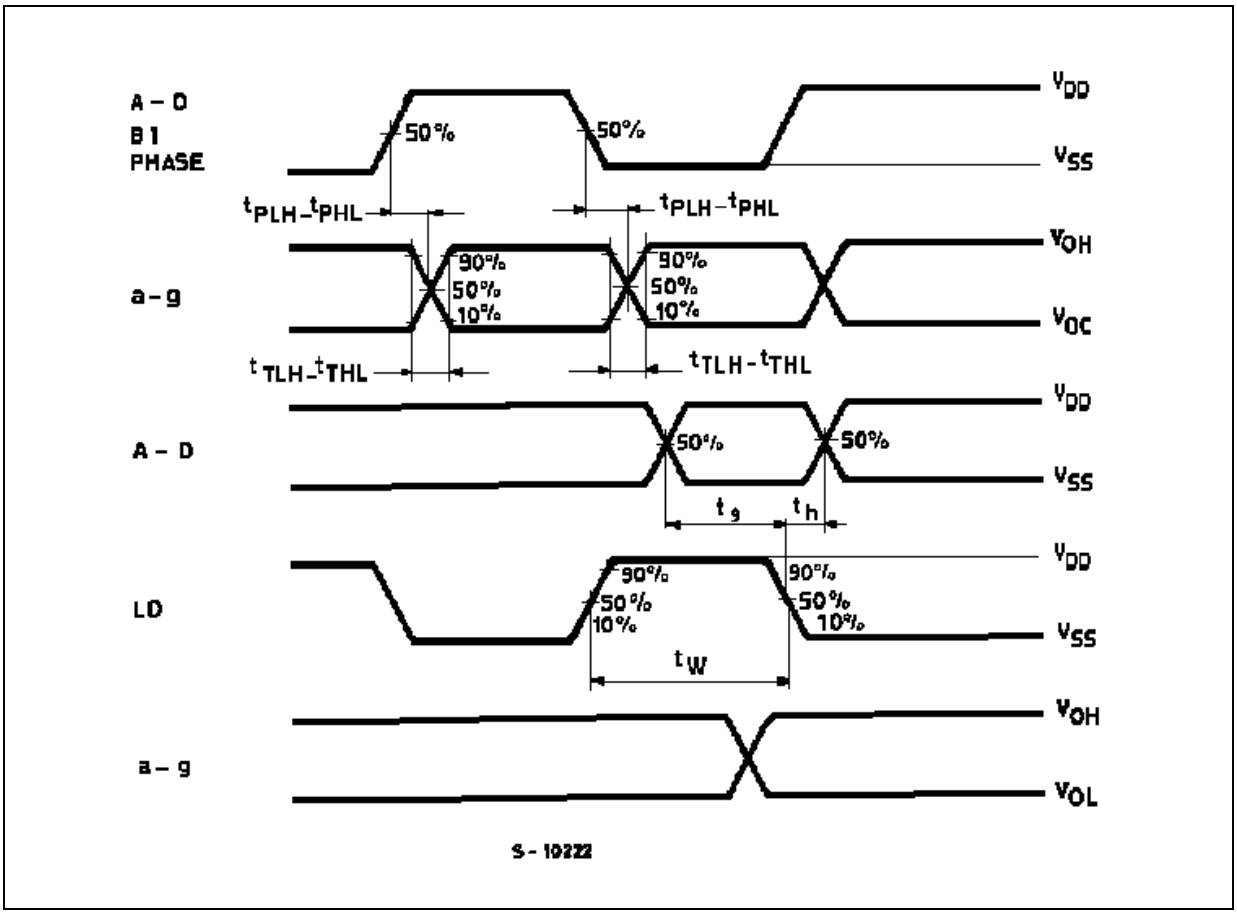


TEST CIRCUIT



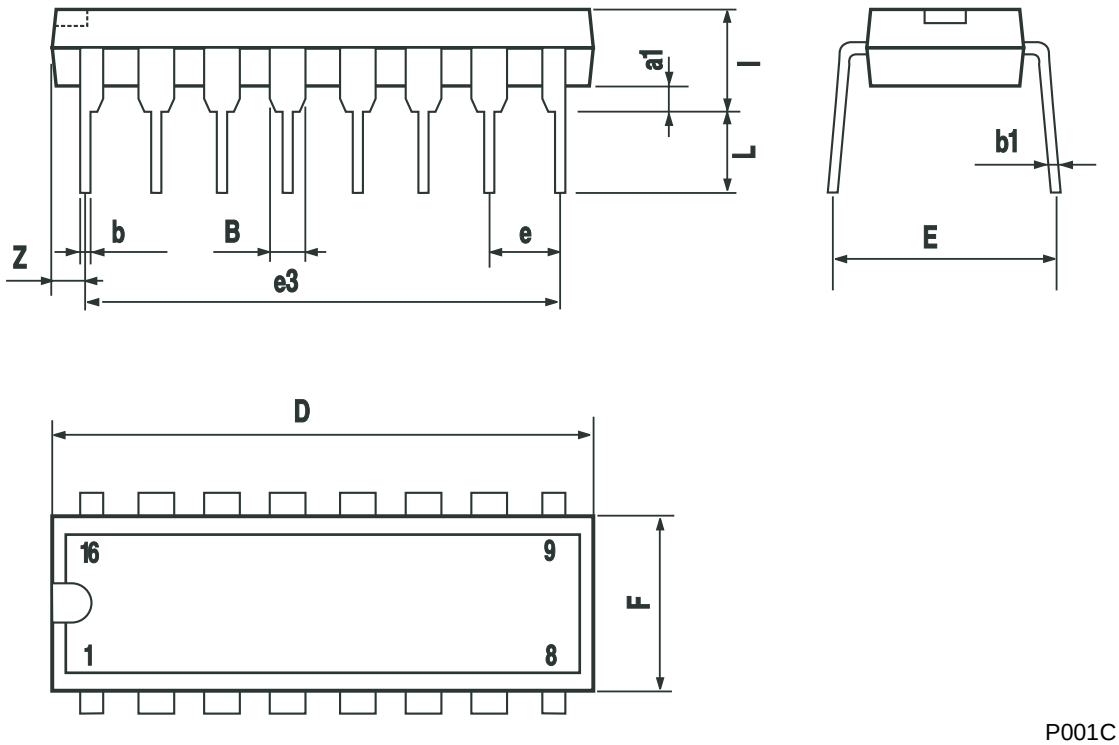
C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY, PULSE WIDTH, SETUP and HOLD TIME (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

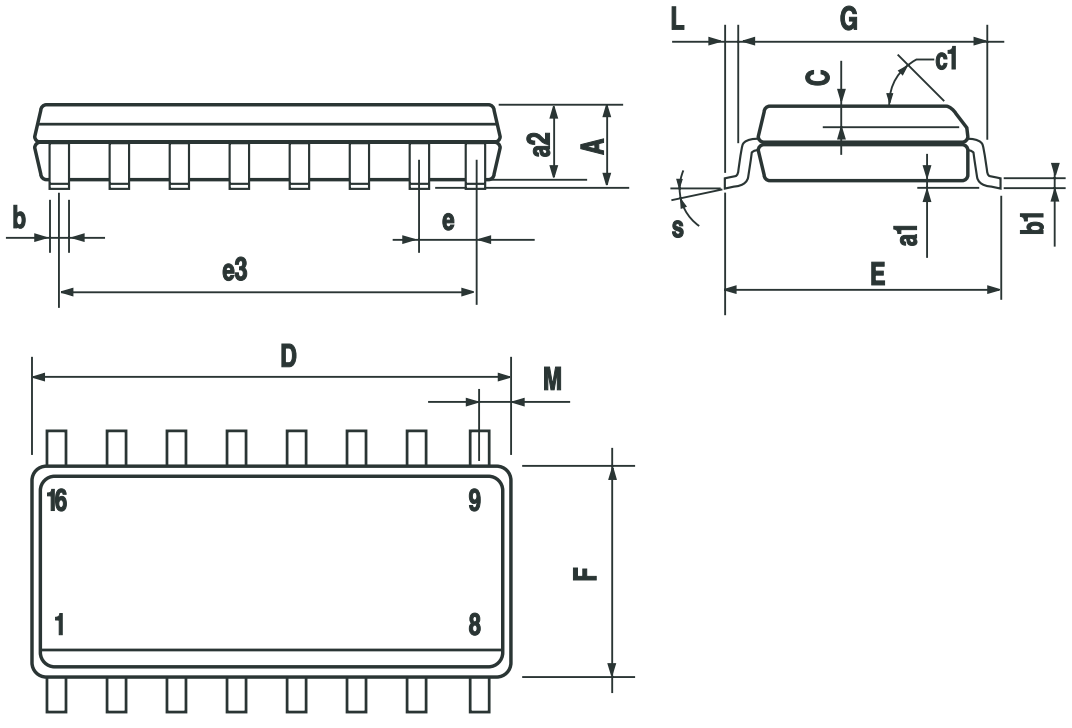
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H